

Interline Unified Power Quality Conditioner

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Abstract—This paper proposes a new connection for a unified power quality conditioner (UPQC) to improve the power quality of two feeders in a distribution system. A UPQC consists of a series voltage-source converter (VSC) and a shunt VSC both joined together by a common dc bus. It is demonstrated how this device is connected between two independent feeders to regulate the bus voltage of one of the feeders while regulating the voltage across a sensitive load in the other feeder. Since the UPQC is connected between two different feeders (lines), this connection of the UPQC will be called an interline UPQC (IUPQC). The structure, control and capability of the IUPQC are discussed in this paper. The efficacy of the proposed configuration has been verified through simulation studies using PSCAD/EMTDC.

Index Terms—Distribution system, power quality, sensitive load, voltage sag, voltage-source converter (VSC).

I. INTRODUCTION

VOLTAGE-SOURCE CONVERTER (VSC)-based custom power devices are increasingly being used in custom power applications for improving the power quality (PQ) of power distribution systems. Devices such as distribution static compensator (DSTATCOM) and dynamic voltage restorer (DVR) have already been discussed extensively in [1]. A DSTATCOM can compensate for distortion and unbalance in a load such that a balanced sinusoidal current flows through the feeder [2]. It can also regulate the voltage of a distribution bus [3], [4]. A DVR can compensate for voltage sag/swell and distortion in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated [5], [6]. A unified power-quality conditioner (UPQC) can perform the functions of both DSTATCOM and DVR [7], [8]. The UPQC consists of two voltage-source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor.

It is also possible to connect two VSCs to two different feeders in a distribution system. In [9], a configuration called IDVR has been discussed in which two DVRs are connected in series with two separate adjacent feeders. The dc buses of the DVRs are connected together. The IDVR absorbs real

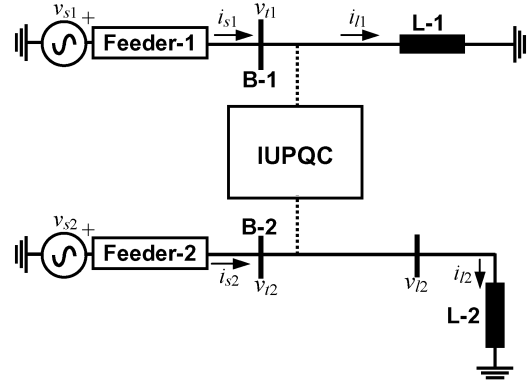


Fig. 1. Single-line diagram of an IUPQC-connected distribution system.

power from one feeder and maintains the dc link voltage to mitigate 40% (about 0.6 p.u.) voltage sag in the other feeder with balanced loads connected in the distribution system. It is also possible to connect two shunt VSCs to different feeders through a common dc link. This can also perform the functions of the two DVRs mentioned above, albeit with higher device rating.

This paper presents a new connection for a UPQC called interline UPQC (IUPQC). The single-line diagram of an IUPQC connected distribution system is shown in Fig. 1. Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations, supply the system loads L-1 and L-2. The supply voltages are denoted by v_{s1} and v_{s2} . It is assumed that the IUPQC is connected to two buses B-1 and B-2, the voltages of which are denoted by v_{t1} and v_{t2} , respectively. Further two feeder currents are denoted by i_{s1} and i_{s2} while the load currents are denoted by i_{l1} and i_{l2} . The load L-2 voltage is denoted by v_{l2} .

The purpose of the IUPQC is to hold the voltages v_{t1} and v_{t2} constant against voltage sag/swell, temporary interruption in either of the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say Feeder-1) to hold v_{l2} constant in case of a sag in the voltage v_{s2} . This can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed. The performance of the IUPQC has been evaluated through simulation studies using PSCAD/EMTDC.

II. STRUCTURE AND CONTROL

The IUPQC shown in Fig. 1 consists of two VSCs (VSC-1 and VSC-2) that are connected back to back through a common energy storage dc capacitor C_{dc} . Let us assume that the VSC-1 is connected in shunt to Feeder-1 while the VSC-2 is connected in series with Feeder-2. Each of the two VSCs is realized by

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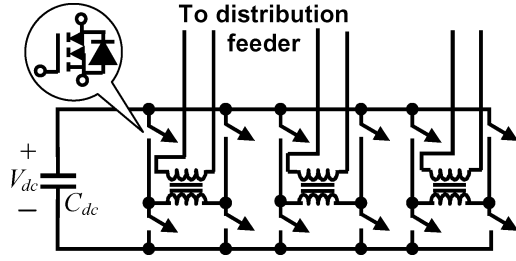


Fig. 2. Schematic structure of a VSC.

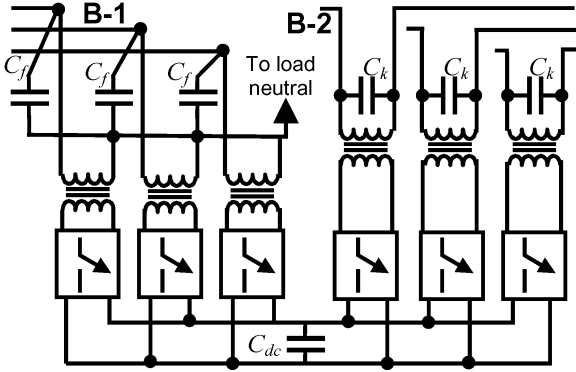


Fig. 3. Complete structure of an IUPQC.

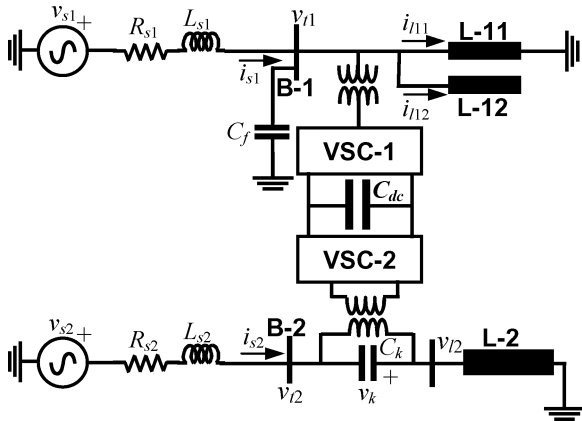


Fig. 4. Typical IUPQC connected in a distribution system.

three H-bridge inverters [10], [11]. The schematic structure of a VSC is shown in Fig. 2. In this structure, each switch represents a power semiconductor device (e.g., IGBT) and an anti-parallel diode as shown in Fig. 2. All the inverters are supplied from a common single dc capacitor (C_{dc}) and each inverter has a transformer connected at its output.

The complete structure of a three-phase IUPQC with two such VSCs is shown in Fig. 3. The secondary (distribution) sides of the shunt-connected transformers (VSC-1) are connected in star with the neutral point being connected to the load neutral. The secondary winding of the series-connected transformers (VSC-2) are directly connected in series with the bus B-2 and load L-2. The ac filter capacitors C_f and C_k are also connected in each phase (Fig. 3) to prevent the flow of the harmonic currents generated due to switching. The six inverters of the IUPQC are controlled independently. The switching action is obtained

TABLE I
SYSTEM PARAMETERS

System quantities	Values
System fundamental frequency (f)	50 Hz
Voltage source v_{s1}	11 kV (L-L, rms), phase angle 0°
Voltage source v_{s2}	11 kV (L-L, rms), phase angle 0°
Feeder-1 ($R_{s1} + j2\pi L_{s1}$)	Impedance: $6.05 + j36.28 \Omega$
Feeder-2 ($R_{s2} + j2\pi L_{s2}$)	Impedance: $3.05 + j18.14 \Omega$
Load L-11	Phase-a $24.2 + j60.50 \Omega$
Unbalanced RL component	Phase-b $36.2 + j78.54 \Omega$
	Phase-c $48.2 + j94.25 \Omega$
Load L-12	A three-phase diode rectifier that supplies a load of $250 + j31.42 \Omega$
Non-linear component	
Balanced Load L-2 impedance	$72.6 + j54.44 \Omega$

using output feedback control. The controller is designed in discrete-time using pole-shifting law in the polynomial domain [1], [12], as discussed in Appendix A.

III. SYSTEM DESCRIPTION

An IUPQC connected to a distribution system is shown in Fig. 4. In this figure, the feeder impedances are denoted by the pairs (R_{s1}, L_{s1}) and (R_{s2}, L_{s2}) . It can be seen that the two feeders supply the loads L-1 and L-2. The load L-1 is assumed to have two separate components—an unbalanced part (L-11) and a non-linear part (L-12). The currents drawn by these two loads are denoted by i_{l11} and i_{l12} , respectively. We further assume that the load L-2 is a sensitive load that requires uninterrupted and regulated voltage. The shunt VSC (VSC-1) is connected to bus B-1 at the end of Feeder-1, while the series VSC (VSC-2) is connected at bus B-2 at the end of Feeder-2. The voltages of buses B-1 and B-2 and across the sensitive load terminal are denoted by v_{t1} , v_{t2} , and v_{l2} , respectively. The aim of the IUPQC is two-fold:

- to protect the sensitive load L-2 from the disturbances occurring in the system by regulating the voltage v_{l2} ;
- to regulate the bus B-1 voltage v_{t1} against sag/swell and or disturbances in the system.

In order to attain these aims, the shunt VSC-1 is operated as a voltage controller while the series VSC-2 regulates the voltage v_{l2} across the sensitive load.

The system parameters used in the study are given in Table I. The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2. The voltage of bus B-1 and load L-1 currents, when no IUPQC is connected to the distribution system, are shown in Fig. 5. In this figure and in all the remaining figures showing three phase waveforms, the phases a, b and c are depicted by solid, dashed and dotted lines, respectively. It can be seen from Fig. 5(a), that due to the presence of unbalanced and non-linear load L-1, the voltage v_{t1} is both unbalanced and distorted. Also, the load L-11 causes an unbalance in the current i_{l12} , while load L-12 causes distortion in the current i_{l11} . We shall now demonstrate how these waveforms can be improved using the IUPQC.

IV. IUPQC OPERATION

As mentioned before, the shunt VSC (VSC-1) holds the voltage of bus B-1 constant. This is accomplished by making

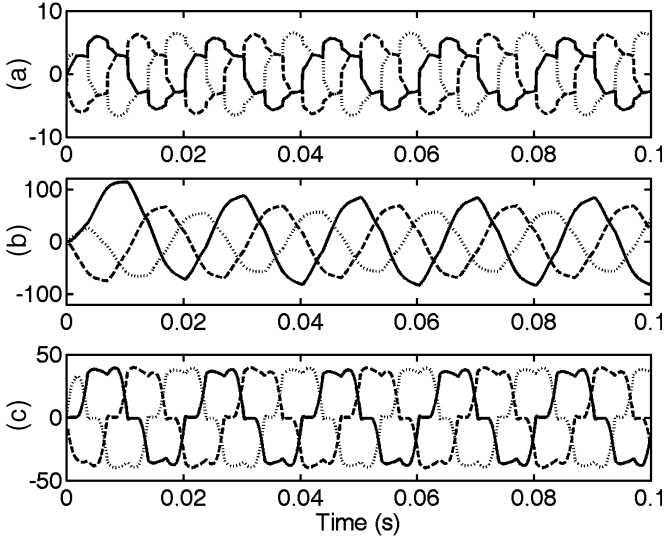


Fig. 5. Voltages and currents in the absence of IUPQC: (a) B-1 bus voltages (v_{t1}), kV, (b) L-11 load currents (i_{l11}), A, and (c) L-12 load currents (i_{l12}), A.

the VSC-1 to track a reference voltage across the filter capacitor C_f . The equivalent circuit of the VSC-1 is shown in Fig. 6(a) in which $u_1 \cdot V_{dc}$ denote the inverter output voltage where V_{dc} is dc capacitor voltage and u_1 is switching action equal to $\pm n_1$ where n_1 is turns ratio of the transformers of VSC-1. In Fig. 6(a), the inverter losses and leakage inductance of the transformers are denoted by R_{f1} and L_{f1} , respectively. All system parameters are referred to the line side of the transformers.

Defining the state vector as $x_1^T = [v_{t1} \ i_{f1}]$, the state space model for the VSC-1 is written as

$$\begin{aligned} \dot{x}_1 &= F_1 x_1 + G_1 z_1 \\ y_1 &= v_{t1} = H x_1 \end{aligned} \quad (1)$$

where

$$F_1 = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_{f1}} & -\frac{R_{f1}}{L_{f1}} \end{bmatrix}, \quad G_1 = \begin{bmatrix} 0 & -\frac{1}{C_f} \\ \frac{V_{dc}}{L_{f1}} & 0 \end{bmatrix}$$

$$H = [1 \ 0], \quad z_1 = \begin{bmatrix} u_{1c} \\ i_{sh} \end{bmatrix}.$$

Note that u_{1c} is the continuous time equivalent of u_1 . The system given in (1) is discretized and is written in input–output form as

$$A_1(z^{-1})y_1(k) = B_1(z^{-1})u_{1c}(k) + C_1(z^{-1})\eta_1(k) \quad (2)$$

where η_1 is a disturbance which is equal to i_{sh} . A pole-shift controller is used to determine the switching action u_1 from u_{1c} . The controller is discussed in Appendix A and is used to track a reference signal $y_{1ref}(k)$.

The reference $y_{1ref}(k)$ is the desired voltage of the bus B-1. The peak of this instantaneous voltage is pre-specified and its phase angle (δ_1) is adjusted to maintain the power balance in the system. To set the phase angle, we note that the dc capacitor (C_{dc} in Fig. 4) must be able to supply VSC-1 while maintaining its dc bus voltage constant by drawing power from the ac system [4].

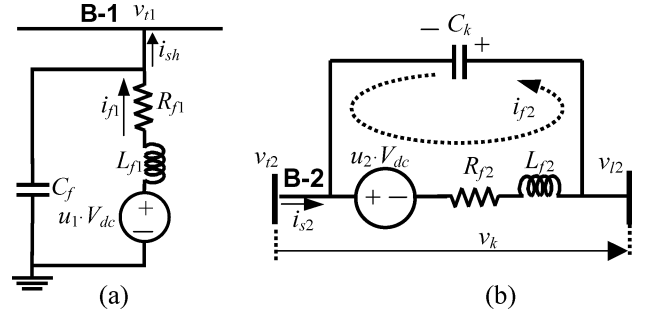


Fig. 6. Single-phase equivalent circuit of (a) VSC-1 and (b) VSC-2.

A proportional controller is used for controlling the dc capacitor voltage (V_{dc}) and is given by

$$\delta_1 = K_P(V_{dcref} - V_{dcav}) \quad (3)$$

where V_{dcav} is the average voltage across the dc capacitor over a cycle, V_{dcref} is its set reference value and K_P is the proportional gain. It is to be noted that the average voltage V_{dcav} is obtained using a moving average low pass filter to eliminate all switching components from the signal.

The equivalent circuit of the VSC-2 is shown in Fig. 6(b) and is similar to the one shown in Fig. 6(a) in every respect. Defining a state and input vector, respectively, as $x_2^T = [v_k \ i_{f2}]$ and $z_2^T = [u_{2c} \ i_{s2}]$, and the state space model for VSC-2 is given as

$$\begin{aligned} \dot{x}_2 &= F_2 x_2 + G_2 z_2 \\ y_2 &= v_k = H x_2 \end{aligned} \quad (4)$$

where F_2 and G_2 are matrices that are similar to F_1 and G_1 , respectively. The discrete-time input–output equivalent of (4) is given as

$$A_2(z^{-1})y_2(k) = B_2(z^{-1})u_{2c}(k) + C_2(z^{-1})\eta_2(k) \quad (5)$$

where the disturbance η_2 is equal to i_{s2} . We now use a separate pole-shift controller to determine the switching action u_2 from u_{2c} so as to track the reference signal $y_{2ref}(k)$.

Note from Fig. 4 that the purpose of the VSC-2 is to hold the voltage v_{l2} across the sensitive load L-2 constant. Let us denote the reference load L-2 voltage as v_{l2}^* . Then the reference y_{2ref} is computed by the application of Kirchoff's voltage law as [see Fig. 6(b)]

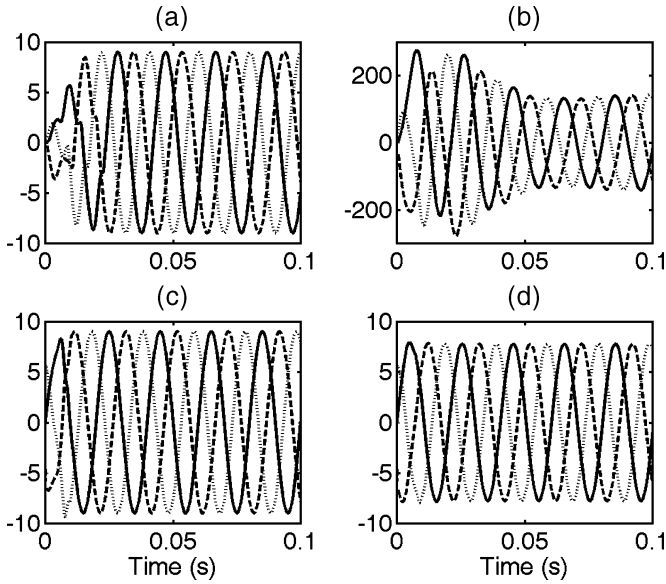
$$y_{2ref} = v_{l2}^* - v_{t2}. \quad (6)$$

We shall now demonstrate the normal operation of the IUPQC through simulation using PSCAD/EMTDC. The IUPQC parameters chosen are listed in Table II and the system parameters are given in Table I. The peak of the reference voltage y_{1ref} is chosen as 9.0 kV and its angle is computed from the angle controller (3) with $K_P = -0.25$. The reference voltage v_{l2}^* is chosen as a sinusoidal waveform with a peak of 9.0 kV and a phase angle of -10° . The simulation results are shown in Figs. 7 and 8.

It is assumed that the dc capacitor is initially uncharged and both the feeders along with the IUPQC are connected at time

TABLE II
 IUPQC PARAMETERS

System quantity	Parameters
System frequency	50 Hz
VSC-1 single-phase transformers	1 MVA, 3/11 kV, 10% leakage reactance
VSC-2 single-phase transformers	1 MVA, 3/11 kV, 10% leakage reactance
Losses	$R_{f1} = 6.0 \Omega$ $R_{f2} = 1.0 \Omega$
Leakage reactance	$2\pi fL_{f1} = 12.1 \Omega$ $2\pi fL_{f2} = 12.1 \Omega$
Filter capacitor (C_f)	50 μF
Filter capacitor (C_k)	30 μF
DC capacitor (C_{dc})	3,000 μF
V_{dcref}	6.5 kV


 Fig. 7. System performance with an IUPQC. (a) B-1 bus voltages (v_{t1}), kV. (b) Feeder-1 currents (i_{s1}), A. (c) L-2 load voltages (v_{l2}), kV. (d) B-2 bus voltages (v_{t2}), kV.

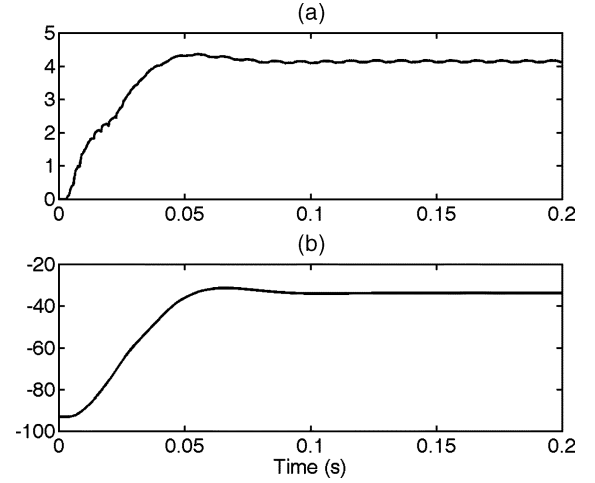
zero. It can be seen from Fig. 7(a), that the three-phase B-1 voltages, v_{t1} are perfectly balanced with a peak of 9 kV. Once these voltages become balanced, the currents drawn by Feeder-1, i_{s1} , also become balanced. The load L-2 bus voltages, v_{l2} shown in Fig. 7(c) are also perfectly sinusoidal with the desired peak of (9 kV) as the converter VSC-2 injects the required voltages in the system. The bus B-2 voltages, v_{t2} , can be seen to have a much smaller magnitude (about 7.75 kV peak). The dc capacitor voltage V_{dc} is shown in Fig. 8(a). It can be observed that it has a settling time of about 4 cycles (0.08 s) and it attains a steady-state value of about 4.17 kV. The phase angle δ_1 shown in Fig. 8(b) settles at -33.88° .

V. TRANSIENT PERFORMANCE OF IUPQC

Now, the performance of IUPQC has been evaluated considering various disturbance conditions. We shall also discuss and evaluate the limits of performance.

A. Voltage Sag in Feeder-1

With the system operating in the steady state, a 5 cycle (100 ms) voltage sag occurs at 0.14 s in which peak of the supply


 Fig. 8. (a) DC capacitor voltage (V_{dc}), kV, and (b) phase angle of B-1 bus voltage (δ_1), deg.

voltage, v_{s1} reduces to 6.5 kV from their nominal value of 9 kV. The various waveforms of only one phase (phase-a) are shown in Fig. 9. The trends in the other two phases are similar. It can be seen that the dc capacitor voltage, V_{dc} drops as soon as the sag occurs. If the bus voltage remains constant, the load power also remains constant. However, since the source voltage v_{s1} has dropped, the power coming out of the source has reduced. In order to supply the balance power requirement of the load, the V_{dc} drops. To offset this, the angle δ_1 retards such that the power supplied by the source increases. As the sag is removed, both the voltage V_{dc} and phase angle δ_1 returns to their steady state values. The current through Feeder-1 is also shown in Fig. 9. It can be seen that in order to supply the same load power at a reduced source voltage, the feeder current increases. Also, the transients in this current occur at the inception and the removal of the sag due to the change in the source voltage.

It has been observed that bus B-1 voltage v_{t1} starts getting distorted when the voltage sag causes the peak of the source voltage v_{s1} to drop below 6.0 kV. Also, for deeper voltage sags, the peak of v_{t1} reduces and the VSC-1 is not able to hold the bus voltage. The next sub-section explains the cause for this.

B. Performance Limits

Refer to Fig. 4 where let us assume the following phasor voltages

$$V_{s1} = V_1 \angle 0^\circ \text{ and } V_{t1} = V_2 \angle \delta_1. \quad (7)$$

Then the current flowing through Feeder-1 is

$$I_{s1} = \frac{V_1 - V_2 \angle \delta_1}{R_{s1} + jX_{s1}} \quad (8)$$

where $X_{s1} = \omega L_{s1}$, ω being the system fundamental frequency in rad/s. Therefore, the per phase real power entering bus B-1 is given by

$$\begin{aligned} P_{t1} &= \text{Re} \{ V_{t1}^* I_{s1} \} = \text{Re} \left\{ V_2 \angle -\delta_1 \left(\frac{V_1 - V_2 \angle \delta_1}{R_{s1} + jX_{s1}} \right) \right\} \\ &= \frac{1}{R_{s1}^2 + X_{s1}^2} [(V_1 V_2 \cos \delta_1 - V_2^2) R_{s1} \\ &\quad - V_1 V_2 X_{s1} \sin \delta_1]. \end{aligned} \quad (9)$$

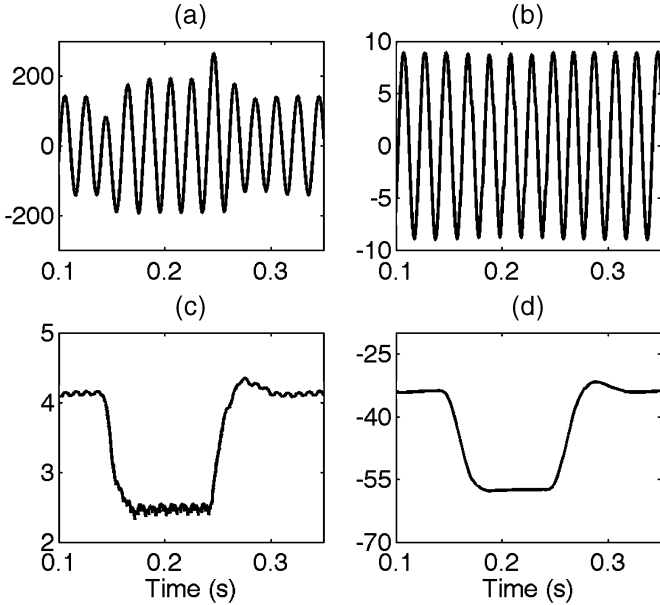


Fig. 9. System response during voltage sag in Feeder-1: (a) phase-a Feeder-1 current, A, (b) phase-a B-1 bus voltage, kV, (c) DC capacitor voltage (V_{dc}), kV, and (d) phase angle of B-1 bus voltage (δ_1), deg.

Solving for δ_1 from the above equation, we get

$$R_{s1} \cos \delta_1 - X_{s1} \sin \delta_1 = \frac{P_{t1} (R_{s1}^2 + X_{s1}^2) + V_2^2 R_{s1}}{V_1 V_2}. \quad (10)$$

Equation (10) forms the basis for the computation of the performance limit. Let us assume that both the VSCs are lossless (i.e., average power entering the bus B-1 is entirely consumed by the load L-1). It is additionally assumed that the power consumed by load L-2 is entirely supplied by the source v_{s2} . Then as V_2 (7) is held constant, the power consumed by the load, and hence P_{t1} , will remain constant. Therefore, the right hand side of (10) is a constant for a particular value of source voltage V_1 . Let us denote this constant as γ , that is

$$\gamma = \frac{P_{t1} (R_{s1}^2 + X_{s1}^2) + V_2^2 R_{s1}}{V_1 V_2}.$$

Also, let us define the feeder impedance as

$$Z_{s1} = R_{s1} + jX_{s1} = |Z_{s1}| \angle \phi_1 \text{ where } |Z_{s1}| = \sqrt{R_{s1}^2 + X_{s1}^2}$$

such that feeder resistance and reactance can be written as

$$R_{s1} = |Z_{s1}| \cos \phi_1 \text{ and } X_{s1} = |Z_{s1}| \sin \phi_1.$$

Therefore, δ_1 from (10) can be written as

$$\delta_1 = \cos^{-1} \left(\frac{\gamma}{|Z_{s1}|} \right) - \phi_1. \quad (11)$$

For the system data given in Tables I and II, the average three-phase real power drawn by the load L-1 for a line-to-line bus B-1 voltage of 11 kV, is 1.47 MW. Since the bus B-1 voltage is balanced, this power is supplied equally by all the three phases. Therefore, we choose P_{t1} as 0.49 MW. The values of δ_1 calculated from (11) and that obtained through simulation for different levels of voltage sag in v_{s1} are listed in Table III. From this table, it can be observed that there is a small discrepancy

TABLE III
VARIATION IN VOLTAGE ANGLE WITH SAG

Peak of v_{s1} = $\sqrt{2}V_1$ (kV)	Value of δ_1 (deg)	
	Calculated from (11)	Obtained from simulation
9.0	-28.22	-33.88
8.5	-30.77	-36.92
8.0	-33.88	-40.72
7.5	-37.60	-45.70
7.0	-42.20	-52.81
6.5	-48.18	-57.36
6.0	-56.76	-61.22
5.75	-63.27	-
5.5	-77.25	-

between the calculated and simulated values of δ_1 . This discrepancy increases as the amount of sag increases. The derivation of (11) assumes that the VSCs are lossless. In practice, however, the losses in VSC-1 and VSC-2 are drawn from the ac system by the angle controller (3). This implies that an additional amount of real power is entering bus B-1 and hence P_{t1} is equal to power supplied to the load L-1 plus the losses in the VSCs.

In Table III, the simulation fails when the source voltage drops to 5.75 kV. The calculated value of δ_1 is -63.27° for this case and the ac system fails to provide the additional power required to replenish the VSC losses. As a consequence, the dc capacitor voltage collapses. It is to be noted that (11) will produce real solution so long as the following condition is satisfied:

$$\gamma \leq |Z_{s1}| \quad (12)$$

when γ is equal to $|Z_{s1}|$, δ_1 becomes equal to $-\phi_1$, which is -80.53° . Therefore, if the source voltage drops even to 5.49 kV, (12) gets violated.

This problem can be solved by either reducing the load L-1 or by reducing the reference magnitude of the bus B-1 voltage V_2 . In both of these cases, P_{t1} reduces, ensuring that (12) is satisfied. For example, if the load is made to be 80% of the nominal value, then the angle δ_1 , calculated from (11), is -60.19° for peak of v_{s1} being 5.0 kV. Fig. 10 shows the simulation results when y_{1ref} , the peak of the reference bus B-1 voltage is assumed as 7.0 kV and the peak of source voltage v_{s1} is 5.75 kV. It can be seen that the dc link voltage V_{dc} charges to about 2.9 kV while angle δ_1 settles to about -50° . The B-1 bus voltage v_{t1} , however, is balanced and sinusoidal with a peak of 7.0 kV. We shall now use this knowledge for the protection of the sensitive load L-2.

C. Voltage Sag in Feeder-2

With the system operating in the steady state, Feeder-2 is subjected to a voltage sag at 0.14 s in which the peak of all three phases of the supply voltage v_{s2} reduces to 3.0 kV from their nominal value of 9.0 kV. The sag lasts for 5 cycles (100 ms). The system response is shown in Figs. 11 and 12. The bus B-2 voltage v_{t2} , the dc link voltage V_{dc} , and the angle δ_1 are shown in Fig. 11. It can be seen that V_{dc} drops to around 2.3 kV during the sag while δ_1 retards to about -60° . The bus B-1 voltage and load L-2 voltage are shown in Fig. 12 at the occurrence of the sag (a and c, respectively) and at the removal of the sag (b and d, respectively). It can be seen that as the dc link voltage falls and the angle retards, some minor distortions occur in the bus B-1

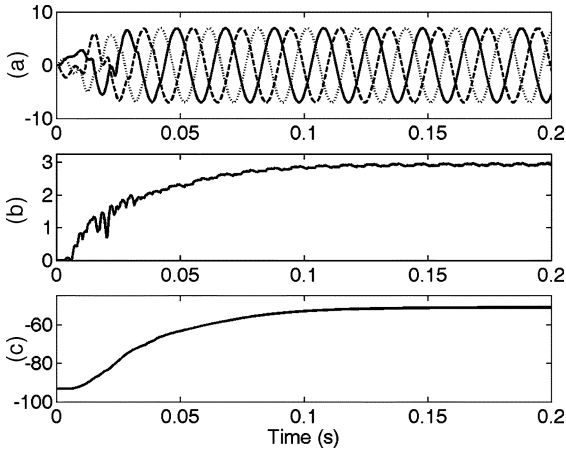


Fig. 10. System response when a peak of v_{s1} is 5.75 kV and that of bus B-1 reference voltage is 7.0 kV. (a) B-1 bus voltages (v_{t1}), kV. (b) DC capacitor voltage (V_{dc}), kV. (c) Phase angle of B-1 bus voltage (δ_1), deg.

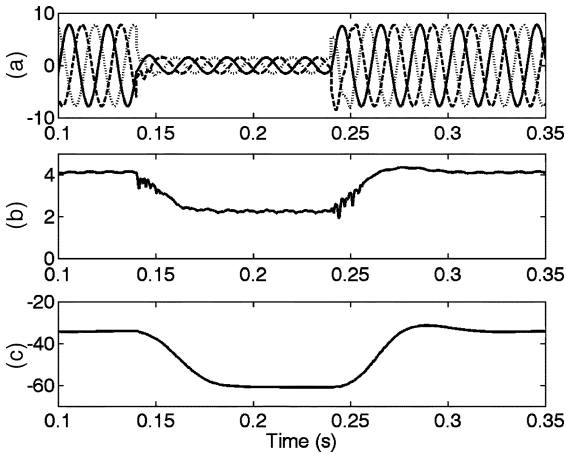


Fig. 11. (a) B-2 bus voltages (v_{t2}), kV (b) DC capacitor voltage (V_{dc}), kV, and (c) phase angle of B-1 bus voltage (δ_1), deg.

voltage. From the 7th row of Table III it can be seen that when the peak of source voltage v_{s1} drops to 6.0 kV, the phase angle δ_1 retards to -61.22° (as per simulation). This case (Figs. 11 and 12) is similar as the phase angle almost reaches the limiting value. The load L-2 voltage remains balanced and sinusoidal barring some glitches at the inception and removal of the sag. However, the dc capacitor will collapse if the peak of the voltage v_{s2} falls below 3.0 kV.

Thus, the IUPQC performs satisfactorily for a voltage sag of about 0.6 p.u. (9 kV to 5.5 kV) for Feeder-1 and 0.33 p.u. (9 kV to 3 kV) for Feeder-2. It should be noted that a 5 cycle (100 ms) voltage sag has been considered here. However, the IUPQC performs satisfactorily even for permanent voltage sags, as the dc capacitor voltage level is enough to supply both the VSCs. According to IEEE standard 1159, the system average rms (variation) frequency index (SARFI) is 27.5 for an rms voltage threshold of 0.9 p.u. while it is only 4.8 for an rms voltage threshold of 0.5 p.u. [13]. Also, 80–90% of the voltage sag events are between 0.6 to 0.9 p.u. Hence, the performance of IUPQC discussed in the paper addresses a large majority of voltage sags.

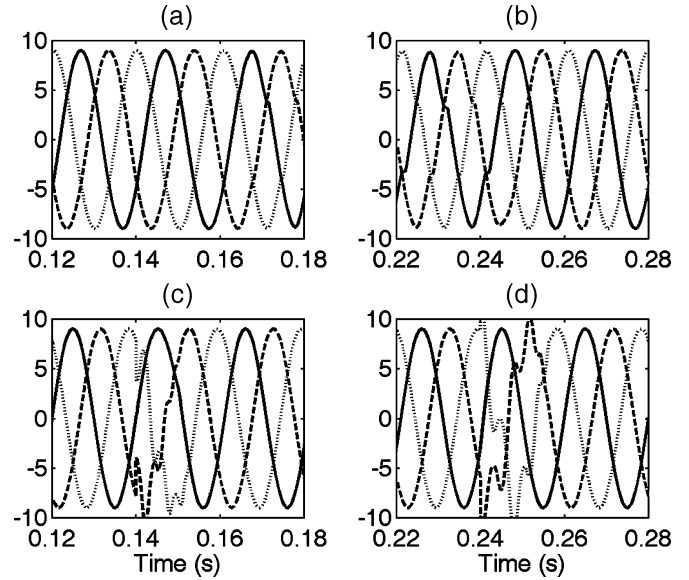


Fig. 12. B-1 and B-2 bus voltages at the inception of the voltage sag (a & c) and during sag removal (b & d) in kilovolts.

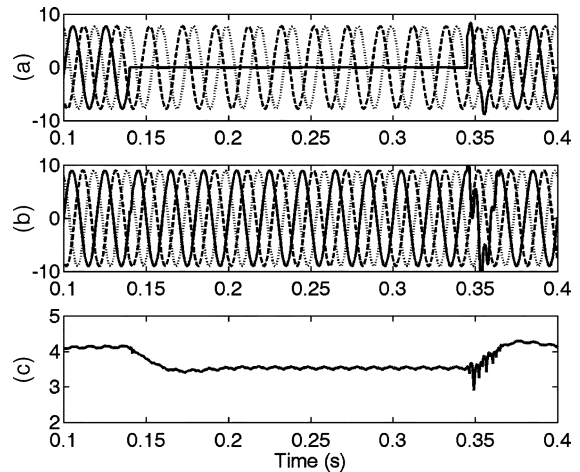


Fig. 13. System response during L-G fault at bus B-2: (a) B-2 bus voltages (v_{t2}), kV, (b) L-2 load voltages (v_{l2}), kV, and (c) DC capacitor voltage (V_{dc}), kV.

D. Upstream Fault in Feeder-2

The performance of the IUPQC is tested when a fault (L-G, L-L-G, and three-phase to ground) occurs in Feeder-2 at bus B-2. The system response is shown in Fig. 13 when a 10 cycle L-G fault occurs at 0.14 s such that the a-phase of B-2 bus voltage becomes zero. When the fault occurs, the power fed to load L-2 by Feeder-2 is reduced. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage to drop from 4.1 kV to 3.5 kV and δ_1 to change from -34° to -42° . It can be seen from Fig. 13(b), that the L-2 load voltages remain balanced throughout the fault period.

The system response is shown in Fig. 14 when a 10 cycle L-L-G fault occurs at 0.14 s such that both the a and b-phases of B-2 bus voltage become zero. B-2 bus voltages are shown in Fig. 14(a). It can be seen from Fig. 14(b), that the L-2 load voltages remain balanced. However, the dc capacitor voltage

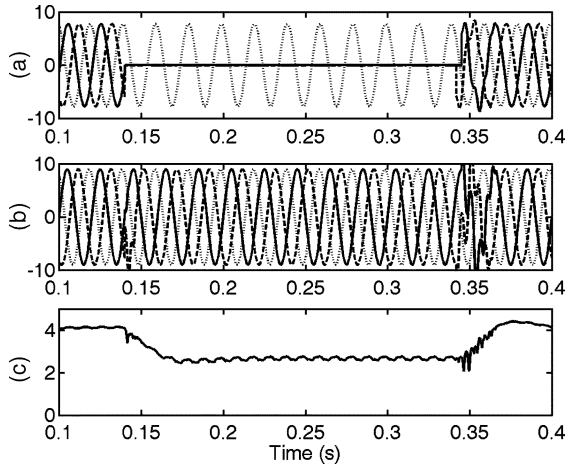


Fig. 14. System response during L-L-G fault at bus B-2 (a) B-2 bus voltages (v_{t2}), kV, (b) L-2 load voltages (v_{l2}), kV, and (c) DC capacitor voltage (V_{dc}), kV.

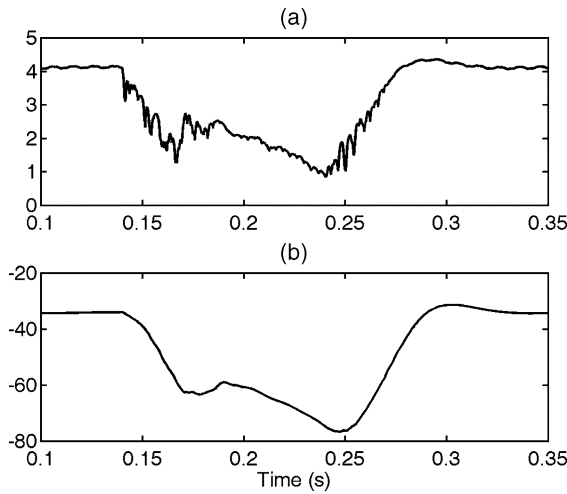


Fig. 15. (a) DC capacitor voltage (V_{dc}), kV, and (b) phase angle of B-1 bus voltage (δ_1) in deg. for a fault at B-2.

now drops to about 2.65 kV and δ_1 from -34° to -55° . Still it is enough to regulate both the load voltages.

Now, the system performance has been tested when a three-phase fault occurs at 0.14 s in Feeder-2 at bus B-2 such that the voltage v_{t2} becomes zero. The system response is shown in Figs. 15 and 16 where the fault is assumed to last 5 cycles only. When the fault occurs, the power fed to load L-2 by Feeder-2 becomes zero. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage V_{dc} to drop and, to offset the voltage drop, the angle δ_1 retards. As a result, power is drawn from the source v_{s1} through Feeder-1 and supplied to both the loads L-1 and L-2. These two quantities regain their nominal steady state values once the fault is cleared. This is evident from Fig. 15.

The bus B-1 voltage v_{t1} and the load L-2 voltage v_{l2} are shown in Fig. 16. It can be seen that barring transients at the beginning and at the end of the fault, the voltage v_{l2} across the sensitive load remains balanced and sinusoidal. However, since the angle δ_1 drops below -75° , the bus B-1 voltage gets distorted and its magnitude also reduces. These voltages, however,

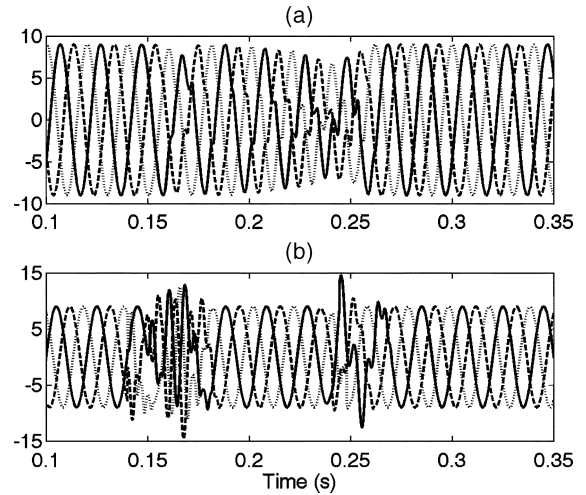


Fig. 16. (a) B-1 bus voltages (v_{t1}), kV and (b) L-2 load voltages (v_{l2}) in kV for a fault at bus B-2.

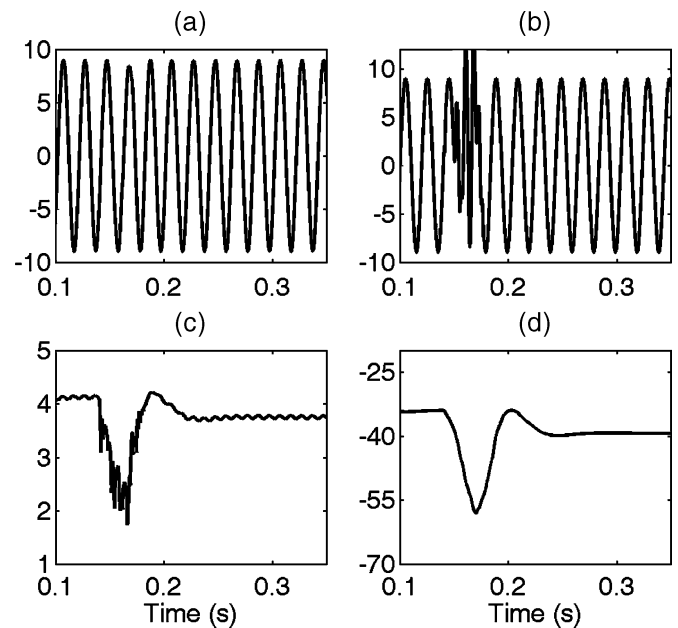


Fig. 17. System response when load L-12 is removed after fault: (a) phase-a B-1 bus voltage, kV, (b) phase-a L-2 load voltage, kV, (c) DC capacitor voltage (V_{dc}), kV, and (d) phase angle of B-1 bus voltage (δ_1), deg.

regain their nominal values within a cycle of the removal of the fault.

If the fault persists for a longer duration, the dc link voltage will continue to drop. This will gradually make the voltage tracking by either of the two VSCs impossible and both the bus B-1 and load L-2 voltages will collapse eventually. In order to avoid this, the load L-1 has to be reduced. To test this, the nonlinear load L-12 is cut off at 0.15 s when the fault occurs at 0.14 s. This implies that a duration of 0.01 s is needed for the detection of the fault. The simulation results with load removal are shown in Fig. 17.

In Fig. 17, only the voltage of phase-a of bus B-1 and load L-2 are shown. The trends in the other two phases are similar. It is assumed that the fault is of permanent nature and source v_{s2} is isolated from the fault by a circuit breaker. This implies that the voltage v_{t2} remains zero till Feeder-2 is reenergized after repair

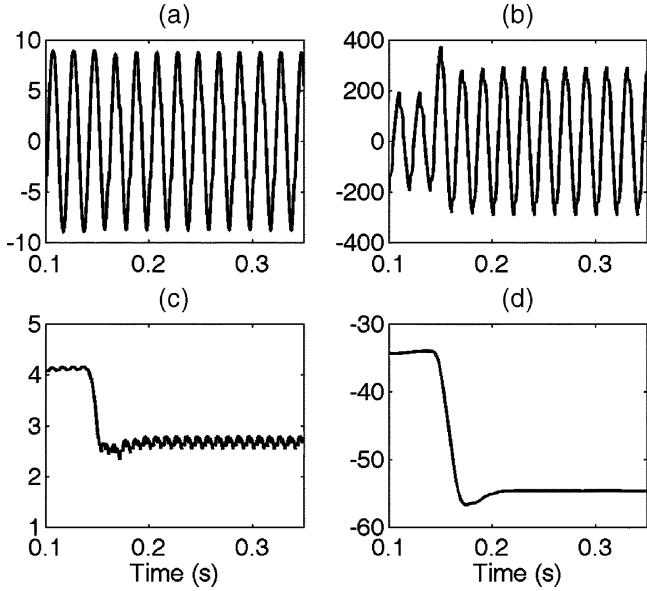


Fig. 18. System response during the change in load L-11: (a) phase-a B-1 bus voltage, kV, (b) phase-a L-1 load current, A, (c) DC capacitor voltage (V_{dc}), kV, and (d) phase angle of B-1 bus voltage (δ_1), deg.

work. It can be seen that as soon as the fault occurs, both the dc link voltage V_{dc} and the phase angle δ_1 of B-1 bus voltage drop and, as a result, the bus B-1 voltage starts getting distorted. However, as soon as the load L-12 is cut off from the system at 0.15 s, all these quantities return to their nominal values within about three cycles.

E. Load Change

Finally to test the system behavior during a load change, the unbalanced RL load L-11 is doubled by reducing its unbalanced impedances to half at 0.14 s. The nonlinear load L-12, however, has been kept unchanged. The system response is shown in Fig. 18. It can be seen that as the load increases, both the dc link voltage V_{dc} and angle δ_1 reduce and attain a new steady state. However, the bus B-1 voltage remains undisturbed. The phase-a load current is also shown in Fig. 18. It can be seen that it increases by about 50% after the load change.

VI. CONCLUSIONS

The paper illustrates the operation and control of an interline unified power quality conditioner (IUPQC). The device is connected between two feeders coming from different substations. An unbalanced and non-linear load L-1 is supplied by Feeder-1 while a sensitive load L-2 is supplied through Feeder-2. The main aim of the IUPQC is to regulate the voltage at the terminals of Feeder-1 and to protect the sensitive load from disturbances occurring upstream. The performance of the IUPQC has been evaluated under various disturbance conditions such as voltage sag in either feeder, fault in one of the feeders and load change. It has been shown that in case of a voltage sag, the phase angle of the bus voltage in which the shunt VSC is connected plays an important role as it gives the measure of the real power required by the load. The IUPQC can mitigate a voltage sag of about 0.6 p.u. (9 kV to 5.5 kV) in Feeder-1 and 0.33 p.u. (i.e., 9 kV to 3 kV) in Feeder-2 for long duration. The IUPQC dis-

cussed in the paper is capable of handling system in which the loads are unbalanced and distorted. Extensive case studies have been included to show that an IUPQC might be used as a versatile device for improving the power quality in an interconnected distribution system.

From above discussion, it has been observed that an IUPQC is able to protect the distribution system from various disturbances occurring either in Feeder-1 or in Feeder-2. As far as the common dc link voltage V_{dc} is at the reasonable level, the device works satisfactorily. The angle controller ensures that the real power is drawn from Feeder-1 to hold the dc link voltage constant. Therefore, even for a voltage sag or a fault in Feeder-2, VSC-1 passes real power through the dc capacitor onto VSC-2 to regulate the voltage v_{l2} . Finally when a fault occurs in Feeder-2 or Feeder-2 is lost, the power required by the Load L-2 is supplied through both the VSCs. This implies that the power semiconductor switches of the VSCs must be rated such that the total power transfer through them must be possible. This may increase the cost of this device. However, the benefit that may be obtained can offset the expense.

In the IUPQC configuration discussed in this paper, the sensitive load is fully protected against sag/swell and interruption. The sensitive load is usually a part of a process industry where interruptions result in severe economic loss [14]. Therefore, the cost of the series part of IUPQC must be balanced against cost of interruptions based on past reliability indices (e.g., CAIFI, CAIDI). It is expected that a part of IUPQC cost can be recovered in 5–10 years by charging higher tariff for the protected line. Furthermore, the regulated bus B-1 can supply several customers who are also protected against sag and swell. The remaining part of the IUPQC cost can be recovered by charging higher tariff to this class of customers. Such detailed analysis is required for each IUPQC installation.

In conclusion, the performance under some of the major concerns of both customer and utility e.g., harmonic contents in loads, unbalanced loads, supply voltage distortion, system disturbances such as voltage sag, swell and fault has been studied. The IUPQC has been shown to compensate for several of these events successfully.

APPENDIX A

POLE-SHIFT CONTROLLER DESIGN FOR VSC

The discrete-time input–output equation of the VSCs given in (2) and (5) can be written in a general form as

$$A(z^{-1})y(k) = B(z^{-1})u_c(k) + C(z^{-1})\eta(k). \quad (\text{A.1})$$

The aim of the pole-shift controller is to track a reference value that is denoted by y_{ref} . The control law is given by [1], [12]

$$u_c(k) = \frac{S(z^{-1})}{R(z^{-1})} \{y_{ref}(k) - y(k)\} \quad (\text{A.2})$$

where S and R are controller polynomials to be determined. From (A.1) and (A.2), the closed-loop system equation is then written as

$$y(k) = \frac{B(z^{-1})S(z^{-1})y_{ref}(k) + C(z^{-1})R(z^{-1})\eta(k)}{A(z^{-1})R(z^{-1}) + B(z^{-1})S(z^{-1})}. \quad (\text{A.3})$$

Let the closed-loop characteristic equation be defined by

$$T(z^{-1}) = A(z^{-1})R(z^{-1}) + B(z^{-1})S(z^{-1}). \quad (\text{A.4})$$

The closed-loop system poles are obtained by radially shifting the open-loop system poles toward the origin by a pole-shift factor $\lambda(0 < \lambda < 1)$, i.e.,

$$T(z^{-1}) = A(\lambda z^{-1}) = 1 + \lambda a_1 z^{-1} + \dots + \lambda^n a_n z^{-n}. \quad (\text{A.5})$$

The closer λ is to one, the smaller will be the control action. The controller parameters are obtained from the solution of the Aryabhata identity (A.4) and the control input $u_c(k)$ is obtained from (A.2). The switching action u is then obtained as

$$u = \begin{cases} +n & \text{for } u_c > h \\ -n & \text{for } u_c \leq -h \end{cases} \quad (\text{A.6})$$

where $2h$ is a hysteresis band and n is the turns ratio of the connecting transformer.

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