Intermodulation Distortion in Current-Commutating CMOS Mixers

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Abstract—The nonlinearity behavior of CMOS current-switching mixers is investigated. By treating the mixer as a periodically-time-varying weakly nonlinear circuit, we study the distortion-causing mechanisms and we predict the mixer distortion performance. Normalized graphs are provided from which the designer can readily estimate the mixer nonlinearity for particular process and design parameters. A simple CMOS transistor model appropriate for our calculations, which also takes into account deviation from the square law is adopted. The significance of a physical transistor model for reliable distortion simulation is demonstrated. The prediction of our analysis is compared with simulation results and with experimental data.

Index Terms—Active mixers, analog integrated circuits, CMOS analog integrated circuits, CMOS mixers, distortion, frequency conversion, Gilbert cell, intermodulation distortion, mixers, nonlinear distortion.

I. INTRODUCTION

IXERS ARE widely used in modern communication systems in order to realize frequency translation of the carrier signals. Intermodulation distortion in the mixer greatly affects the dynamic range of most communication systems. Since mixers are not linear-time-invariant circuits, one cannot apply classical distortion analysis techniques using power series at low frequencies and Volterra series at high frequencies [1], [2], appropriate for linear amplifiers. Designers usually lack a complete understanding of the distortion-generating mechanisms, and design optimization usually relies on simulation using transient analysis, which is time consuming and, depending on the transistor model used, often unreliable, as will become apparent below.

Active mixers which employ a switching transistor pair for current commutation, such as the Gilbert cell, are frequently used [3]–[7], because they offer advantages such as high conversion gain and high port-to-port isolation. Their principle of operation is technology independent and they can be realized in bipolar or CMOS processes. A transconductance stage is used to transform the input voltage signal to current, which is then commutated with the switching pair. Modern sub-micron CMOS technologies are increasingly used in the design of integrated communication systems because they have low fabrication cost and are appropriate for a high level of integration, while realizing good high-frequency performance. The CMOS Gilbert

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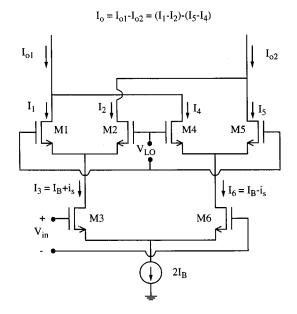


Fig. 1. A CMOS Gilbert cell.

cell is shown in Fig. 1 and the active single-balanced mixer is shown in Fig. 2. A brief description of their operation can be found in [8]. The Gilbert cell, being a double-balanced structure, has the advantage of rejecting the strong local oscillator (LO) component and the even-order distortion products. Compared with passive CMOS mixers, active CMOS mixers offer conversion gain and provide in general a better system noise performance, while their linearity is generally significantly worse.

The CMOS transistors used in the transconductance stage of active mixers demonstrate fairly good linearity and are used often with little or no degeneration, in contrast with the bipolar transconductance stages which often require significant degeneration. The transconductance stage linearity can be analyzed with classical techniques [1], [2], [9]. However, little has been published on the distortion characteristics of the CMOS switching pair. Its nonlinearity imposes problems, particularly when together with high linearity, high gain is required from the mixer, since then the signal at the output of the transconductance stage is large. While the exponential I-V characteristics of the bipolar transistor make the bipolar transistor switching pair arbitrarily linear at low frequency if the device base resistance is low [10], [11], this is not true for the CMOS switching pair, which demonstrates significant nonlinearity even at low frequencies.

The analysis of the switching pair presented here aims to illuminate the distortion mechanisms and to provide intuition and the means for fast performance estimation. The switching

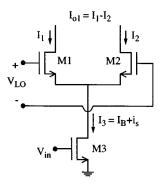


Fig. 2. A single-balanced active CMOS mixer.

pair is treated as a weakly nonlinear periodically time-varying circuit and time-varying power series are employed in the analysis. It will be shown that if the capacitive effects are negligible, in the frequency band of interest the distortion behavior of the switching pair can be described by a time-invariant power series which can be cascaded with the power series of the transconductance stage to calculate the total distortion. The methodology also applies to high frequencies, where time-varying Volterra series replace the time-varying power series. Similar approaches have been used in [12] and [13] for the distortion of diode mixers, and in [14] for the distortion of passive MESFET mixers. Our analysis also identifies the characteristics of a transistor model for a reliable mixer distortion simulation.

A distortion study of a bipolar switching pair has been presented in [10] and [11], but the method used was different from the one employed here. The behavior of the bipolar switching pair was found to depend on only a few normalized variables, and transient simulation was used to find their effect on the distortion. Using the methods described here for fast evaluation of the CMOS switching pair distortion, we also provide normalized graphs from which one can predict the intermodulation for any given technology and operating conditions.

II. TRANSISTOR MODEL

The transistors of the CMOS switching pair operate in weak, moderate, and strong inversion. It will become apparent below that a model which ignores the subthreshold region, or uses different equations to describe the different modes of operation, is inappropriate for a distortion analysis of the switching pair. A model which describes all three regions with a single analytical expression and therefore has continuous derivatives of any order is needed. Furthermore, it must be simple enough for analytical calculations.

Continuous MOS transistor models have been presented in [15] and [16]. We will use the same kind of smooth interpolation between the regions of operation. We will take into account to a first order the deviation from the square law in strong inversion while we will neglect second-order phenomena such as channel-length modulation, which complicate the transistor model. As a result of the latter assumption, we will neglect the distortion introduced by the output impedance of the devices, assuming that a linear load dominates the mixer output. The drain current

I as a function of the gate-source voltage V_{GS} is modeled in this paper by

$$I = f(V_{GS} - V_T) = K \frac{X^2}{1 + \theta X}$$
 (1)

where

$$X = 2\eta \phi_t \ln(1 + e^{(V_{GS} - V_T)/(2\eta \phi_t)}). \tag{2}$$

Above, V_T is the threshold voltage, ϕ_t is the thermal voltage kT/q, and K is a constant depending on the technology and the transistor dimensions, proportional to the transistor width. Parameter θ approximately models source series resistance, mobility degradation because of the vertical field, and short-channel effects such as velocity saturation [17]. For a minimum-length device of an existing $0.8-\mu m$ technology, it was estimated to be 0.9 V^{-1} , and for a different 0.25- μm technology, it was found to be approximately 2.5 V^{-1} . It is a function of the channel length and is independent of the body effect. Parameter η determines the rate of exponential increase of the drain current with the gate-source voltage in the subthreshold region, and also the size of the moderate inversion region. It takes values approximately between 1 and 2 and it decreases (approaching 1) because of the body effect when the source-body voltage increases, while it tends to be higher when short-channel phenomena are present. It is shown in [15] to depend slightly on V_{GS} , but for simplicity η will be considered here a constant for a given channel length. The parameter corresponding to our parameter X is referred to in the BSIM3 Version 3 Manual [16] as the effective $V_{GS} - V_T$ voltage. Using this model, the analysis presented in [8] can also be performed while taking into account the effect of weak and moderate inversion.

This model reduces to known expressions in strong and weak inversion. In strong inversion where the exponential term dominates the argument of the logarithm in (2), $X = V_{GS} - V_T$, and (1) becomes

$$I = K \frac{(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)}$$
 (3)

the common I-V relation in saturation. In weak inversion, using the approximation $\ln(1+z)\approx z$ for small z, we obtain

$$X = 2\eta \phi_t e^{(V_{GS} - V_T)/(2\eta \phi_t)} \tag{4}$$

and since X is small, 1 dominates in the denominator of (1), and it provides

$$I = K(2\eta\phi_t)^2 e^{(V_{GS} - V_T)/(\eta\phi_t)}$$
(5)

which is the exponential $I{-}V$ relation of the transistor in weak inversion. In moderate inversion equations (1) and (2) provide a smooth monotonic increase, interpolating between (3) and (5). However, the proportionality constant of (5) is probably inaccurate and the value of parameter $\eta\phi_t$ that provides the correct exponential increase in weak inversion does not necessarily provide accurate moderate-inversion modeling. For distortion prediction of the switching pair the moderate-inversion region is more significant than the subthreshold and it is preferable to consider an η value that better models the moderate inversion.

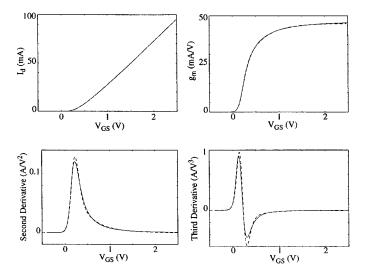


Fig. 3. I-V curve and first three derivatives for a quarter-micron CMOS technology. The solid line is the simple model and the dashed line is obtained from the BSIM3 version 3 model.

Nevertheless, it will be shown that the value of η has only a minor effect on the distortion prediction.

The I-V transistor curve in saturation and its first three derivatives with respect to V_{GS} obtained from this simple model were compared with the corresponding curves obtained from the SPICE models BSIM3 version 3 and version 2, in Figs. 3 and 4, respectively. The two SPICE models describe different technologies of channel length 0.25 μ m and 0.8 μ m, respectively. The parameters of the simple model were curve fitted to the I-V curves obtained from SPICE. The derivatives of the simple model were derived analytically (see Appendix), while those of the SPICE models were calculated numerically. As numerical noise imposes problems in the evaluation of the second and third derivative with successive differences, a more sophisticated method was used. For every value of V_{GS} , a polynomial was fitted to a number of points around this value and then the derivatives of the polynomial were taken analytically [18].

As can be seen in Fig. 3, model BSIM3 version 3 provides smooth derivatives, as one would expect from a physical model, and the simple model is in close agreement with it. In Fig. 4 we observe that the I-V curve and the first derivative generated with the BSIM3 version 2 model coincide with those of the simple model. However, the use of a different equation for the weak, moderate, and strong inversion in the BSIM3 version 2 model becomes apparent in the second and third derivatives, where discontinuities appear at the transitions. We will see below the effect of these discontinuities on the distortion simulation of the switching pair.

III. SWITCHING PAIR DISTORTION AT LOW FREQUENCIES

A. Low-Frequency Large-Signal Equations

Consider the single-balanced mixer of Fig. 2. The operating point of the transistors of the switching pair varies periodically with time. In the following analysis we need to be able to find

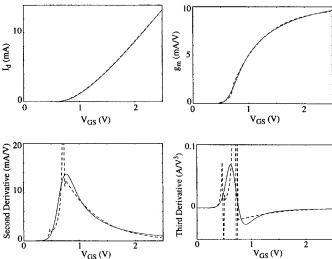


Fig. 4. I-V curve and first three derivatives for a $0.8-\mu\,\mathrm{m}$ CMOS technology. The solid line is the simple model and the dashed line is obtained from the BSIM3 version 2 model.

this operating point for a given bias current I_B and instantaneous LO voltage $V_{\rm LO}(t)$. The output conductance of the devices is neglected and the load at the drains of M1 and M2 is assumed such that they remain in saturation during the whole LO period. This assumption is usually satisfied since if the transistors of the switching pair enter the triode region, the commonsource node becomes a high impedance point and performance is degraded because of reactive effects. If $I = f(V_{GS} - V_T)$ is the I-V relation of a transistor as given by (1) and (2), the large-signal behavior of the switching pair is described by the following:

$$f(V_1) + f(V_2) = I_B$$
 (6)

$$V_1 - V_2 = V_{LO}$$
 (7)

where $V_1 = V_{GS1} - V_T$, $V_2 = V_{GS2} - V_T$, and V_{GS1} and V_{GS2} are the gate-source voltages of M1 and M2, respectively. Substituting V_2 from (7) to (6), we obtain one nonlinear equation with V_1 as an unknown which can be solved rapidly with an iterative numerical method.

From (7) and (6) we observe that the drain current of each transistor does not depend on V_T , and therefore to the extent of validity of the transistor model used here, the behavior of the switching pair is independent of the body effect and the common-mode LO voltage. The same conclusion was reached in [8], but without taking into account the subthreshold region of operation.

B. Distortion Calculations

At low frequencies the switching pair is a memoryless system. Neglecting the output resistance of the transconductance stage, the output current, defined as the difference of the drain currents of M1 and M2, is a function of the instantaneous values of the output current of the transconductance stage and the LO voltage:

$$I_{o1} + i_{o1} = F(V_{LO}(t), I_B + i_s)$$
 (8)

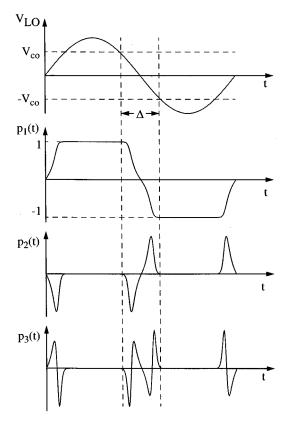


Fig. 5. Typical shape of waveforms $p_1(t)$, $p_2(t)$, and $p_3(t)$.

where I_{o1} , I_{B} denote values without input signal present, and i_{o1} , i_{s} denote incremental values. Since i_{s} is small, a third-order Taylor expansion provides

$$i_{o1} = \frac{dF}{dI_B} \cdot i_s + \frac{1}{2} \frac{d^2F}{dI_B^2} \cdot i_s^2 + \frac{1}{6} \frac{d^3F}{dI_B^3} \cdot i_s^3$$
 (9)

or

$$i_{o1} = p_1(t) \cdot i_s + p_2(t) \cdot i_s^2 + p_3(t) \cdot i_s^3$$
 (10)

where $p_1(t)$, $p_2(t)$, $p_3(t)$ are periodic waveforms of which a typical shape is shown in Fig. 5. The value of these waveforms is easily determined when one of the transistors is off. For example, when M2 is off $p_1(t)=1$ and $p_2(t)=p_3(t)=0$. When instantaneously $V_{\rm LO}(t)=0$, $i_{o1}=0$, and $p_1(t)=p_2(t)=p_3(t)=0$, because of symmetry. When the conductance of both M1 and M2 is significant, $p_1(t)$, $p_2(t)$, and $p_3(t)$ depend on the bias current I_B , the LO voltage $V_{\rm LO}$, and the device characteristics.

With some manipulation, waveforms $p_1(t)$, $p_2(t)$, and $p_3(t)$ can be expressed in terms of the derivatives of the I-V function f with respect to V_{GS} as follows:

$$p_1(t) = \frac{f_{1V} - f_{2V}}{f_{1V} + f_{2V}} \tag{11}$$

$$p_2(t) = \frac{f_{2V} f_{1VV} - f_{1V} f_{2VV}}{(f_{1V} + f_{2V})^3}$$
(12)

$$p_{3}(t) = \frac{(f_{1}VV + f_{2}VV)(f_{1}Vf_{2}VV - f_{2}Vf_{1}VV)}{(f_{1}V + f_{2}V)^{5}} + \frac{f_{2}Vf_{1}VVV - f_{1}Vf_{2}VVV}{3(f_{1}V + f_{2}V)^{4}}.$$
 (13)

The derivatives of f are denoted with the symbol f followed by an index, whose first character (1 or 2) denotes the transistor (M1 or M2 respectively) and the number of V's following denotes the order of the derivative.

Without loss of generality, $p_1(t)$, $p_2(t)$, and $p_3(t)$ can be considered odd functions of time and can be expanded in a series of sinusoids. In this case (10) provides

$$i_{o1} = \sum_{k=1}^{\infty} \left[p_{1,k} \cdot i_s + p_{2,k} \cdot i_s^2 + p_{3,k} \cdot i_s^3 \right] \cdot \sin(2\pi k f_{\text{LO}} t) \quad (14)$$

where $p_{i,k}$ is the kth coefficient of the waveform $p_i(t)$ in the series, and $f_{\rm LO}$ is the LO frequency. The mixer is usually used for upconversion or downconversion by one LO multiple and in this case the distortion behavior of the switching pair in the frequency band of interest can be described by a time-invariant power series¹

$$i_{o1} = b_1 \cdot i_s + b_2 \cdot i_s^2 + b_3 \cdot i_s^3 \tag{15}$$

where

$$b_i = \frac{p_{i,1}}{2} = \frac{1}{T_{LO}} \int_0^{T_{LO}} p_i(t) \sin(2\pi f_{LO} t) dt$$
 (16)

and T_{LO} is the LO period. If i_s consists of two tones of equal magnitude I_s at two closely spaced frequencies f_1 and f_2

$$i_s = I_s \cos(2\pi f_1 t) + I_s \cos(2\pi f_2 t)$$
 (17)

and the generated third-order intermodulation is

$$IM_3 = \frac{3}{4} \frac{b_3}{b_1} I_s^2. \tag{18}$$

For high LO amplitude, $p_1(t)$ resembles a square waveform and b_1 approaches $2/\pi$. Assuming that the time interval Δ (see Fig. 5), during which $p_2(t)$ and $p_3(t)$ are nonzero, is small compared to the whole period and that during this time the LO voltage is a linear function of time with slope λ , it can be shown that the coefficients b_2 and b_3 decrease inversely proportional to the square of λ . Indeed, for b_3 for example, approximating the sinusoid with its argument, (16) provides

$$b_3 = \frac{4 \cdot 2\pi}{\lambda^2 T_{LO}^2} \int_0^{V_{co}} p_3(V_{LO}) V_{LO} \, dV_{LO}$$
 (19)

where V_{co} is some LO cutoff voltage above which the conduction of one of the two devices is insignificant and $p_3(t)$ is zero. Simulation with sinusoidal LO waveform of amplitude V_o shows that indeed intermodulation asymptotically reduces proportionally to $1/V_o^2$ for high values of V_o while it drops at a higher rate for moderate values of V_o . For the rest of the paper, the LO waveform will be considered sinusoidal and V_o will denote its amplitude.

Figs. 6 and 7 show the quantity $0.75(b_3/b_1)(1\ A)^2$ (in dB, calculated as $20\log_{10}(IM_3)$) versus bias current simulated with SpectreRF using the BSIM3 version 3 and BSIM3 version 2 model, respectively, and also as obtained from the simple model. This quantity corresponds to the intermodulation value for I_s

¹Equation (15) as well as (26) below are 'loose,' in the sense that the left and right side refer to the output and input frequency bands, respectively.

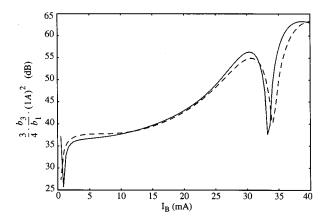


Fig. 6. Comparison of prediction (solid line) and simulation (dashed line) using the BSIM3 version 3 model, of the low-frequency intermodulation versus bias current for a switching pair of the 0.25 μ m technology and channel width 100 μ m. The LO amplitude is 1 V.

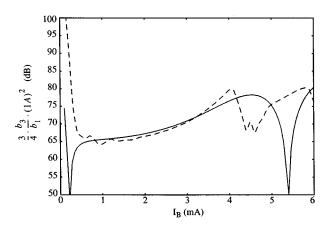


Fig. 7. Comparison of prediction (solid line) and simulation (dashed line) using the BSIM3 version 2 model, of the low-frequency intermodulation versus bias current for a switching pair of the 0.8 μ m technology and channel width 100 μ m. The LO amplitude is 1 V.

equal to 1A, assuming that the system remains weakly nonlinear. If for example I_s is 1 mA, one must subtract 120 dB from the value read from these figures. The transistor width was in both cases equal to 100 μ m and the LO amplitude was 1 V. The simulation result in Fig. 6 is a smooth curve, in very close agreement with the prediction of the simple model. However, the BSIM3 version 2 model used in Fig. 7 is inappropriate for distortion simulation of the switching pair, as the discontinuities in the second and third derivatives of the I-V curve observed in Fig. 4 create large errors. Very high numerical accuracy is needed to reduce discontinuities in the intermodulation curve versus bias current and obtain the curve of Fig. 7, and even then the result shows large discrepancies from the simple model prediction. As we shall see, the latter agrees well with measurements.

The intermodulation prediction is largely insensitive to the value of parameter $\eta\phi_t$. Fig. 8 shows predicted intermodulation as a function of bias for three different values of $\eta\phi_t$, 26, 38, and 50 mV, versus bias. Instead of bias current we express here bias in terms of V_x/V_o where V_x is the LO voltage value sufficient

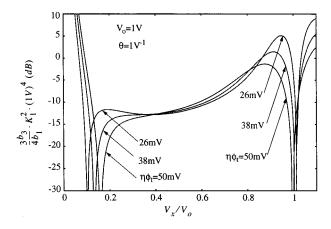


Fig. 8. Low-frequency intermodulation of a switching pair for different values of the parameter $\eta \phi_t$. The intermodulation value is almost insensitive to this parameter.

to completely switch off one of the two devices (neglecting the subthreshold conduction²), and has been found in [8] to be

$$V_x = \frac{I_B \theta}{2K_1} + \sqrt{\left(\frac{I_B \theta}{2K_1}\right)^2 + \frac{I_B}{K_1}}.$$
 (20)

The conversion gain of the switching pair has been found approximately equal to

$$b_1 \approx \frac{2}{\pi} \left(\frac{V_x/V_o}{\arcsin(V_x/V_o)} \right).$$
 (21)

In [8] the subthreshold conduction was neglected and parameter normalization was used to express the performance of the switching pair as a function of fewer independent parameters. For this purpose, all currents were multiplied with θ^2/K_1 and all voltages were multiplied with θ . Even though this normalization is not exact in the present analysis because the subthreshold region of operation is taken into account, we can conjecture that the intermodulation can be approximately expressed in terms of similarly normalized quantities. Evaluation of the intermodulation as described previously shows that indeed this is the case. Fig. 9 shows the value of the quantity $0.75(b_3/b_1)(K_1^2/\theta^4)$ versus V_x/V_o , for $\theta V_o = 1$ and for three different values of V_o . We observe that the three curves approximately coincide for moderate values of V_x/V_o which are most often used in practice, while they differ for very low and very high values of V_x/V_o . The agreement is better for higher LO amplitudes because these correspond to higher bias currents in this graph and the subthreshold region has a smaller effect. This observation allows us to give normalized intermodulation graphs.

In order to reduce the range of the intermodulation values and improve the readability of the normalized graphs we express intermodulation in terms of the quantity

$$\frac{3}{4} \frac{b_3}{b_1} \frac{K_1^2}{\theta^4} \frac{(V_o \theta)^4}{(1 + V_o \theta)^2}.$$
 (22)

The result is shown in Fig. 10 which was generated with $\eta \phi_t = 36$ mV and $V_o = 1$ V. The ratio b_3/b_1 can be calculated from this graph.

 $^2 \mbox{Voltage}~V_{co}$ is generally higher than V_x because of the subthreshold conduction.

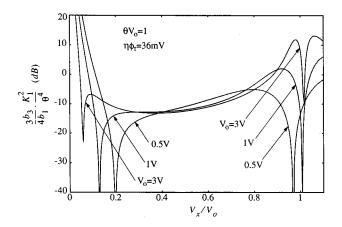


Fig. 9. Normalized intermodulation for a fixed value of θV_o but three different values of V_o : 0.5, 1, and 3 V.

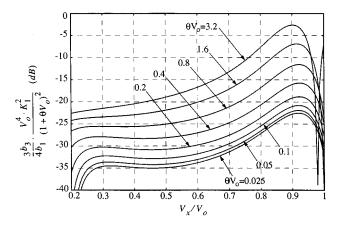


Fig. 10. Normalized intermodulation versus V_x/V_o .

C. Cascading the Driver Stage and the Switching Pair

Let us assume now that the nonlinearity of the transconductance stage is described by a power series as follows:

$$i_s = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 (23)$$

where v_{in} is the input voltage. Cascading the power series of the transconductance stage with that of the switching pair, the output current can be related to the input voltage with a new time-varying power series. Substituting (23) in (10) we obtain

$$i_{o1} = a_1 p_1(t) \cdot v_{in} + (a_2 p_1(t) + a_1^2 p_2(t)) \cdot v_{in}^2 + (a_3 p_1(t) + 2a_1 a_2 p_2(t) + a_1^3 p_3(t)) \cdot v_{in}^3.$$
 (24)

Using the expansion of $p_1(t)$, $p_2(t)$, and $p_3(t)$ in a series of sinusoids as in (14) we obtain

$$i_{o1} = \sum_{k=1}^{\infty} \left[a_1 p_{1,k} \cdot v_{in} + (a_2 p_{1,k} + a_1^2 p_{2,k}) \cdot v_{in}^2 + (a_3 p_{1,k} + 2a_1 a_2 p_{2,k} + a_1^3 p_{3,k}) \cdot v_{in}^3 \right] \cdot \sin(2\pi k f_1).$$
(25)

If frequency translation by one LO multiple is of interest, the distortion performance can be described by a time-invariant power series

$$i_{o1} = c_1 \cdot v_{in} + c_2 \cdot v_{in}^2 + c_3 \cdot v_{in}^3 + \cdots$$
 (26)

where

$$c_1 = a_1 b_1 \tag{27}$$

$$c_2 = a_2 b_1 + a_1^2 b_2 (28)$$

$$c_3 = a_3b_1 + 2a_1a_2b_2 + a_1^3b_3. (29)$$

Observe that these coefficients can be obtained directly by cascading the power series (23) and (15).

The total mixer third-order intermodulation is now given by

$$IM_3 = \frac{3}{4} \frac{c_3}{c_1} V_{in}^2 \approx \frac{3}{4} \left(\frac{a_3}{a_1} V_{in}^2 + \frac{b_3}{b_1} a_1^2 V_{in}^2 \right)$$
(30)

where in the last expression V_{in} is the amplitude of each input tone in the intermodulation test and the second term on the right side of (29) has been neglected as small. The total mixer intermodulation is approximately equal to the sum of the intermodulation values that the driver stage and the switching pair would generate if the other stage were ideal.

D. Distortion of Differential Versus Single-Ended Output

A differential output was considered above for the single-balanced mixer of Fig. 2 but it can be shown that if the LO waveform is symmetric around zero, the distortion behavior is exactly identical if the output is taken single-ended. Assume that if I_1 is taken as output, the mixer distortion performance is described by a time-varying power series

$$i_1 = q_1(t) \cdot v_{in} + q_2(t) \cdot v_{in}^2 + q_3(t) \cdot v_{in}^3 + \cdots$$
 (31)

and let us denote the Fourier coefficients of the waveform $q_k(t)$ by $q_{k,n}$. It is easy to see that if the LO waveform is symmetric, the relevant power series for I_2 is

$$i_2 = q_1 \left(t + \frac{T_{\text{LO}}}{2} \right) \cdot v_{in} + q_2 \left(t + \frac{T_{\text{LO}}}{2} \right)$$
$$\cdot v_{in}^2 + q_3 \left(t + \frac{T_{\text{LO}}}{2} \right) \cdot v_{in}^3 + \cdots$$
(32)

and that the Fourier coefficients of the waveform $q_k(t+(T/2))$ are $(-1)^nq_{k,n}$, where for frequency translation by one LO multiple n=1. The coefficients of the corresponding time-invariant power-series for differential output are twice these for single-ended output, and the generated distortion in the two cases is identical. A similar argument holds at high frequencies where Volterra series replace the power series. A similar approach shows that the distortion of the Gilbert cell is identical if single-ended or differential output is obtained. In fact for the Gilbert cell this statement can be shown true even if the LO waveform is not symmetric.

IV. HIGH FREQUENCIES

A. Numerical Calculations

Time-varying Volterra series can be used at high frequencies to analyze the high-frequency intermodulation performance of the switching pair. We will consider now the effect of the gate-source capacitors of the transistors M1 and M2, C_1 and C_2 , respectively, and the total capacitance from the common-source node to ground C_b consisting of the source-body capacitance

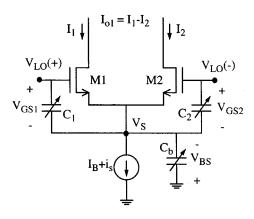


Fig. 11. Switching pair as considered in the high-frequency analysis.

of M1 and M2 and the drain-body capacitance of M3, as shown in Fig. 11. We will neglect the gate-drain capacitances and assume that the LO voltage is perfectly sinusoidal, generated by an ideal voltage source while the common LO voltage is a constant. Denoting again the I-V relation of a transistor with I=f(V), with no small signal present, the equation describing the switching pair at high frequencies is

$$I_B = f(V_1) + f(V_2) + \frac{d}{dt}Q_1 + \frac{d}{dt}Q_2 + \frac{d}{dt}Q_s$$
 (33)

where Q_1 , Q_2 , and Q_s are the charges of the capacitors C_1 , C_2 , and C_b , respectively, and $V_1 = V_{GS1} - V_T$, $V_2 = V_{GS2} - V_T$ have been defined before. The capacitances satisfy

$$C_1(V_1) = \frac{dQ_1}{dV_{CG1}}$$
 (34)

$$C_2(V_2) = \frac{dQ_2}{dV_{GS2}}$$
 (35)

$$C_b(V_{BS}) = \frac{dQ_s}{dV_{BS}} \tag{36}$$

where V_{BS} is the body–source voltage of M1 and M2. Capacitance C_b is the sum of an area and a sidewall junction capacitance and each of its components is given by an expression of the form

$$C_j = \frac{C_{jo}}{\left(1 - \frac{V_{BS}}{\phi_j}\right)^{m_j}} \tag{37}$$

where the symbols C_{jo} , ϕ_j , and m_j have the usual meaning. Capacitances C_1 and C_2 are dependent on the region of operation and will be approximated by

$$C_1(V_1) = Cgs_{ol} + \frac{Cgs_{\text{sat}} - Cgs_{ol}}{1 + \exp(-(V_1/\eta\phi_t))}$$
 (38)

which provides a smooth transition from the overlap capacitance in subthreshold Cgs_{ol} to the capacitance value in saturation $Cgs_{\rm sat}$. From (37) and (38), analytical expressions for the derivatives of the capacitances with respect to their voltage arguments can be obtained. From (33), (34)–(36), and expressing V_{GS1} , V_{GS2} , and V_{BS} in terms of $V_{\rm LO}(t)$ and the common

source potential V_S , we obtain

$$I_{B} = f(V_{1}) + f(V_{2}) + \frac{1}{2} (C_{1} - C_{2}) \frac{dV_{LO}}{dt} - (C_{1} + C_{2} + C_{b}) \frac{dV_{S}}{dt}.$$
 (39)

Substituting

$$V_1 = V_{\text{LO},c} + \frac{V_{\text{LO}}}{2} - V_S - V_T \tag{40}$$

$$V_2 = V_{\text{LO},c} - \frac{V_{\text{LO}}}{2} - V_S - V_T \tag{41}$$

where $V_{{\rm LO},c}$ is the common LO voltage considered constant, (39) becomes a nonlinear differential equation with periodic boundary conditions which must be solved to find the periodic steady-state operating point of the devices. This was accomplished by discretizing (39), and solving for the vector of the values of V_S over one period, using a Newton–Raphson method as described in [19]. A software package for sparse matrix manipulation [21] was employed. The body effect was neglected and the threshold voltage was considered a constant. We will adopt this approximation for the rest of the analysis, and will comment on the role of the body effect later.

When a small-signal current $i_s(t)$ is present at the transconductance stage output, voltages V_1, V_2 , and V_{BS} will change to V_1+v, V_2+v , and $V_{BS}+v$, respectively. Taking a third-order Taylor expansion of (33) and removing the large-signal part of the equation we obtain

$$i_s = Gv + G_v v^2 + G_{vv} v^3 + \frac{d}{dt} \left[Cv + C_v v^2 + C_{vv} v^3 \right]$$
(42)

where

$$G = f_{1V} + f_{2V} (43)$$

$$G_v = \frac{1}{2}(f_{1VV} + f_{2VV}) \tag{44}$$

$$G_{vv} = \frac{1}{6}(f_{1VVV} + f_{2VVV}) \tag{45}$$

$$C = C_1 + C_2 + C_b (46)$$

$$C_v = \frac{1}{2}(C_{1V} + C_{2V} + C_{bV}) \tag{47}$$

$$C_{vv} = \frac{1}{6}(C_{1VV} + C_{2VV} + C_{bVV}) \tag{48}$$

and C_{1V} , C_{1VV} , C_{2V} , C_{2VV} , C_{bV} , and C_{bVV} denote the first and second derivatives of the capacitances C_1 , C_2 , and C_b , with respect to their voltage arguments in (34)–(36). The incremental voltage v is related to the incremental current i_s with a time-varying Volterra series, as

$$v = H_1(t, f_a) \circ i_s + H_2(t, f_a, f_b) \circ i_s^2 + H_3(t, f_a, f_b, f_c) \circ i_s^3 + \cdots$$
(49)

Substituting (49) into (42), equating terms of similar power of i_s , and using the usual notation for i_s as a sum of sinusoids [1], we obtain (50)–(52), shown at the bottom of the next page. In these equations, the bar above certain terms denotes as usual the average over all the terms that result from all possible permutations of the frequency arguments [1]. These are linear differential equations with periodic boundary conditions and were solved as described in [20] for the case of a periodic ac analysis, by discretizing them and solving one algebraic sparse linear

system of equations. Once the time-varying Volterra series that relates i_s with v is known (coefficients H_1 , H_2 , and H_3), it can be cascaded with the time-varying power series which relates v with the output current i_{o1} , whose coefficients are

$$d_1(t) = f_{1V}(t) - f_{2V}(t)$$
(53)

$$d_2(t) = \frac{1}{2}(f_{1VV}(t) - f_{2VV}(t)) \tag{54}$$

$$d_3(t) = \frac{1}{6}(f_{1VVV}(t) - f_{2VVV}(t)) \tag{55}$$

in order to relate i_s with i_{o1} as follows:

$$i_{o1} = P_1(t, f_a) \circ i_s + P_2(t, f_a, f_b) \circ i_s^2 + P_3(t, f_a, f_b, f_c) \circ i_s^3 + \cdots$$
 (56)

Above

$$P_{1}(t, f_{a}) = d_{1}(t)H_{1}(t, f_{a})$$

$$P_{2}(t, f_{a}, f_{b}) = d_{1}(t)H_{2}(t, f_{a}, f_{b})$$

$$+ d_{2}(t)H_{1}(t, f_{a})H_{1}(t, f_{b})$$
(58)

$$P_{3}(t, f_{a}, f_{b}, f_{c}) = d_{1}(t)H_{3}(t, f_{a}, f_{b}, f_{c}) + 2d_{2}(t)\overline{H_{1}(t, f_{a})H_{2}(t, f_{b}, f_{c})} + d_{3}(t)H_{1}(t, f_{a})H_{1}(t, f_{b})H_{1}(t, f_{c}).$$
(59)

As with low frequencies, time-invariant Volterra coefficients $B_1(f_a)$, $B_2(f_a,f_b)$, and $B_3(f_a,f_b,f_c)$ that describe intermodulation in the frequency band of interest can be extracted by taking the first Fourier coefficients of $P_1(t,f_a)$, $P_2(t,f_a,f_b)$, and $P_3(t,f_a,f_b,f_c)$, respectively. Assume that the nth time-varying Volterra coefficient has the following Fourier expansion:

$$P_n(t,\cdot) = \sum_{k=-\infty}^{\infty} P_{n,k}(\cdot)e^{j2\pi k f_{\text{LO}}t}$$
 (60)

where a dot has replaced the frequency arguments. For a down-converter $P_{n,-1}(\cdot)$ must be used if the input signal frequency f_s is higher than $f_{\rm LO}$, or its conjugate if f_s is lower than $f_{\rm LO}$. For an upconverter $P_{n,1}(\cdot)$ must be used when the output frequency is higher than $f_{\rm LO}$ while the conjugate of $P_{n,-1}(\cdot)$ must be used if

the output frequency is lower than f_{LO} , but the result is essentially the same if the input signal frequency is low compared to f_{LO} .³

If i_s consists of two tones of equal magnitude as in (17) where $f_1 \approx f_2 \approx f_s$ and f_s is the input signal frequency, the third-order intermodulation generated by the switching pair can now be calculated as

$$IM_3 = \frac{3}{4} \cdot \left| \frac{B_3}{B_1} \right| \cdot I_s^2 \tag{61}$$

where we have used the notation $B_1=B_1(f_s)$ and $B_3=B_3(f_s,f_s,-f_s)$. It is easy to see that to evaluate these coefficients we need $H_1(t,f_s)$, $H_2(t,f_s,f_s)$, $H_2(t,f_s,-f_s)$, and $H_3(t,f_s,f_s,-f_s)$. Hence we must solve (50) once, (51) twice, and (52) once.

The total mixer distortion can be found by cascading the power series or Volterra series that describes the transconductance stage with the time-invariant Volterra series derived for the switching pair. Assuming that the Volterra series that describes the transconductance stage is

$$i_s = A_1(f_a) \circ v_{in} + A_2(f_a, f_b) \circ v_{in}^2 + A_3(f_a, f_b, f_c) \circ v_{in}^3$$
(62)

the Volterra coefficients that describe the total mixer distortion are

$$C_1(f_a) = B_1(f_a)A_1(f_a)$$

$$C_2(f_a, f_b) = B_1(f_a + f_b)A_2(f_a, f_b)$$
(63)

$$+B_{2}(f_{a}, f_{b})A_{1}(f_{a})A_{1}(f_{b}) \tag{64}$$

$$C_3(f_a, f_b, f_c) = B_1(f_a + f_b + f_c)A_3(f_a, f_b, f_c)$$
(65)

$$+2\overline{B_2(f_a, f_b + f_c)A_1(f_a)A_2(f_b, f_c)}$$
 (66)

$$+B_3(f_a, f_b, f_c)A_1(f_a)A_1(f_b)A_1(f_c).$$
 (67)

(52)

To calculate $C_3(f_1,f_1,-f_2)$, besides $B_1(f_s)$ and $B_3(f_s,f_s,-f_s)$ we need $B_2(f_s,0)$ and $B_2(-f_s,2f_s)$ which implies that $H_2(f_s,0)$, $H_2(-f_s,2f_s)$, $H_1(0)$, and $H_1(2f_s)$ must also be calculated. Approximately, the second-order

 $\frac{{}^3\text{We} \quad \text{mention}}{P_{n,k}(f_1,\cdots,f_n)} \text{ that } \frac{\overline{P_n(t,f_1,\cdots,f_n)}}{P_n(t,f_1,\cdots,f_n)} = P_n(t,-f_1,\cdots,-f_n) \text{ and } \frac{P_n(t,f_1,\cdots,f_n)}{P_n(t,f_1,\cdots,f_n)} = P_n(t,-f_1,\cdots,f_n)$ where here the bar denotes the complex conjugate.

$$G(t)H_{1}(t,f_{a})e^{j2\pi f_{a}t} + \frac{d}{dt}\left[C(t)H_{1}(t,f_{a})e^{j2\pi f_{a}t}\right] = e^{j2\pi f_{a}t}$$

$$G(t)H_{2}(t,f_{a},f_{b})e^{j2\pi(f_{a}+f_{b})t} + \frac{d}{dt}\left[C(t)H_{2}(t,f_{a},f_{b})e^{j2\pi(f_{a}+f_{b})t}\right]$$

$$= -G_{v}(t)H_{1}(t,f_{a})H_{1}(t,f_{b})e^{j2\pi(f_{a}+f_{b})t} - \frac{d}{dt}\left[C_{v}(t)H_{1}(t,f_{a})H_{1}(t,f_{b})e^{j2\pi(f_{a}+f_{b})t}\right]$$

$$G(t)H_{3}(t,f_{a},f_{b},f_{c})e^{j2\pi(f_{a}+f_{b}+f_{c})t} + \frac{d}{dt}\left[C(t)H_{3}(t,f_{a},f_{b},f_{c})e^{j2\pi(f_{a}+f_{b}+f_{c})t}\right]$$

$$= -\left[(2G_{v}(t)\overline{H_{1}(t,f_{a})H_{2}(t,f_{a},f_{b})} + G_{vv}(t)H_{1}(t,f_{a})H_{1}(t,f_{b})H_{1}(t,f_{c}))e^{j2\pi(f_{a}+f_{b}+f_{c})t}\right]$$

 $-\frac{d}{dt} \left[(2C_v(t)\overline{H_1(t,f_a)H_2(t,f_a,f_b)} + C_{vv}(t)H_1(t,f_a)H_1(t,f_b)H_1(t,f_c))e^{j2\pi(f_a+f_b+f_c)t} \right]$

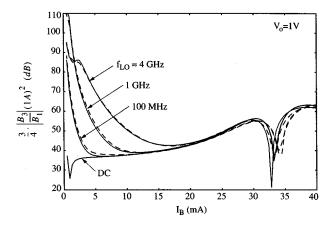


Fig. 12. High-frequency intermodulation prediction (solid line) and simulation with spectreRF (dashed line) for a switching pair operating as a downconverter, versus bias current and for several LO frequencies. The model corresponds to a 0.25 μ m technology, the channel width is 100 μ m, and the the LO amplitude is 1 V.

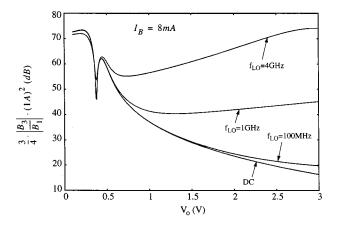


Fig. 13. High-frequency intermodulation versus LO amplitude, for a fixed bias current and several LO frequencies.

interaction can be neglected and the total mixer distortion can be given as the sum of the intermodulation generated by the transconductance stage and the switching pair separately, in a similar fashion to (30) for the low-frequency case. It is worth noting, however, in the example of Fig. 21, that when the high-frequency switching-pair nonlinearity dominates the mixer distortion, the interaction between the two stages partially improves linearity and the total mixer intermodulation is lower than that of the switching pair alone. This behavior is not observed at low frequencies.

B. Results and Comments

Fig. 12 shows intermodulation for downconversion operation, as predicted with the above method and as simulated with SpectreRF, versus bias current and for several values of the LO frequency. The quarter-micron technology whose BSIM3 version 3 model is available was used, the channel width was 100 μ m and the LO amplitude was 1 V. Similar simulation with the BSIM3 version 2 model results in a high-frequency intermodulation curve with large discontinuities, caused by discontinuities in the derivatives of the gate–source capacitance of this model.

Fig. 13 shows intermodulation for the same switching pair of the same 0.25- μ m technology, performing downconversion as

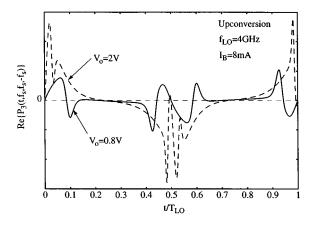


Fig. 14. The third-order time-varying Volterra coefficient $P_3(t,f_s,f_s,-f_s)$ for fixed LO frequency $f_{\rm LO}=4$ GHz, bias current $I_B=8$ mA, and two different LO amplitudes $V_o=0.8$ V and 2 V.

a function of the LO amplitude for a fixed bias current I_B = 8 mA and several LO frequencies. We observe that contrary to the low-frequency case where the intermodulation improves monotonically as the LO amplitude increases, at high frequencies there exists an optimal value after which the intermodulation increases. The same behavior is observed for upconversion and has also been reported for bipolar transistor switching pairs in [10], [11]. Because of the higher voltage swing of the common-source node when the LO amplitude is high, higher current is injected by the parasitic capacitances which accentuates the high-frequency phenomena and alters the periodic operating point of the devices. Fig. 14 shows the real part of the third-order time-varying Volterra coefficient $P_3(t, f_s, f_s, -f_s)$ of an upconverter over one LO period, for two different values of the LO amplitude, 0.8 and 2 V, and for the same bias current 8 mA and LO frequency 4 GHz (for upconversion the complex exponentials of (50)–(52) approach 1 and the time-varying Volterra coefficients are mostly real).

Let us qualitatively comment on the role of the body effect. We have already established in Section III-A that at low frequencies the behavior of the switching pair is largely insensitive to the body effect. Observe that in the I-V relation of the transistor, the sum $V_S + V_T$ appears. Whenever because of a change in the LO voltage or the transconductance stage current a change in $V_S + V_T$ occurs, the change in V_S is smaller in the presence of body effect than in its absence, because part of the variation in $V_S + V_T$ is contributed by the change in V_T . Reduced V_S swing means that at high frequencies the body effect effectively reduces the value of the capacitance connected to the common-source node approximately by the quantity 1/(1+b)where b is the ratio of the small-signal body transconductance over the small-signal gate transconductance (although b depends on V_S , for simplicity it is considered here a constant). A typical value for the quantity 1/(1+b) is 0.9 and this modification to the capacitance value causes only a minor change to the distortion prediction. However, it has been taken into account in the predicted curves shown in this paper.

Finally, let us comment on some assumptions adopted about the local oscillator. The presence of a time-varying common LO voltage results in an additional voltage swing of the common source node and enhances the reactive effects which appear at

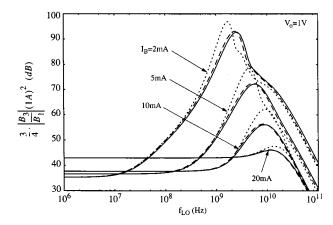


Fig. 15. Comparison of the-high frequency intermodulation prediction using realistic voltage-dependent capacitor models (solid line), a fixed-value capacitor connected from the common-source node to ground (short dashed line), and the simple approximation in which $0.25C_{\rm tot}$ is a gate-source capacitor and $0.75C_{\rm tot}$ is a fixed capacitor to ground (long dashed line).

lower frequencies. This was also verified experimentally. The assumption about the approximately sinusoidal shape of the LO voltage waveform is usually realistic at high frequencies. In the case that a tuned load *LC* buffer provides the LO signal, the LO waveform remains approximately sinusoidal as long as the load capacitance is not dominated by the time-varying gate—source capacitances. The presence of an output impedance of the local oscillator causes small error in the predicted intermodulation value if the actual applied LO waveform amplitude is considered in the prediction.

C. High-Frequency Intermodulation in Terms of Normalized Parameters

The calculation of the switching-pair intermodulation at high frequencies is very fast when compared with the performance of a circuit simulator. It requires, however, the use of numerical methods and is not easily applicable by a designer. For this reason we will attempt to capture the intermodulation performance of the switching pair in graphs of normalized variables.

Having the ability to rapidly evaluate the intermodulation of the switching pair, we can experiment with the related parameters. Neglecting the terms involving derivatives of the capacitances in (50)-(52) does not appreciably change the prediction, while replacing all the time-varying capacitors by one of constant value C_{tot} from the common-source node to ground causes only a small inaccuracy. Since for the largest part of the LO period one of M1 and M2 is cut-off, a reasonable value for C_{tot} is the sum of the total junction capacitance to ground, the gate-source capacitance of one of the two transistors in saturation, and the gate-source overlap capacitance of the other transistor. To generate the following graphs of normalized variables we will make the arbitrary but better than the constant capacitance approximation that $0.25\ C_{\mathrm{tot}}$ is a gate-source capacitance dependent on the transistor region of operation as in (38), and the rest, $0.75 C_{\text{tot}}$, is a constant capacitance to ground. Fig. 15 shows intermodulation of a switching pair operating as a downconverter versus LO frequency, for a fixed capacitor connected to the common-source node, for the simple model that arbitrarily breaks down $C_{
m tot}$ as just described, and for the more

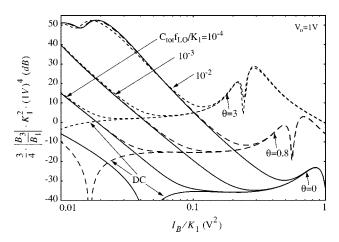


Fig. 16. High-frequency intermodulation versus bias current for several values of the parameters $C_{\rm tot}f_{\rm LO}$ and θ for $V_o=1$ V.

complete model of voltage-dependent capacitors described in Section IV-A. In this simulation, the quarter-micron technology was used, the channel width was 100 $\mu \rm m$, the LO amplitude was 1 V, and several values of the bias current are shown. It is worth noticing in this graph that for relatively high bias current, the high frequency deterioration up to very high frequencies is almost negligible.

Fig. 16 shows intermodulation of the switching pair operating as a downconverter versus bias current for a fixed LO amplitude of 1 V, for several values of the parameter θ , and for several values of the parameter $C_{\rm tot}f_{\rm LO}$, including the one that corresponds to dc. We observe that the intermodulation at any given frequency can be viewed as the sum of its value at low frequencies and a high-frequency component. In addition, the high-frequency component does not significantly depend on parameter θ , and can be approximately calculated from the particular case of $\theta=0$ which corresponds to square-law devices. For very high frequencies, however, the curves for different θ values start to deviate. For $C_{\rm tot}f_{\rm LO}/K_1=3\cdot 10^{-2}$ V, the curve for $\theta=0$ stands higher than that for $\theta=3$ V⁻¹ by approximately 6 dB.

For reasonably high LO amplitudes, and when capacitive effects are significant, we can assert that the subthreshold conduction of the devices does not significantly affect the mixer behavior. From (40) and (41), the common source potential equals

$$V_S = V_{\text{LO},c} - \frac{V_1 + V_2}{2} - V_T \tag{68}$$

where $V_{\mathrm{LO},c}$ is the common LO voltage. Using the latter in (39), assuming square-law devices and neglecting the subthreshold conduction, we obtain the equations that determine the high-frequency intermodulation

$$I_{B} = K_{1}u(V_{1})^{2} + K_{1}u(V_{2})^{2} + (C_{1} - C_{2})V_{o}\pi f_{LO}\cos(2\pi f_{LO}t) + \frac{(C_{1} + C_{2} + C_{b})}{2} \frac{d}{dt} (V_{1} + V_{2})$$

$$(69)$$

$$V_o \sin(2\pi f_{\rm LO} t) = V_1 - V_2 \tag{70}$$

where u(x) is the step function which equals its argument if it

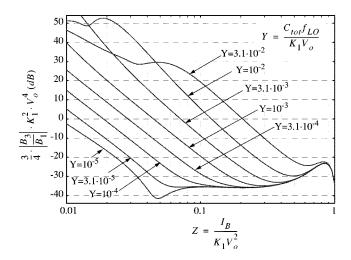


Fig. 17. Normalized high-frequency intermodulation for a downconverter and square-law devices.

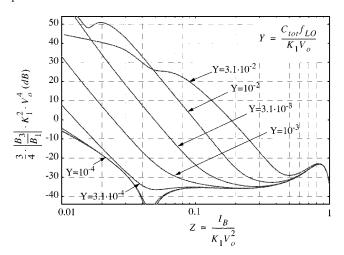


Fig. 18. Normalized high-frequency intermodulation for an upconverter and square-law devices.

is positive and is zero otherwise. Equivalently

$$\frac{I_B}{K_1 V_o^2} = u \left(\frac{V_1}{V_o}\right)^2 + u \left(\frac{V_2}{V_o}\right)^2 \\
+ \frac{(C_1 - C_2) f_{LO} \pi \cos(2\pi t')}{K_1 V_o} \\
+ \frac{(C_1 + C_2 + C_b) f_{LO}}{2K_1 V_o} \\
\cdot \frac{d}{dt'} \left(\frac{V_1}{V_o} + \frac{V_2}{V_o}\right) \tag{71}$$

$$\sin(2\pi t') = \frac{V_1}{V_o} - \frac{V_2}{V_o} \tag{72}$$

where the normalized time variable $t'=tf_{\rm LO}$ has also been introduced. It is now apparent that the high-frequency part of the intermodulation can approximately be expressed in terms of two parameters, $Z=I_B/(K_1V_o^2)$ and $Y=C_{\rm tot}f_{\rm LO}/(V_oK_1)$. Fig. 17 shows normalized intermodulation $3/4(B_3/B_1)K_1^2V_o^4$ for downconversion operation in terms of the two parameters. These particular curves were obtained for LO amplitude 1 V, but close agreement is observed if the calculations are repeated with a different one. The same normalization can be shown to

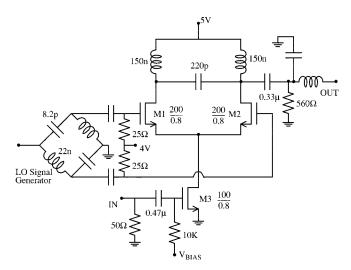


Fig. 19. Measurement setup.

be valid for an upconverter. Letting $f_s \simeq 0$, we obtain the corresponding graphs shown in Fig. 18. In these normalized graphs the body effect is neglected, but can be approximately accounted for by reducing the capacitance value as discussed previously in Section IV-B.

V. MEASUREMENTS

To experimentally verify the validity of our results, third-order input intercept point (IIP₃) measurements were taken from a single-balanced active CMOS mixer fabricated in the Philips Qubic2 process. The measurement setup is shown in Fig. 19. The LO frequency was 375 MHz, the input signal consisted of two tones around 395 MHz spaced 60 kHz apart, and the output was obtained at 20 MHz. The input was resistively matched to 50 Ω .

The width of the transconductance stage transistor was 100 μ m, that of the switching pair devices was 200 μ m, while minimum channel length 0.8 μ m was used for all the transistors. An I–V curve was obtained using the available SPICE model, and the parameters $\theta=0.94~{\rm V}^{-1},~K=10.4~{\rm mA/V^2},$ and $\eta\phi_t=44~{\rm mV}$ were extracted with curve fitting for a 100- μ m-wide device. The capacitances were also estimated from the available SPICE model and provided a total effective capacitance of approximately 0.8 pF, connected to the common-source node. For the total mixer intermodulation prediction, the nonlinearity of the transconductance stage was provided by a power series which can be easily derived from the expressions given in the Appendix.

Fig. 20 shows measurements and prediction of IIP₃ versus bias current for a fixed LO amplitude of 1 V. Very good agreement is observed. Also shown are the individual contributions of the transconductance stage and the switching pair, as well as the contribution that the switching pair would have at low frequencies. The switching pair nonlinearity dominates at high bias current. At low bias current, where the switching-pair performance deteriorates compared to dc, the performance of the transconductance stage is also poor, and as a result the total mixer intermodulation prediction is almost identical with that at low frequencies.

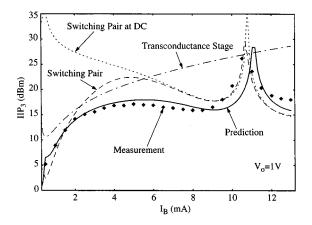


Fig. 20. Intermodulation measurements versus bias current for a fixed LO amplitude $V_o=1~{\rm V}.$

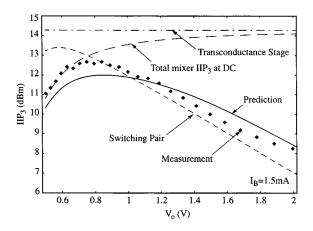


Fig. 21. Intermodulation measurements versus LO amplitude for a fixed bias current $I_B\,=\,1.5\,$ mA.

The high frequency effects are better demonstrated in Fig. 21 where the bias current is fixed at the low value of 1.5 mA and the LO amplitude is swept from 0.5 to 2 V. The individual contributions of the transconductance stage and the switching pair, together with the total mixer IIP₃ at low frequencies, are shown. Clearly the large LO amplitude causes high-frequency deterioration. Again, very good agreement between prediction and measurement is observed.

VI. CONCLUSION

A nonlinearity analysis of the CMOS transistor switching pair has been performed. We demonstrated that in the frequency band of interest its nonlinearity can be accurately described by a regular power series, or Volterra series at high frequencies, and we described how the coefficients of these series can be calculated. As a result of our analysis we produced normalized graphs from which the active-mixer intermodulation can be predicted for any technology parameters and operating conditions. Using these, the designer can rapidly estimate the suitability of a given CMOS process for a given set of mixer specifications, and can accelerate the design cycle. Several useful results were derived in the course of the analysis. The importance of a physical CMOS transistor model, describing weak, moderate, and strong inversion with a single analytical equation was demonstrated and a simple appropriate model was discussed and used.

APPENDIX

If I = f(V) is the I-V relation of a transistor in saturation as given by (1) and (2), with direct differentiation we find

$$f_V = f_X \cdot X_V \tag{73}$$

$$f_{VV} = f_{XX} \cdot X_V^2 + f_X \cdot X_{VV} \tag{74}$$

$$f_{VVV} = f_{XXX} \cdot X_V^3 + 3(f_{XX} \cdot X_V \cdot X_{VV})$$

+ $f_X \cdot X_{VVV}$ (75)

where

$$f_X = K \frac{X \cdot (2 + \theta X)}{(1 + \theta X)^2} \tag{76}$$

$$f_{XX} = K \frac{2}{(1 + \theta X)^3} \tag{77}$$

$$f_{XXX} = K \frac{-6\theta}{(1+\theta X)^4} \tag{78}$$

are the first three derivatives of f with respect to X,

$$X_V = \frac{1}{1 + s^{-2}} \tag{79}$$

$$X_{VV} = \frac{1+s^{-2}}{2\eta\phi_t} \cdot \frac{1}{(s+s^{-1})^2}$$
 (80)

$$X_{VVV} = -\frac{1}{(2\eta\phi_t)^2} \cdot \frac{(s-s^{-1})}{(s+s^{-1})^3}$$
 (81)

are the first three derivatives of X with respect to V, and

$$s = e^{(V - V_T)/(4\eta\phi_t)}$$
. (82)

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REFERENCES

- D. D. Weiner and J. E. Spina, Sinusoidal Analysis and Modeling of Weakly Nonlinear Circuits. New York, NY: Van Nostrand Reinhold, 1980
- [2] P. Wambacq and W. Sansen, Distortion Analysis of Analog Integrated Circuits. Boston, MA: Kluwer, 1998.
- [3] J. C. Rudell, J.-J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray, "A 1.9-GHz Wide-Band IF Double-Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 2071–2088, Dec. 1977.
- [4] A. N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and mixer," *IEEE J. Solid-State Circuits*, vol. 11, pp. 1939–1944, Dec. 1996.
- [5] S. Wu and B. Razavi, "A 900-MHz 1.8-GHz CMOS Receiver for Dual-Band Applications," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2178–2185, Dec. 1998.
- [6] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LANs," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1382–1385, Oct. 1999
- [7] P. Orsatti, F. Piazza, and Q. Huang, "A 20-mA-receive 55-mA-transmit single-chip GSM transceiver in 0.25-\(\mu\)m CMOS," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1869–1880, Dec. 1999.
- [8] M. T. Terrovitis and R. G. Meyer, "Noise in current-commutating CMOS mixers," *IEEE J. Solid State Circuits*, vol. 34, pp. 772–783, June 1999.
- [9] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE J. Solid State Circuits*, vol. 33, pp. 1023–1036, July 1998.

- [10] R. G. Meyer, "Intermodulation in high-frequency bipolar transistor integrated-circuit mixers," *IEEE J. Solid State Circuits*, vol. SC-21, pp. 534–537, Aug. 1986.
- [11] C. Hull, "Design and Optimization of Receivers," Ph.D. dissertation, Univ. Calif., Berkeley, 1992.
- [12] R. B. Swerdlow, "Analysis of Intermodulation Noise in Frequency Converters by Volterra Series," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-26, pp. 305–313, Apr. 1978.
- [13] S. Maas, "Two-tone intermodulation in diode mixers," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-35, pp. 307–314, Mar. 1987.
- [14] S. Maas and D. Neilson, "Modeling MESFETs for intermodulation analysis of mixers and amplifiers," *IEEE Trans. Microwave Theory and Techniques*, vol. 38, pp. 1964–1971, Dec. 1990.
- [15] Y. Tsividis, K. Suyama, and K. Vavelidis, "Simple 'reconciliation' MOSFET model valid in all regions," *Electron. Lett.*, pp. 506–508, Mar. 1995
- [16] BSIM3 Version 3 Manual, Final Version. BSIM Research Group, Dept. Elec. Eng. Comput. Sci., Univ. Calif., Berkeley. [Online] Available: http://www-device.EECS.Berkeley.EDU/~bsim3
- [17] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 3rd ed. New York, NY: Wiley, 1993.
- [18] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, Numerical Recipes in C—The Art of Scientific Computing, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 1992, pp. 650–655.
- [19] R. Telichevesky, K. Kundert, I. Elfadel, and J. White, "Fast simulation algorithms for RF circuits," in *Custom Integrated Circuits Conf.*, 1996, pp. 437–444.
- [20] R. Telichevesky and K. Kundert, "Efficient ac and noise analysis of two-tone RF circuits," in *Design Automation Conf.*, 1995, pp. 292–297.
- [21] K. Kundert and A. Sangiovanni-Vincentelli. Sparse 1.3, A Sparse Linear Equation Solver. [Online] Available: www.netlib.org/sparse



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