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Internal Current Return Path for Ground Leakage Current Mitigation in Current Source Inverters

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ABSTRACT This paper analyzes in detail the effect of a simple solution for ground leakage current mitigation applicable to transformerless three-phase current source inverter (CSI). The circuit modification solution is assessed for both traditional CSI topology and for CSI with an additional seventh switch, in literature named CSI7 (or H7), in particular with the splitting of the dc input inductance. In the present work, the solution is applied to grid-connected converters for string photovoltaic applications: scope of the circuit modification is to provide an internal return path from the wye connected capacitors of the output CL filter. This additional return path is able to significantly reduce the ground leakage current without adversely affecting THD. The performance of the proposed solution is assessed by the numerical simulations in case of a string of photovoltaic (PV) modules and the different behavior of CSI and CSI7 topologies is thoroughly investigated. Furthermore, the definition of V_{cmZC} is assessed by applying it to the common mode equivalent circuits for CSI7 with additional return path and their validation by means of a two-step simulation. The simulation results and experimental validation shows good agreement and confirm that the proposed solution is able to strongly reduce the ground leakage current.

INDEX TERMS Current source inverter, photo-voltaic power systems, ground leakage current, renewable energy sources.

I. INTRODUCTION

Current Source Inverter (CSI) topologies constitute an alternative solution to the Voltage Source Inverter (VSI) paradigm, and they have been exploited for medium voltage applications [1]. Because of the intrinsic voltage boosting behavior and with the development of high-frequency switching devices, they have been investigated for single-stage photovoltaic (PV) inverter solutions [2], [3]. Because no electrolytic capacitor is needed for the DC link, a microinverter realized with a CSI would have a lifetime similar to the one of the PV panel [4].

The usual installation of PV panels implies the presence of a metal frame to which the solar cells are assembled. In the case of large installation, the metal frame constitutes a sizeable part of the structure. For safety reasons, the metal surfaces must be grounded, to prevent the electrocution of the personnel and to detect faults towards ground.

Although necessary from the point of view of the safety, because of the presence of a parasitic capacitance between the solar cells and the metal frame, it is possible for ground leakage current to flow through the circuit composed of the electrical grid, the parasitic capacitance and the metal frame of the panel. The magnitude of this current can be high and can constitute a safety risk itself, if precautions are not taken [5].

The issue of the ground leakage current has been addressed extensively for the VSI topologies, where usually modified structures of the power electronics are adopted [6], [7]. Also passive solutions based on common mode filters have been proposed [8].

Because of the development of the semiconductor devices and market needs, reverse blocking devices did not achieve performance comparable to the devices without reverse

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voltage blocking capabilities. This has forced the CSI adopters to add diodes in series to the switches, with the obvious drawback of increasing the conduction losses. A modification to the CSI topology have been performed, with the attempt of solving the efficiency issue, has been recently proposed for PV system [9], [10]. In this paper, a simple solution is analyze to dramatically reduce the ground leakage current of a CSI7 converter used for PV systems. It is worth mentioning that the development of wide-bandgap semiconductors with bi-directional voltage blocking capability may reverse this trend in the near future, making CSI topologies even more competitive. An initial version of this work has been presented at the IEEE ECCE2018 [11], in the present version, a comprehensive study of the common mode circuit is carried out and additional results are reported.

The paper is organized as follows: Section II describes the CSI7 topology, Section III shows the novel approach for ground leakage current reduction. A performance comparison between CSI and CSI7 is shown in Section IV. Section V explains the design criteria and Sections VI and VII present the results.

II. CSI7 TOPOLOGY

Figure 1 shows the CSI7 topology, where an additional device is added to the full-bridge with respect to the traditional CSI topology.

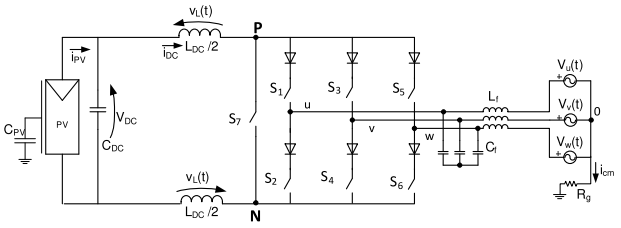

FIGURE 1. Schematic of CSI7 topology.

As for the three-phase VSI, there are six admissible active space vectors (SV), but there are three zero vector, obtained by causing a leg short circuit with one of the three legs. Although these are admissible states also for the CSI7 topology, the main advantage is to employ S7 to generate the zero vector. In this way, the conduction losses during the zero state are dramatically reduced (only one device carrying the current instead of four). If a sizeable amount of reactive power must be processed by the converter (as per some grid regulations), the voltage over S7 could be reversed, causing the body diode to switch on. If this operation can happen, a series diode must be introduced to S7.

A degree of freedom of the Space Vector Modulation (SVM) is to select the sequence of the active and zero states. It has been shown in [9] that he alternated SVM (in Figure 2) allows improving both the ground leakage current both the grid power quality. By alternating the sequences during the odd and even sextant, it is possible to reduce harmonic excitation of the output filter, improving the power quality.

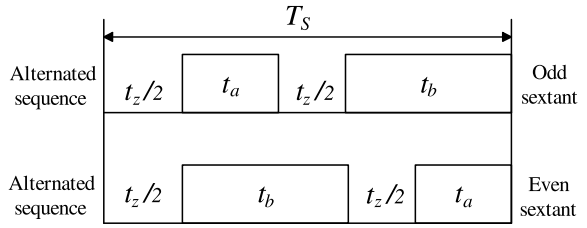

FIGURE 2. Alternated SVM.

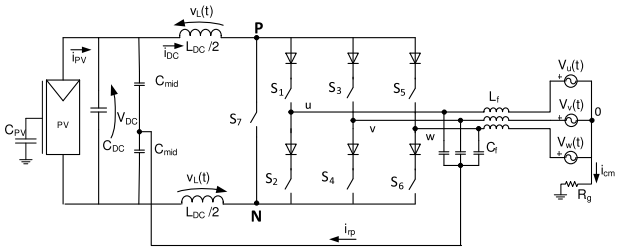

FIGURE 3. Schematic of CSI7 topology with integrated i_{CM} return path.

III. CSI7 TOPOLOGY WITH COMMON-MODE RETURN PATH

Figure 3 shows the modified connection to the midpoint of the DC input voltage through two capacitors C_{mid} with the objective of reducing the ground leakage current. A similar approach has been attempted for a single-phase VSI converter in [8]. In the present manuscript, no additional common mode chokes are necessary and the solution is customized for a three-phase CSI. Advantages and disadvantages of this kind of approach will be analyzed in this section.

In order to carry out the analysis, a new definition of common mode voltage will be used: V_{cmZC} is the common mode voltage at the zero current condition. This modification is necessary, because, differently from the case of the VSI, the common mode voltage of the CSI depends on the actual current.

For completeness sake, the presence of two C_{mid} is not mandatory, as the return path could also be directly connected to each of the sides of the input capacitors. Objective of the following sections is to guide the engineers in the design of C_{mid} so that an acceptable leakage current reduction as well as the minimization of the circulating current of the converter can be achieved.

As reported in the scientific literature, the high frequency content of the common mode voltage determines a ground leakage current to flow through the parasitic capacitance of the PV panels [12]

According to literature, in CSI the v_{cm} can be calculated by using the star point of the three-phase grid voltage as voltage reference, [1], [13], resulting in eq.(1).

$$v_{cm} = \frac{V_{P0} + V_{N0}}{2} \tag{1}$$

As anticipated and shown in eq. (1), v_{cm} depends on the value of i_{cm}. For this reason, the quantity v_{cmZC} (identifies the v_{cm} signal with zero i_{cm}) will be used for the analysis.

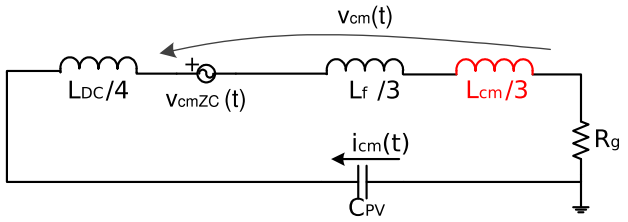

FIGURE 4. Common mode circuit of the CSI.

The common mode circuit of a grid-connected CSI converter is shown in Figure 4. The inductor L_{CM} is a three-phase common-mode choke that is quite often adopted for electromagnetic interference (EMI) mitigation in off-the-shelf power converters. Because the common mode inductor is connected in series with the parasitic capacitance, an appropriate choice of the parameter must be operated, so that the the switching harmonics are at higher frequency. Having the resonance at lower frequency also allows for an improvement of the power quality, as the common mode circuit could act as a secon-order filter for the common mode voltage harmonics.

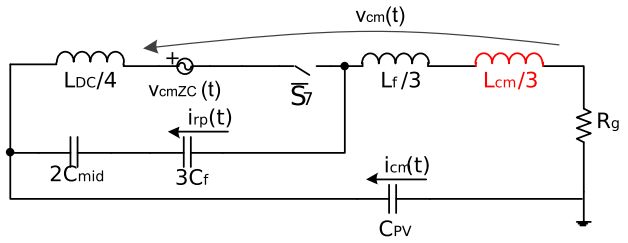

FIGURE 5. Common mode circuit of CSI with integrated i_{CM} return path.

In Figure 5 the common mode circuit of the CSI7 with integrated return path is depicted. As can be seen, a switch models the decoupling of the mains and the DC input when the zero vector is applied. As it appears evident from the circuit, the return path is more effective if the impedance $2C_{mid}$ and $3C_f$ is lower than the path composed of the inductors and the parasitic capacitance. In fact, the two branches act as a current divider for the i_{cm}.

Although the integrated return path could be applied to any CSI-based topology, it will be shown in the next section that the magnitude of the current flowing through this additional branch could be too high.

IV. CLASSIC CSI VS CSI7 BEHAVIOR

Figure 6 shows the switches sequence for the first sextant in case of CSI topology with Alternated modulation. In case of traditional CSI topology, the zero state is applied by turning on the switches S_1 and S_2, as shown in Fig.6-1. When taking into consideration the additional return path in case of traditional CSI topology, the circuit during the zero state becomes the one shown in Fig.8. In this figure it is possible to see that there is a circuit formed by only one of the capacitors C_{mid} and DC input inductors $L_{DC}/2$ (due to the presence of the two diodes) and the output CL filter connected as in Fig. 8 together with the grid phase voltages. Since before the application of the zero vector the voltages across the capacitors C_f are very close to the grid phase voltages, and the voltage across every C_{mid} is equal to $V_{DC}/2$ a large current can flow in the resulting multi-resonant circuit.

Figure 7 summarizes the switches sequence for the first sextant in case of CSI7 topology with Alternated modulation. In case of CSI7 topology, the zero state is applied by turning on the additional seventh switch S_7 with all the other switches off, as shown in Fig.7-1. When introducing the additional return path, the circuit becomes the one depicted in Fig.9. With the CSI7 topology is possible to use the return path, because during the zero state the voltages on filter capacitors don't change significantly thanks to the disconnection of the main full-bridge outputs from C_f capacitors.

Summarizing the issues of the application of the return path, the proposed solution is only viable in case of CSI7 topologies with split input inductors, as the split input inductors limit the value of i_{RP}, as it can be seen by analyzing the common-mode circuit of Fig. 5: in case of a single input inductor the equivalent impedance related to L_{DC} disappears.

V. CONSIDERATIONS ON DC SPLIT CAPACITANCE VALUES

The design of the split capacitance must achieve the two objectives:

- minimization of the split capacitance to reduce the cost and weight of the converter
- reduction of the ground leakage current i_{cm}
- minimization of the current in the return path i_{RP}

These requirements translate into the need of a considerably low impedance of the overall return path at the harmonic frequencies of v_{cmZC}. It is important to highlight that the output filter $3C_f$ is connected in series to the return path, so increasing the value of the split capacitance much above the output filter ones would lead to no additional current reduction.

The common mode impedance $i_{cm}/v_{cmZC}(j\omega)$ of the circuit of Fig. 5 is evaluated. The parameters are listed in TABLE 1 and 2 and the results are shown in Fig. 10.

The same parameters will be used in Section VI for the numerical simulations.

As can be seen from the graph of Fig. 10, values in the range of uF for the return path capacitor allows for a marked attenuation, whereas increasing C_{mid} above 7 uF, there is no significant benefits. If $C_{mid} = 0$, it means that the CSI converter does not have a return path.

The resulting ground leakage current depends not only on the value of the common mode impedance, but also on the value of the common mode voltage v_{cmZC}. For this reason, the harmonic component is evaluated in Figs 11 and 12. The main switching harmonics are located at twice the switching frequency $2f_s = 50kHz$ whereas the harmonics introduced by the space vector modulation are at $3f_{grid}$.

As anticipated, the selection of the return path capacitor C_{mid} must also comply with a limitation of the return path current. The value 7 uF represents the optimum of

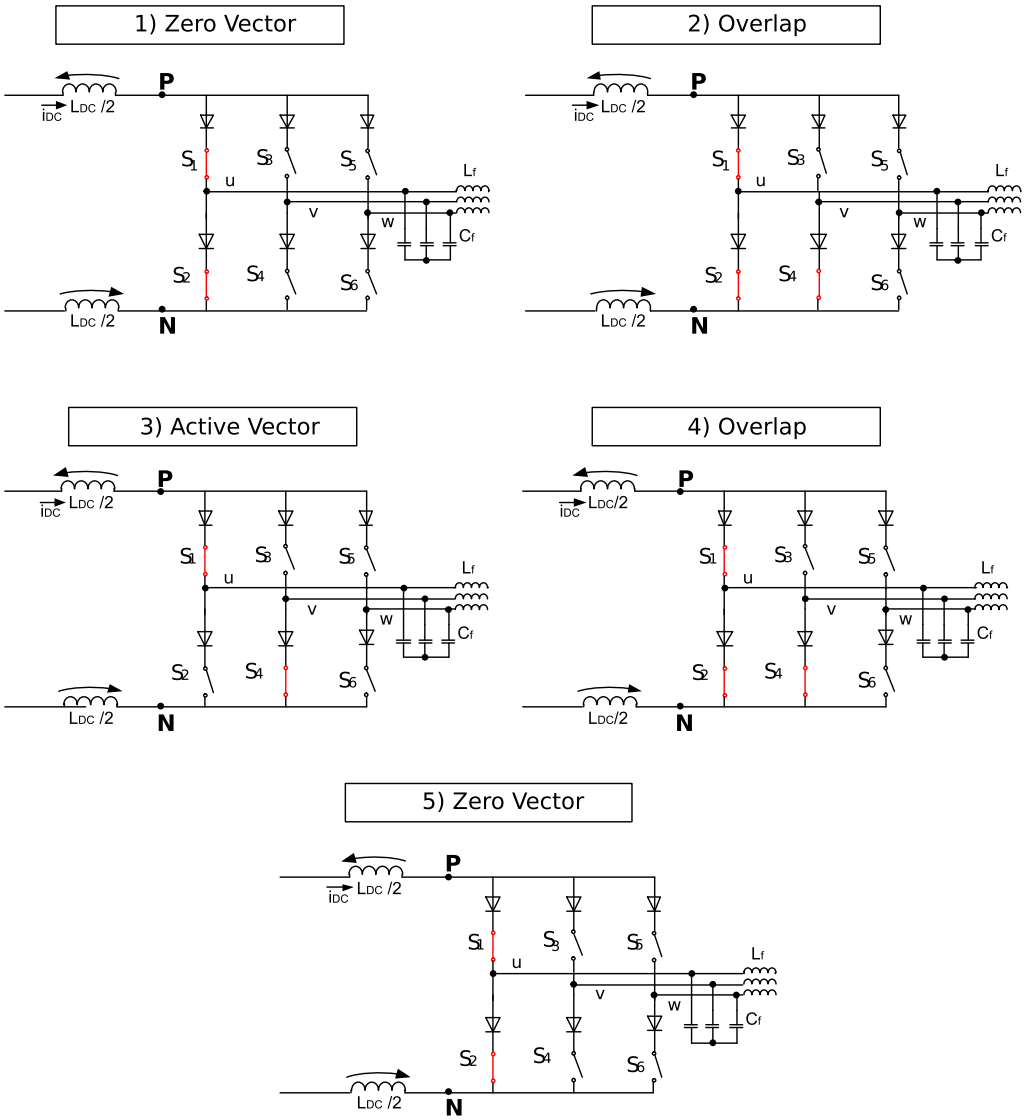

FIGURE 6. Switch configuration of Classic CSI during Alternated modulation (sequence covers one half period): (1) zero vector; (2) overlap time; (3) active vector; (4) overlap time; (5) zero vector.

the capacitance size and leakage current minimization, but a lower value could be chosen to limit the magnitude of the return path current i_{RP}.

VI. NUMERICAL SIMULATIONS

All the numerical simulations were carried out in Matlab - PLECS environment considering a string PV source composed by a varying number of PV modules, working under MPP condition. The same parameters of TABLE 2 are used, considering 150nF/kWp as the worst case scenario, that translates into 37.5nF for each module.

Two sets of simulations were carried out separately, in order to assess the internal return path solution feasibility in case of different CSI topologies operated with Alternated modulation and to assess the usefulness of the developed CM equivalent circuits under the definition of V_{cmZC}.

The first set of simulations is aimed at verifying the effectiveness of the proposed internal return path solution at reducing i_{cm} value in CSI7 topologies.

For a better modeling of the actual condition, a common mode choke with inductance equal to $L_{cm} = 3 \times 2$mH is considered, as explained in Section II.

TABLE 1 summarizes all the relevant simulation parameters for the power converter simulations.

A simulation comparison between three different topologies with alternated SVM is carried out in Figure 13 considering the ground leakage current as benchmark: CSI, CSI7 and CSI7 with return path (CSI7+RP). Even with a visual inspection of the waveforms, it is evident that there is a significant benefit changing from a CSI topology to a CSI7 one. CSI7+RP reduces the ground leakage current even further.

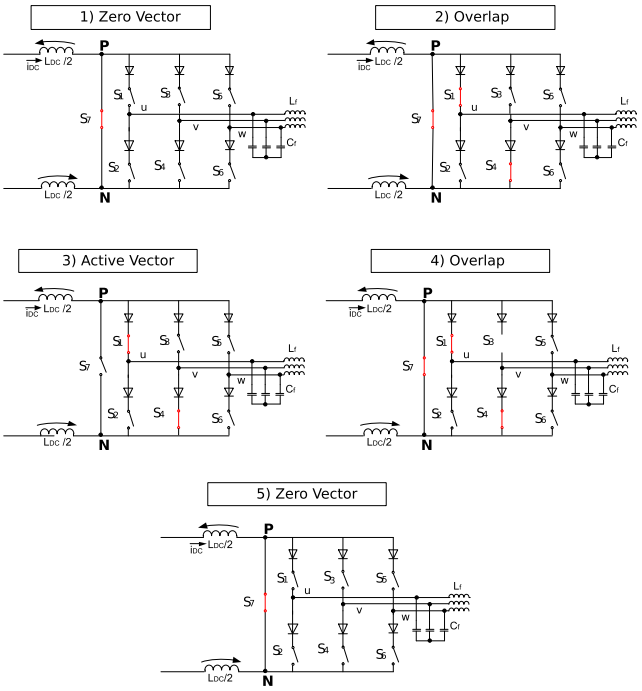

FIGURE 7. Switch configuration of CSI7 during Alternated modulation (sequence covers one half period): (1) zero vector; (2) overlap time; (3) active vector; (4) overlap time; (5) zero vector.

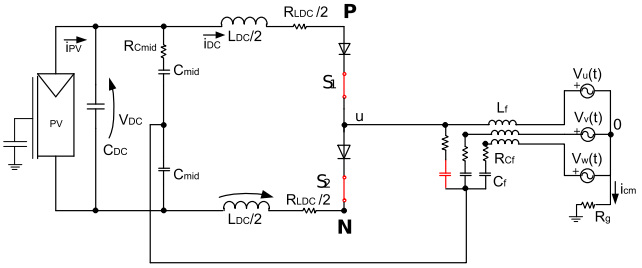

FIGURE 8. Zero state simplified circuit in case of CSI topology with integrated i_{CM} return path.

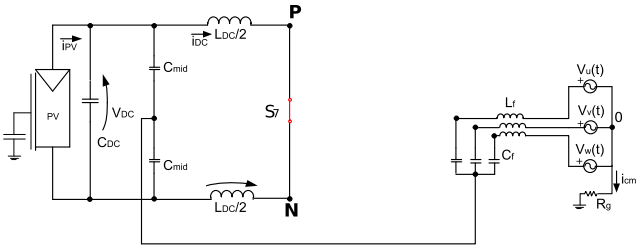

FIGURE 9. Zero state simplified circuit in case of CSI7 topology with integrated i_{CM} return path.

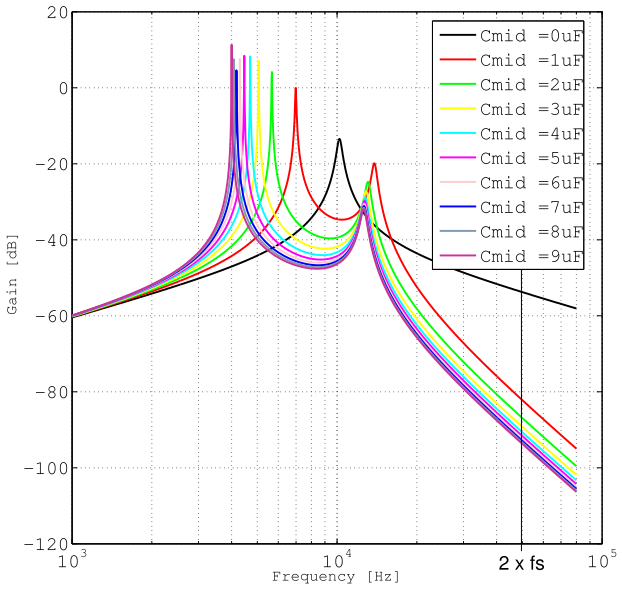

FIGURE 10. Bode Plot of $i_{cm}/v_{cmZC}(j\omega)$ of the CSI7 with integrated return path and 8 panels.

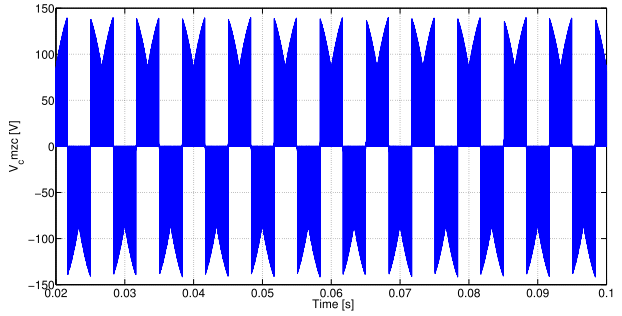

FIGURE 11. v_{cmZC} with 8 PV modules.

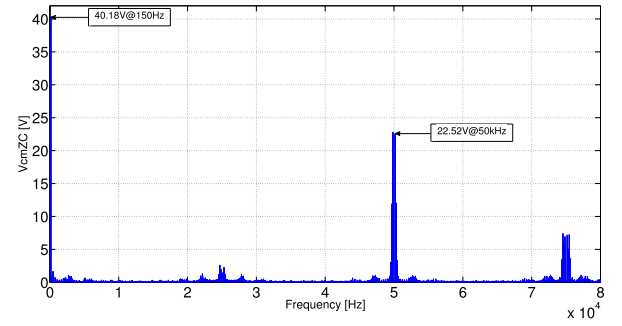

FIGURE 12. FFT of v_{cmZC} with 8 PV modules.

Figure 14 shows the phase voltage, grid current and i_{RP} in the case of CSI7+RP. Return path current i_{RP} results 0.17 A (rms) with a phase current of 1.41 A (rms).

An analysis of the current flowing through the filter capacitors I_{C_f} shows that no great difference exists between the topologies.

The performance comparison considering a different number of PV modules vor the CSI7+RP is reported in Table 4. The increase of the modules implies an increase of the ground leakage current. It can be seen that this increment is non linear (more than proportional) because the increase of C_{PV} reduces the effectiveness of the return path if considering the

TABLE 1. Power converter parameters.

Name	Value	Unit
L_{DC}	2	mH
f_S	25	kHz
T_{ov}	2	us
V_{grid} (line-to-line)	400	V (rms)
f_{grid}	50	Hz
L_f	1.4	mH
L_{cm}	2	mH
C_f	1.5	uF
R_g	4.7	Ohm
C_{mid}	7	uF

TABLE 2. Nameplate values of the PV module used in simulations.

Name	Value	Unit
V_{mpp}	30.3	V
I_{mpp}	8.24	A
$C_{PV_{single-module}}$	37.5	nF

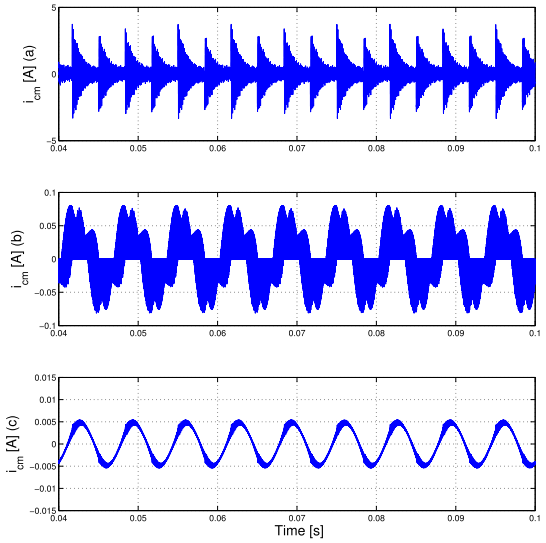

FIGURE 13. Simulation results. i_{cm} with CSI (a), CSI7 (b) and CSI7+RP (c). PV source composed by 4 modules (1kW).

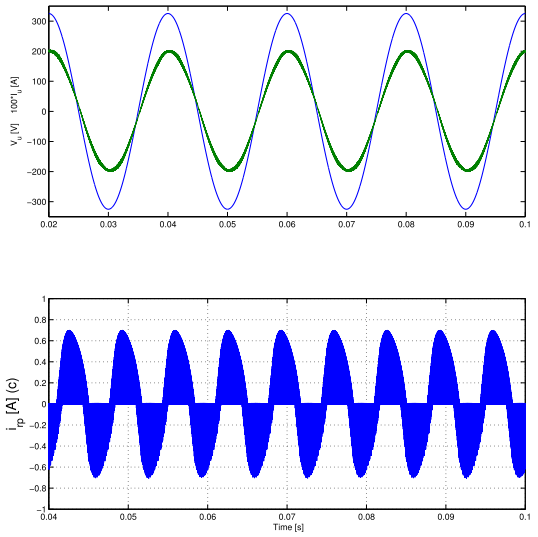

FIGURE 14. Simulation results. Voltage and current (green trace, ×100) and i_{RP} waveforms in case of CSI7+RP. PV source composed by 4 modules (1kW).

TABLE 3. Simulations results. Performance comparison in case of 4 PV modules.

Name	I_{cm} [A (rms)]	I_{cf} [A (rms)]	THD[%] I_u	I_{RP} [A (rms)]
CSI	950	3.02	29.18 %	-
CSI7	17	2.953	0.978 %	-
CSI7+RP	3.5	2.954	0.983 %	0.17

TABLE 4. Simulation results summary with CSI7+RP and CSI7 (only for I_{cm} between brackets).

Name	2 PV modules	4 PV modules	8 PV modules	Unit
$P_{modules}$	500	1000	2000	W
C_{PV}	75	150	300	nF
I_{cm}	0.51 (8.3)	3.5 (17)	13.7 (33.5)	mA (rms)
I_{RP}	66	170	290	mA (rms)
THD[%] I_u	0.99	0.98	1.08	%

same value of C_{mid}, for different number of modules. In fact, an increased C_{PV} would reduce the impedance of the grid return path compared to the internal return path.

From the same table it is possible to see that the RMS value of i_{RP} is proportional to the number of PV modules due to the proportional increase of the harmonic amplitudes of v_{cmZC}. The value of the return path current is always moderated.

The power losses of the devices in case of 8 PV modules, with and without the return path, were computed in PLECS environment using GW15N120H3 (15A, 1200V) MOSFET and RHRG30120 (30A, 1200V) diodes. The presence of the return path affects in no noticeable manner the power loss.

A second set of simulations was used to assess the proposed CM equivalent circuits. The applied method is a two-step process comprising a first step during which the converter operation is simulated with zero C_{PV} and with the disconnection of i_{cm} RP. The resulting V_{cmZC} is measured and applied to the equivalent CM circuit (see Fig. 5 by means of a controlled voltage source, in order to obtain the expected quantities i_{cm} and i_{RP}.

A subsequent simulation of the entire converter with the specified value of C_{PV} and with the connection of the additional return path is then run and the resulting same quantities are compared against each other. Since the additional return path is not technically feasible in case of traditional CSI, all the simulation were carried out only for the CSI7 topology with return path.

Figures 15 and 16 show respectively the i_{CM} waveform and a zoomed-in view of the same: as it can be seen by comparing the results obtained with the actual converter simulation against the ones from the equivalent CM circuit, there is a very good level of agreement.

The same considerations apply in case of figs. 17 and 18, that show respectively the i_{RP} waveform and a zoomed-in

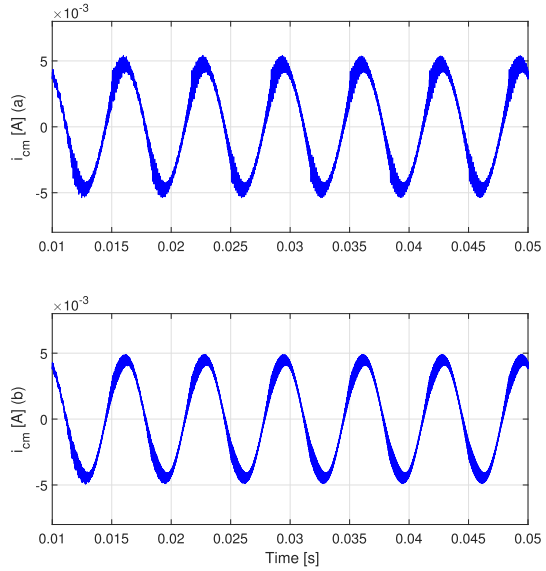

FIGURE 15. Waveform comparison of I_{CM}: Upper trace - actual converter; lower trace - equivalent CM circuit.

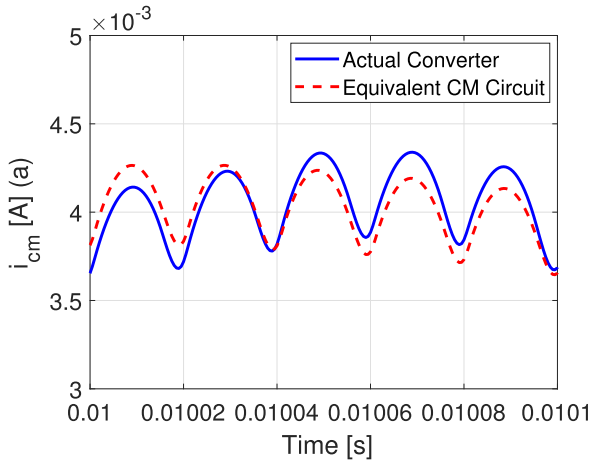

FIGURE 16. Zoomed-in waveform comparison of I_{CM}: Solid line - actual converter; dashed line - equivalent CM circuit.

TABLE 5. Experimental and simulation results comparison (simulation results between brackets).

	CSI7	CSI7+RP	Unit
I_{cm}	25.3 (17)	4.5 (3.5)	mA (rms)
I_{RP}	n.a.	129 (170)	mA (rms)

view of the same. Comparing the results obtained with the actual converter simulation against the ones from the equivalent CM circuit results in an excellent level of agreement. The good agreement was obtained despite the neglecting of the power converter behavior during overlap times.

VII. EXPERIMENTAL VALIDATION

A power electronics converter implementing the CSI7 and CSI7 with return path capabilities was realized and the prototype is shown in Fig. 19. The goal of the experiments is

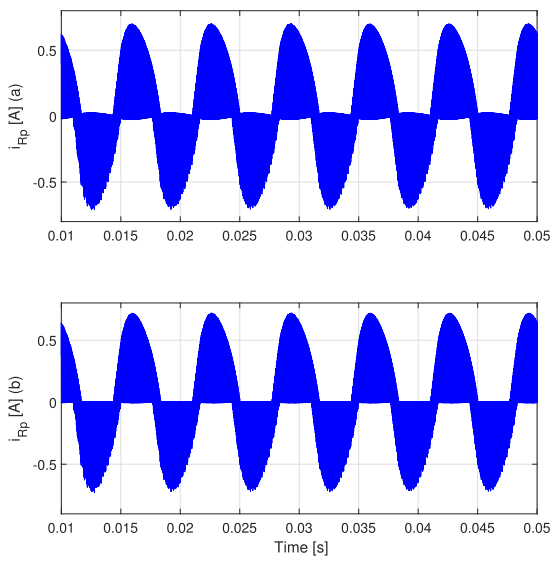

FIGURE 17. Waveform comparison of I_{Rp}: Upper trace - actual converter; lower trace - equivalent CM circuit.

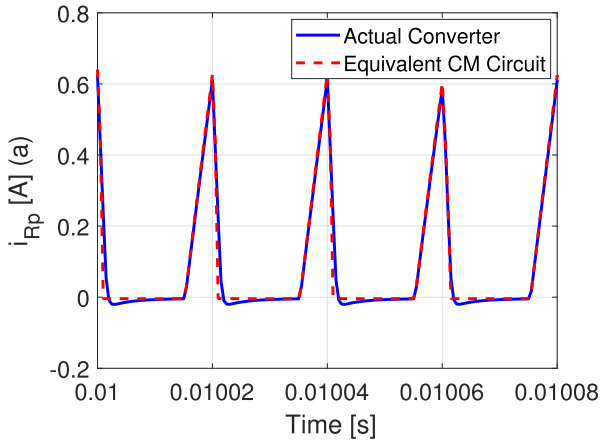

FIGURE 18. Zoomed-in waveform comparison of I_{Rp}: Solid line - actual converter; dashed line - equivalent CM circuit.

to evaluate the performance related to the ground leakage current of the different architectures. To decouple the effects of a real grid, the prototype is run in island operation. A balanced resistive load (value 252 Ohm) is used as load and the other experimental parameters match the ones used in the simulations (TABLE 1). The DC voltage $V_{DC} = 120V$ with a $C_{PV} = 100nF$. The reference current is 0.91 A) (rms) to match an equivalent grid voltage V_{grid} (line-to-line)= 400 V (rms). Because of the intrinsic boost operation of the CSI, the input voltage must be lower than the line-to-line output voltage.

The results are shown in Figures 20 and 21. A phase voltage with the ground leakage current i_{cm} and return path current i_{RP} for both solution is shown.

Although several assumptions were made in the simulation part and several non-linear effects of the power converter

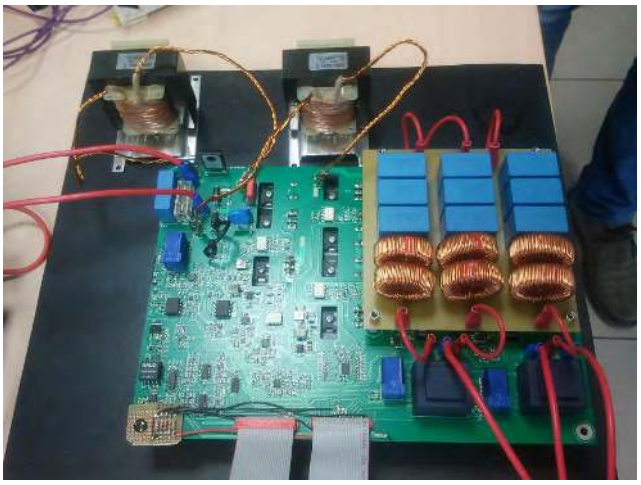

FIGURE 19. CSI7 power converter prototype.

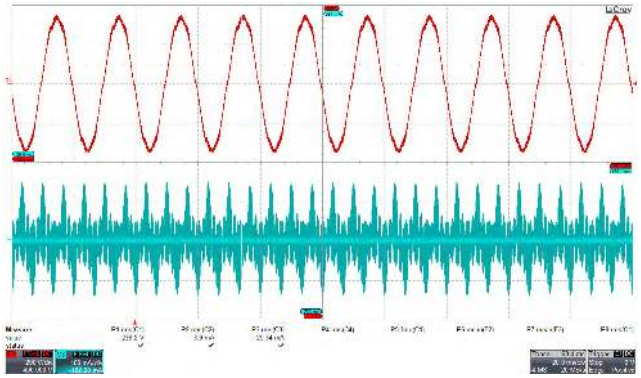

FIGURE 20. Experimental results. CSI7 topology, $i_u(t) * R_L$ (upper trace, 200V/div.), and $i_{cm}(t)$ (lower trace, 100mA/div.).

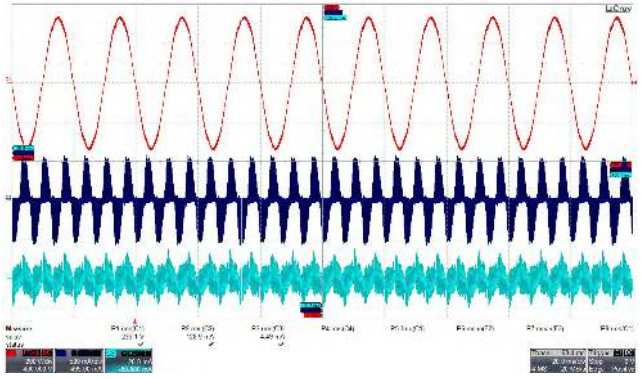

FIGURE 21. Experimental results. CSI7+RP topology, $i_u(t) * R_L$ (upper trace, 200V/div.), $i_{RP}(t)$ (middle trace, 500mA/div.) and $i_{cm}(t)$ (lower trace, 20mA/div.).

were not modeled, the mitigation of i_{cm} from 25.3 mA (rms) to 4.5 mA (rms) is confirmed. The current of the return path amounts to 129mA (rms).

In order to obtain a better agreement between simulations and experiments a better modeling of the power switches S_x should be carried out. The non linear output capacitance of the power transistors and the junction capacitance of the diodes should be taken into consideration in the simulation of the entire actual converter.

VIII. CONCLUSION

This work analyzed the critical aspects of ground leakage current in CSI grid-connected converters for string photovoltaic applications.

This manuscript carried out an in-depth analysis of the ground leakage current for Current Source Inverters used in grid-connected photovoltaic applications. The proposed approach in order to study and mitigate ground leakage currents in CSI inverter comprises two areas of intervention: first is to provide an internal return path for the common mode current, then suitable CM equivalent circuits are developed to which apply the definition of V_{cmZC} (common-mode voltage with zero stray capacitance).

The novelty of the proposed approach relies in the use of two additional capacitors in the DC link whose mid-point is connected to the star point of the CL output filter. The internal return path does not lose its effectiveness even when employing only one additional capacitor (of doubled capacitance) connected between the star point of the CL filter and the positive or negative terminal of the DC Source.

This creates an internal return path with lower impedance that prevents the ground leakage current from flowing into the grid.

Thorough study of the different behavior between traditional CSI and CSI7 topology demonstrated that the internal return path is technologically feasible only for CSI7 topology, due to the large i_{RP} in case of traditional CSI topology.

Following the definition of V_{cmZC}, different common-mode equivalent circuits for CSI and CSI7 with additional return path were developed and were validated by means of a two-step simulation process: comparing the relevant waveforms of i_{cm} and i_{RP} of the entire converter against the ones of the simplified CM circuit resulted in an excellent agreement.

Thanks to the CSI7 topology, the internal return path is able to significantly reduce the ground leakage current. Specifically, the internal return path requires only the presence of a split input DC capacitance C_{mid} and it does not require a dedicated connection to the grid neutral conductor. In sizing C_{mid} there is a point of diminishing returns, after which the attenuation of i_{cm} do not improve significantly even for very large values of C_{mid}. Simulations and experimental results are in good agreement and show that the proposed solution is able to strongly reduce the ground leakage current. The expected slight increase in power losses does not substantially affect power conversion efficiency of the CSI7 converter. Accurate power losses analysis, together with a more detailed modeling of the power switches non-linear output capacitance will be the subject of future works.

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