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Interpolation by a Prime Factor other than 2 in Low-Voltage Low-Power ΣΔ DAC

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***Abstract*—This paper presents power optimization of a sigma-delta (ΣΔ) modulator based digital-to-analog converter (DAC) for hearing-aid audio back-end application. In a number of state-of-the-art publications the oversampling ratio (OSR) of the ΣΔ modulator is chosen as a factor of integer power of two. The reason given is the simplicity of the interpolation filter (IF) block. However, being able to choose OSR factors of integer powers of two only, might be restricting and not necessarily optimal. Therefore the ΣΔ modulator based DAC designs with multistage IF that include a stage performing oversampling by a factor of 3 are investigated. This new design freedom is used to lower the operating frequency of the whole DAC and save considerable amount of power. It is shown that the figure-of-merit (FOM) of such designs can be lower than designs using oversampling by a factor of integer powers of two. The same optimization approach can be used for other low voltage low power portable audio applications (mobile phones, notebook computers etc.).**

Keywords—sigma-delta modulator; interpolation filter; class D; hearing aid; low voltage, low power

I. INTRODUCTION

High audio quality, longer operation time and small device size are parameters demanded in hearing-aids today. Optimum balance between the design parameters in every part of a hearing-aid device is therefore of vital importance, making the power consumption one of the crucial parameters for the design. This is also the case of the audio signal processing path, which requires digital-to-analog conversion and power amplification at the back-end to drive the speaker (see Fig.1). As part of the audio back-end a digital ΣΔ modulator with class D power amplifier (PA) is usually used in low-voltage low-power audio applications. Design specifications of such back-end intended for hearing-aid application are covered in Section II. The use of class D PA eliminates problems with device matching and reduced power efficiency experienced in case class AB PA is used [1, 2]. The class D PA is usually implemented as an H-bridge (schematic in Fig.1 is simplified) and operates in switched mode with switching frequency $f_{s,PA}$. Compared to [1, 2] that use class AB power stage, the class D allows to perform all signal processing before the output filter in digital domain. Digital design provides the advantage of low-voltage low-power and cost effective implementation and scales down with integrated circuit (IC) technologies of today.

When using a multi-bit ΣΔ modulator with Q bits, digital pulse width modulation (DPWM) block that turns the ΣΔ signal into symmetrical 1 bit pulse width modulation, is needed. As can be seen in Fig.1 the DPWM block requires the fastest clock in the back-end system and thus sets the system clock to $f_{s,DPWM} = 2^Q$. OSR . f_s, where f_s is the input sampling frequency.

Due to the oversampling nature of the ΣΔ modulator an IF is needed prior to the modulator. In [3] it has been shown that with the class D PA being the main power consumer in the back-end and its switching frequency $f_{s,PA}$ = OSR . f_s depending on the OSR factor, decrease of the OSR results in considerable power savings. However, as will be shown in Section III of this work, the OSR decrease and the search for optimum design might be limited when the OSR has to be a

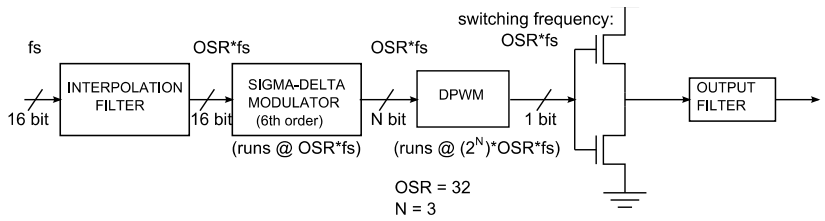

Figure 1. Simplified schematic of the back-end of audio signal processing chain: interpolation filter, ΣΔ modulator, class-D output-stage and output filter.

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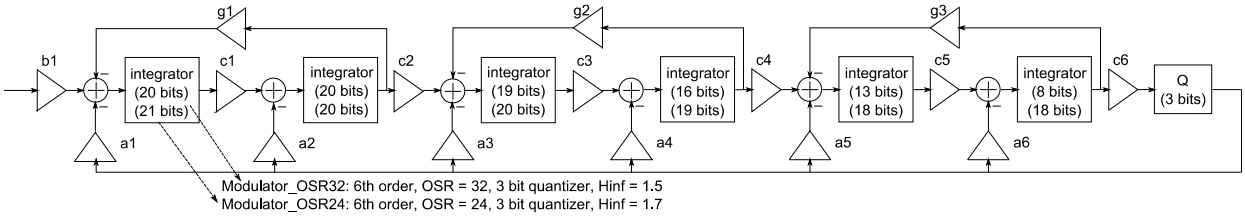


Figure 2. Simplified schematic of the 6th order ΣΔ modulator.

factor of integer power of two as in [3 - 7]. To gain more design freedom a stage performing oversampling by a factor of 3 might be used as one of the stages of the IF. Such solution is discussed in Section IV along with simulation results and comparison with previous designs. Conclusion can be found in Section V.

II. Design and Figure-of-Merit Specifications

A thorough discussion on hearing-aid audio back-end system specification and the ΣΔ modulator is provided in [4]. Ideal 16 bit quantization of the system input signal is assumed. The input signal has band-width (BW) of 10 kHz. This results in signal-to-quantization-noise ratio (SQNR) = 98 dB. The sampling frequency at the system input is fs_{in} = 22.05 kHz. The input signal of the back-end is then up-sampled using an IF and passed to the ΣΔ modulator. The IF in state-of-the-art designs [1 - 8] consists of multiple stages. Another requirement is the signal-to-noise-and-distortion ratio (SNDR) at the total output of the back-end of 90 dB. We designed the IF and the ΣΔ modulator to keep the quality of the audio signal at SNDR = 98 dB so that a margin of 8 dB is left for the performance reduction introduced by the output stage. Maximum stable amplitude (MSA) at the input of the ΣΔ modulator is also a crucial parameter in hearing-aids, the lowest limit in this work is set to -1.2 dBFS.

Note that the ΣΔ modulator in this work is fully digital and is treated as a digital filter. This allows judging the complexity and power savings of the ΣΔ modulator and the IF using the figure-of-merit:

$$FOM = \Sigma_i (b_i \,.\, OSR_i) \qquad (1)$$

Where i is the number of adders in the ΣΔ modulator block, b_i is the number of bits used in individual adders and OSR_i is the oversampling used for the individual adders. In the case of the ΣΔ modulator block OSR_i is the same for all the adders. Since most of power consumption in the IF and the ΣΔ modulator is caused by the adders, the FOM is approximately proportional to power consumption. There are more precise figures of merit for ΣΔ modulators used in other works [8]. However, these figures of merit can be used only after the design has been completed and possibly measured. The advantage of the figure of merit of Eq. 1 is that it allows comparison of different designs early in the design process allowing critical system design decisions.

III. Interpolation by a Factor of Integer Power of Two

Fig.1 shows a ΣΔ modulator based DAC that will be optimized with respect to power. The system level parameters of the ΣΔ modulator used in this DAC (see Fig. 2, Modulator_OSR32) [3] are 6th order, OSR = 32, 3 bit quantizer. Maximum noise transfer function (NTF) gain H_{inf} = 1.5 is used as advised in [8]. The coefficients of this ΣΔ modulator can be seen in Tab. I. Fig.3(a) shows the IF (IF_OSR32) used for the ΣΔ modulator of Fig. 2, Modulator_OSR32. The IF consists of 4 stages and performs oversampling by 32 in total. The first two stages are designed as IIR filters as a parallel connection of two all-pass filter cells (see Fig. 4 and Fig. 5). The coefficients used in these filters can be found in Tab. II and Tab. III. The third stage is designed as a 3rd order cascaded-integrator-comb (CIC) filter and the fourth stage as a second order CIC filter [8].

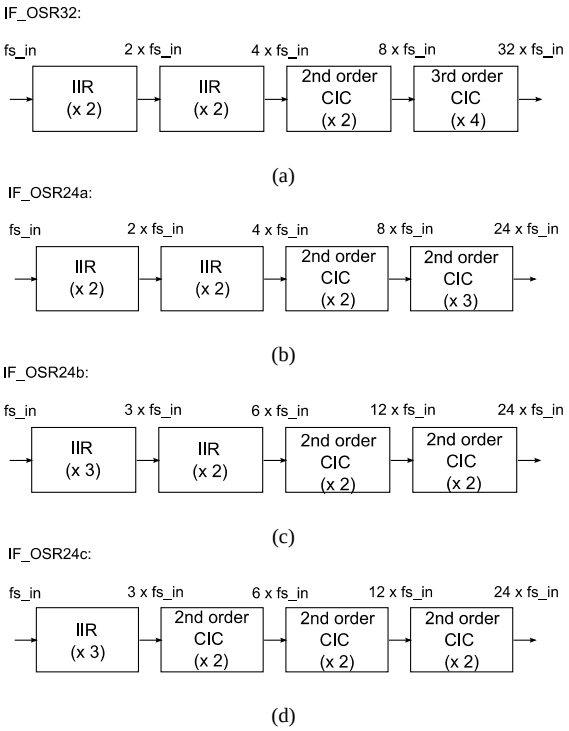


Figure 3. Multistage interpolation filters compared in this work.

TABLE I. COEFFICIENTS OF THE ΣΔ MODULATOR OF FIG.2, MODULATOR_OSR32

Coefficient	Value	Shift / Add	Adders
a_1	1/16	2^{-4}	0
a_2	0.1542	2^{-3}	0
a_3	0.1705	$2^{-3}+2^{-5}$	1
a_4	0.2532	2^{-2}	0
a_5	0.5544	$2^{-1}+2^{-5}$	1
a_6	0.6353	$2^{-1}+2^{-3}$	1
b_1	1/16	2^{-4}	0
c_1	1/8	2^{-3}	0
c_2	1/8	2^{-3}	0
c_3	1/4	2^{-2}	0
c_4	1/2	2^{-1}	0
c_5	1/2	2^{-1}	0
c_6	0.8791	$2^{0}-2^{-3}$	1
g_1	0.0044	2^{-8}	0
g_2	0.0168	2^{-6}	0
g_3	0.0167	2^{-6}	0

TABLE II. COEFFICIENTS OF THE FIST STAGE OF IF _OSR32 (FIG. 3(A))

Coefficient	Value	Shift / Add	Adders
$\mathbf{a_{1,3}}$	0.9375	$2^{-1}-2^{-4}$	1
$\mathbf{a_{0,3}}$	0.8047	$2^{-1}+2^{-2}+2^{-4}-2^{-7}$	3
$\mathbf{a_{1,2}}$	0.6406	$2^{-1}+2^{-3}+2^{-6}$	2
$\mathbf{a_{0,2}}$	0.4453	$2^{-1}-2^{-4}+2^{-7}$	2
$\mathbf{a_{1,1}}$	0.2422	$2^{-2}-2^{-7}$	1
$\mathbf{a_{0,1}}$	0.0703	$2^{-4}+2^{-7}$	1

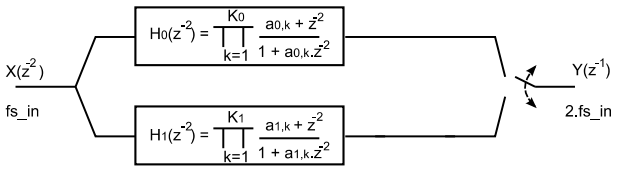


Figure 4. IIR filter using a parallel connection of two all-pass cells. Used as the first stage of IF_OSR32 (Fig. 3(a)).

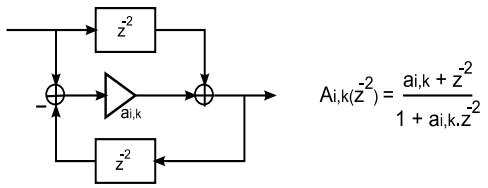


Figure 5. Second-order all-pass filter cell and its transfer function.

TABLE III. COEFFICIENTS OF THE SECOND STAGE OF IF _OSR32 (FIG. 3(A))

Coefficient	Value	Shift / Add	Adders
$\mathbf{a_{1,1}}$	0.9375	$2^{-1}+2^{-4}+2^{-6}$	2
$\mathbf{a_{0,1}}$	0.1348	$2^{-3}+2^{-7}+2^{-9}$	2

A model of this design using fixed-point arithmetic has been built and simulated in Matlab [3]. This model is transferable to VHDL. FFT spectrum of the ΣΔ modulator output signal is in Fig. 6, the transfer functions of the IF and the ΣΔ modulator are in Fig. 7. The FOM of the ΣΔ modulator and individual stages of the IF was calculated according to Eq. 1 and can be seen in Tab. IV.

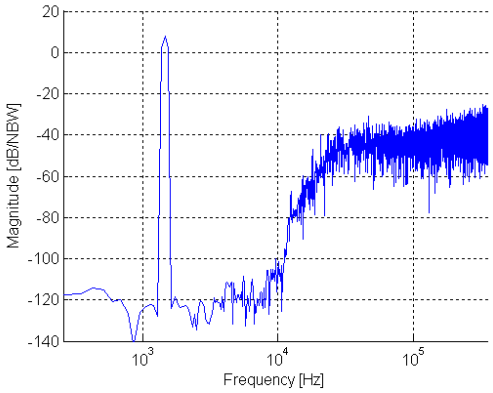


Figure 6. Output signal FFT spectrum of the ΣΔ modulator design Modulator_OSR32 (Fig.2). NBW = 1.8311e-04.

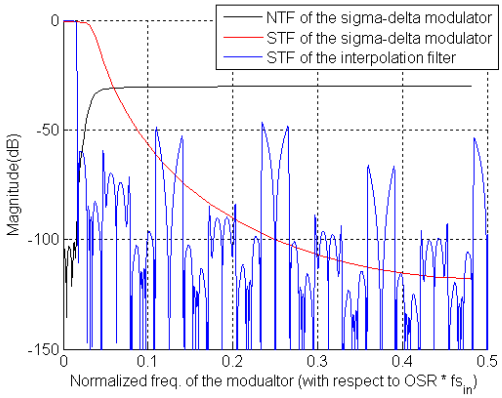


Figure 7. Transfer functiond of the ΣΔ modulator and the interpolation filter of Tab IV.

TABLE IV. FOM OF THE INDIVIDUAL BLOCKS OF IF AND OF THE ΣΔ MODULATOR

IF design	IF_OSR32	IF_OSR24a	IF_OSR24b	IF_OSR24c
IF stage 1	9.5	9.5	19.9	19.9
IF stage 2	7.2	7.2	10.8	3.4
IF stage 3	8.6	4.5	6.7	6.7
IF stage 4	25.5	53	13.5	13.5
IF total	51	74	51	43.5
ΣΔ modulator	192	180	180	180
IF + ΣΔ	243	254	231	223.5

The goal is to optimize the DAC with respect to power compared to the design of [3] by reducing the OSR of the ΣΔ modulator. If the OSR is restricted to be a factor of integer power of two the only option is to reduce the OSR from 32 down to 16. Such optimization would reduce the switching

frequency of the Class D PA by 50% and thus save 50% of power compared to the design of [3]. Moreover the power consumption of the DPWM block would also be reduced by 50% as its operating frequency $fs_{,DPWM} = 2^Q \cdot OSR \cdot f_s$ depends directly on OSR. Power consumption would also be saved in the IF because the last stage that increases the frequency from $16.f_{s\_in}$ to $32.f_{s\_in}$ would not be needed. Tab IV shows that this stage has the highest FOM of all stages and thus consumes the largest amount of power in the IF. The only block of the DAC that remains to be investigated to see whether or not this optimization approach is reasonable is the ΣΔ modulator.

For this reason a plot of achievable peak SQNR for ΣΔ modulator with 3 bit quantizer as a function of OSR for orders 1 – 8 is shown in Fig. 8.

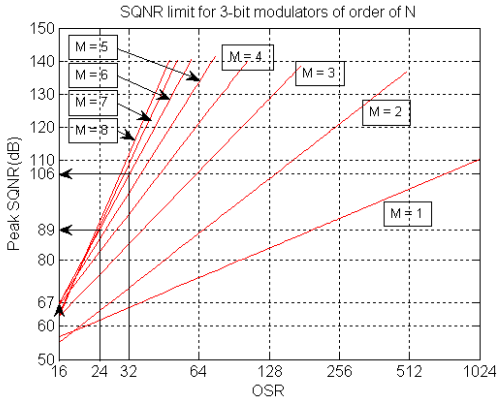


Figure 8. peak SQNR of the 3 bit ΣΔ modulator output signal as a function of OSR for modulator orders 1- 8.

It can be seen that the design of Fig.2, Modulator_OSR32 achieves 106 dB peak SQNR. Since only 98 dB SQNR is needed at the output of the ΣΔ modulator according to the specification in Section II this leaves 106 – 98 = 8 dB for

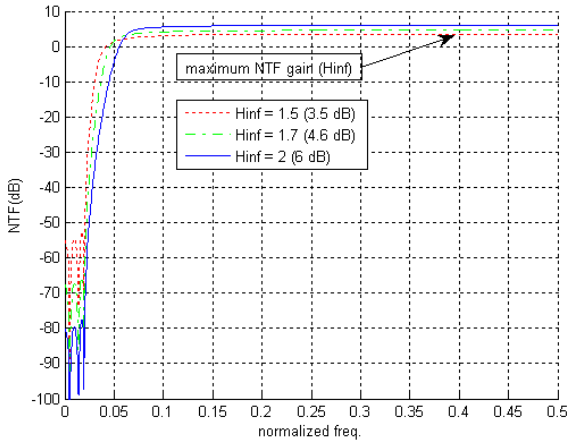


Figure 9. Raising the cutoff frequency of the ΣΔ modulator loop filter by increasing the maximum NTF gain of the ΣΔ modulator.

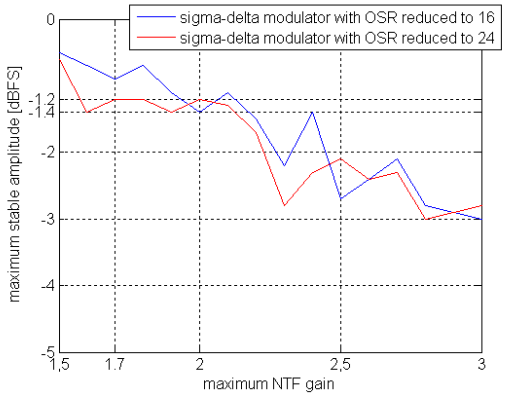


Figure 10. Maximum stable amplitude at ΣΔ modulator input as a function of max. NTF gain.

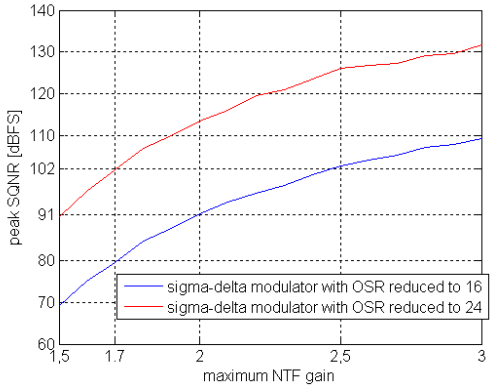


Figure 11. peak SQNR of the ΣΔ modulator output signal as a function of max. NTF gain.

performance reduction by coefficient quantization [3]. If the OSR is reduced from 32 to 16 the achievable peak SQNR drops from 106 dB to 67 dB, not fulfilling the specification. In order to improve the SQNR the cutoff frequency of the ΣΔ modulator loop filter must be raised. This can be done by increasing the maximum NTF gain H_{inf} of the ΣΔ modulator (see Fig. 9). However, at the same time, increase of the maximum NTF gain of the ΣΔ modulator reduces the MSA. The blue plot of Fig. 10 shows that at maximum NTF gain = 2 the MSA drops below the specification of -1.2 dBFS but the peak SQNR in the blue plot of Fig. 11 reaches only 91 dB, still below the specification. This shows that the reduction of the OSR from 32 to 16 brings the design out of specification and is not acceptable. Therefore if the DAC has to be optimized with respect to power by lowering the OSR factor, the OSR has to be lower than 32 but higher than 16 e.g. a factor that is not an integer power of two. This solution will be discussed in the next section.

IV. Introducing Interpolation by a Factor of 3

By introducing a stage performing interpolation by a factor of 3 the OSR can be reduced from 32 down to 24. In such case the ΣΔ modulator is 6th order with 3bit quantizer, OSR = 24 and maximum NTF gain H_{inf} = 1.5. However Fig.5 shows again that if H_{inf} = 1.5 is used as advised in [8] the modulator will reach only 89 dB peak SQNR, which is below the specification of Section II. This time increasing the maximum NTF gain helps to reach above the required 98 dB SQNR before the MSA drops below -1.2 dBFS (see Fig.10 red plot and Fig.11 red plot). H_{inf} = 1.7 is used for the optimized ΣΔ modulator. Simplified schematic of the ΣΔ modulator is in Fig. 2, Modulator_OSR24. A model of this design using fixed-point arithmetic has been built and simulated in Matlab. The model is transferable to VHDL. FFT spectrum of the ΣΔ modulator output signal is in Fig. 12. The coefficients of this optimized ΣΔ modulator can be found in Tab. V.

TABLE V. Coefficients of Modulator_OSR24 (Fig.2)

Coefficient	Value	Shift / Add	Adders
a_1	1/16	2^{-4}	0
a_2	0.1172	$2^{-3}-2^{-7}$	1
a_3	0.0977	$2^{-4}+2^{-5}+2^{-8}$	2
a_4	0.1094	$2^{-3}-2^{-6}$	1
a_5	0.1875	$2^{-3}+2^{-4}$	1
a_6	0.1563	$2^{-3}+2^{-5}$	1
b_1	1/16	2^{-4}	0
c_1	1/8	2^{-3}	0
c_2	1/8	2^{-3}	0
c_3	1/4	2^{-2}	0
c_4	1/2	2^{-1}	0
c_5	1/2	2^{-1}	0
c_6	3.8750	$2^{2}-2^{-3}$	1
g_1	0.0078	2^{-7}	0
g_2	0.0313	2^{-5}	0
g_3	0.0293	$2^{-5}-2^{-9}$	1

The IF stage performing interpolation by 3 can be either the last CIC filter (see IF_OSR24a, Fig. 3(b)) or the first IIR filter (see IF_OSR24b, Fig.3(c)). In the case of IF_OSR24a the first two stages are reused from IF_OSR32. The third and fourth stage is second order CIC filter. The FOM of the ΣΔ modulator and individual stages of the IF was again calculated according to Eq. 1 and can be seen in Tab. IV.

Tab. IV shows that the IF_OSR24a and the ΣΔ modulator Modulator_OSR24 have worse FOM than in the case of OSR = 32, but still by lowering the OSR from 32 to 24 the power consumption of the DPWM block and the main power consumer – the Class D PA is lowered by 25%, yielding an overall power reduction. Tab. IV also shows that the largest contribution to FOM of the IF_OSR24a comes from the last stage. The reason for this is that it performs oversampling by a factor of 3 which makes it more complex compared to the situation of IF_OSR32. To improve the FOM further the stage performing interpolation by a factor of 3 can be the first stage IIR filter instead of the last stage CIC filter (see IF_OSR24b, Fig. 3(c)).

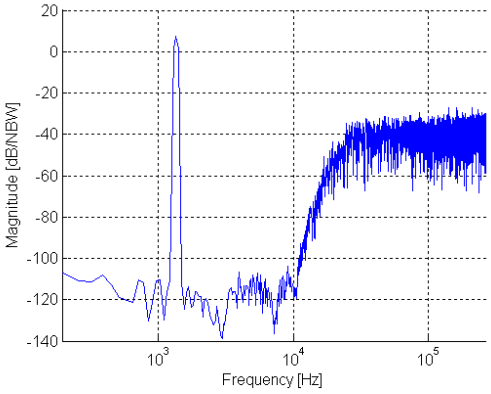


Figure 12. Output signal FFT spectrum of the ΣΔ modulator design Modulator_OSR24 (Fig.2). NBW = 1.8311e-04.

TABLE VI. Coefficients of the fist stage of IF_OSR24b (Fig. 3(c))

Coefficient	Value	Shift / Add	Adders
$\mathbf{a_{2,3}}$	0.9587	$2^{0}-2^{-5}-2^{-7}-2^{-9}-2^{-12}$	4
$\mathbf{a_{1,3}}$	0.8892	$2^{0}-2^{-3}+2^{-6}-2^{-9}+2^{-11}$	4
$\mathbf{a_{0,3}}$	0.7773	$2^{0}-2^{-2}+2^{-5}-2^{-8}$	3
$\mathbf{a_{2,2}}$	0.6592	$2^{-1}+2^{-3}+2^{-9}+2^{-7}+2^{-10}$	4
$\mathbf{a_{1,2}}$	0.5151	$2^{-1}+2^{-6}-2^{-11}$	2
$\mathbf{a_{0,2}}$	0.3652	$2^{-1}-2^{-3}-2^{-7}-2^{-9}$	3
$\mathbf{a_{2,1}}$	0.2207	$2^{-2}-2^{-5}+2^{-9}$	2
$\mathbf{a_{1,1}}$	0.1016	$2^{-4}+2^{-5}+2^{-7}$	2
$\mathbf{a_{0,1}}$	0.0303	$2^{-5}-2^{-10}$	1

In such case the first stage (IIR filter) is designed as a parallel connection of three second-order all-pass filter cells (see Fig. 12). The second-order all-pass filter cell used is in Fig.5. Coefficients of the first stage IIR filter can be found in Tab.VI. Again the FOM of the ΣΔ modulator and individual stages of the IF was calculated according to Eq. 1 and can be seen in Tab. IV.

Moreover a second order CIC filter can be used instead of the IIR filter in second stage (see IF_OSR24c, Fig. 3(d)). In this case the first stage of IF_OSR24b is reused and the remaining stages are second order CIC filters. The FOM of the ΣΔ modulator and individual stages of the IF was again calculated according to Eq. 1 and can be seen in Tab. IV.

For comparison a summary of the designs used in this work is

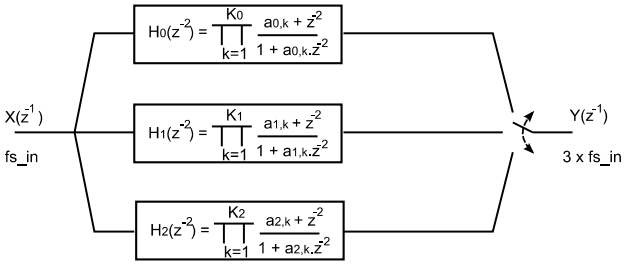


Figure 12. IIR filter using a parallel connection of three all-pass cells. Used as the first stage of IF_OSR24b (Fig. 3(c)).

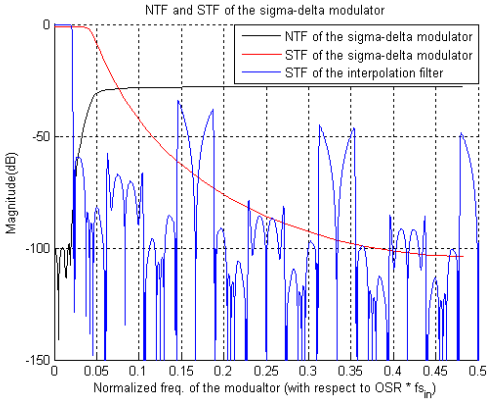
provided in Tab.VII. The transfer functions of the optimized Modulator_OSR24 and the three IFs of IF_OSR24b/c/d are in Fig.12. The peak-SQNR and the MSA of the Modulator_OSR24 (Fig.2), in the Matlab model using fixed-point arithmetic was the same, no matter which one of the three IFs was used. The peak of the IF transfer function reaching above the ΣΔ modulator NTF in the case of IF_OSR24b and IF_OSR24c is shown not to be a problem in the case of interpolation. However, in the case of decimation it could cause problems with down-folding of noise. In the caae of interpolation, the difference is only in FOM of the IFs and their pass-band ripple, favoring the IF_OSR24d despite of the larger pass-band ripple, as 0.6 dB is within the specification of a hearing-aid.

TABLE VII. COMPARISON OF THE ΣΔ MODULATOR AND IF DESGNS

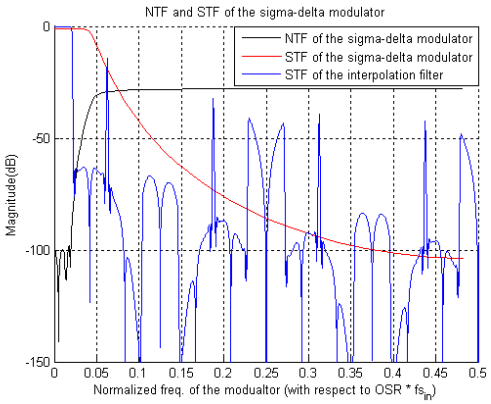
Design	IF_OSR32	IF_OSR24a	IF_OSR24b	IF_OSR24c
FOM (IF + ΣΔ modulator)	243	254	231	223.5
DPWM frequency	5.65 MHz	4.23 MHz	4.23 MHz	4.23 MHz
Class D PA switching frequency	705 kHz	529 kHz	529 kHz	529 kHz
IF pass-band ripple	0.5 dB	0.5 dB	0.5 dB	0.6 dB

V. CONCLUSION

This work shows that the optimized design with OSR factor other than integer power of two (OSR = 24) has 25% operating frequency reduction in the DPWM block and the class D PA compared to the original design. Thus these blocks consume 25% less power while the audio quality has been kept within specifications. Based on the FOM results, power is saved if the stage performing interpolation by a prime factor other than 2 is implemented as the first stage IIR filter rather than the last stage CIC filter. The combined power consumption of the IF and the ΣΔ modulator was reduced by 8%. In total considerable power savings were achieved. Therefore OSR factors other than integer powers of two should be considered when optimizing a ΣΔ modulator based DAC for low-voltage low-power portable audio applications.



(a)



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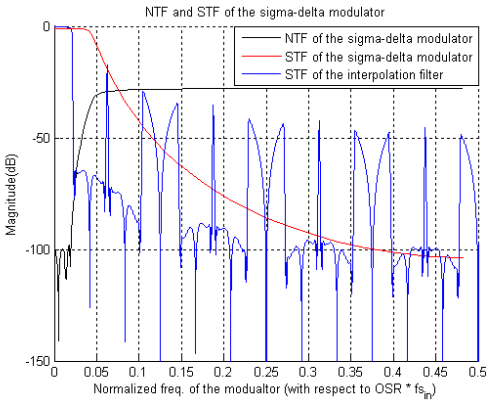

(c)

Figure 12. Transfer functions of the ΣΔ modulator Modulator_OSR24 (Fig.2) and the interpolation filter of (a) IF_OSR24a, (b) IF_OSR24b and (c) IF_OSR24c.

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