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Interval Robust Controller to Minimize Oscillations Effects Caused by Constant Power Load in a DC Multi-Converter Buck-Buck System

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ABSTRACT Multi-converter electronic systems are becoming widely used in many industrial applications; therefore, the stability of the whole system is a big concern to the real-world power supplies applications. A multi-converter system comprised of cascaded converters has a basic configuration that consists of two or more converters in series connection, where the first is a source converter that maintains a regulated dc voltage on the intermediate bus while remaining are load converters that convert the intermediate bus voltage to the tightly regulated outputs for the next system stage or load. Instability in cascaded systems may occur due to the constant power load (CPL), which is a behavior of the tightly regulated converters. CPLs exhibit incremental negative resistance behavior causing a high risk of instability in interconnected converters. In addition, there are other problems apart from the CPL, e.g., non-linearities due to the inductive element and uncertainties due to the imprecision of a mathematical model of dc–dc converters. Aiming to effectively mitigate oscillations effects in the output of source converter loaded with a CPL, in this paper, an interval robust controller, by linear programming based on Kharitonov rectangle, is proposed to regulate the output of source converter. Several tests were developed by using an experimental plant and simulation models when the multi-converter buck–buck system is subjected to a variation of power reference. Both simulation and experimental results show the effectiveness of the proposed controller. Furthermore, the performance indices computed from the experimental data show that the proposed controller outperforms a classical control technique.

INDEX TERMS Constant power load (CPL), multi-converter buck-buck system, parametric uncertainties, robust control based on Kharitonov rectangle, mitigation oscillations in multi-converter buck-buck system.

I. INTRODUCTION

Nowadays, multi-converter electronic systems are increasingly used in industrial applications due to their simplicity in structure, high power efficiency, low cost and high reliability [1], [2]. Some modern industries, whose processes demand high dynamic performance, have applied different types of converters for applications such as in variable speed DC motor drivers [3], renewable energy systems [4]–[6], transportation systems [7], [8], hybrid energy storage system [9], [10], communications systems [11]. In several of these applications, converters are controlled by switching through Pulse Width-Modulation (PWM) to transfer power from a power source to loads having a constant

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power characteristic. Because of switching, the converters have some inherent nonlinear behaviors, e.g., high frequency of switching, increasing harmonics in the system, current and voltage distortion, and instabilities occur due this effects [12], [13]. Therefore, it is a challenging task to ensure the stability, transient performance and higher efficiency of such converters [13].

A multi-converter system comprised of cascaded converters has a basic configuration that consists of two converters in series connection, where the first is a source converter while the second one is a load converter. The source converter maintains a regulated DC voltage on the intermediate bus, and the load converter transforms the intermediate bus voltage to tightly regulated outputs for the next system stage or load. In a cascaded buck converter system a large variety of dynamic and static interactions are possible and these can lead to irregular behavior of a converter, a group of converters or the whole system.

When a converter tightly regulates its output, it behaves as a Constant Power Load (CPL), thereby, in cascaded systems, load converter acts as a CPL when it is tightly regulated, its dynamic response is faster than the dynamic response of the source converter and its switching operation frequency is faster than source converter [14]. If the source converter is faster than the load converter, then it will compensate for disturbances and will regulate its output before the feedback loop of the load converter reacts to disturbances. Therefore, the load converter will not act as a perfect CPL for the feeding converter [15]–[21].

Different from a resistive load, CPL is a nonlinear load with variable negative impedance characteristics, i.e., the input current increases/decreases with a decrease/increase in its terminal voltage [15]–[21]. Because of the negative impedance characteristics of CPL, the system may become unstable, which may lead the system into oscillation or failure, and stress or damage the system equipment when feeding a CPL [17]–[21]. For this issue, CPLs are receiving more attention of researchers to give solutions aiming to cancel or compensate the negative effects of CPL.

Traditionally, the stability analysis and controller design of cascaded DC-DC converters is carried out by using the impedance criterion applied to averaged and linearized models [19]–[22]. The load converter under a tight control is conventionally modeled CPL for stability analysis or for controller design [19]–[22].

In order to mitigate the destabilizing effect of CPL, several methods have been proposed [23], such as passive and active damping [24]–[26], Lyapunov redesign control [8], nonlinear feedback linearization [27]–[29], Sliding Mode Control (SMC) [30]–[32], fuzzy control [33], Model Predictive Control (MPC) [34], [35] and robust control [36], [37]. However, there are other problems apart from the CPL, e.g., uncertainties present in the system parameters, which may lead to performance degradation [38]. In literature can be found control strategies applied to DC-DC power converters that deal with parametric uncertainties [39]–[41].

In research on dynamic systems with parametric uncertainties, the techniques that deal with this problem have been studied extensively over the last 40 years [42], [43].

To the best of the authors' knowledge, it seems that most papers published so far focus on mitigating the destabilizing effect of CPL without considering the uncertainties present in the system parameters. Therefore, studies reporting robust parametric methodologies for DC-DC converters feeding a CPL to mitigate oscillations effects caused by CPL still scarce in literature. However, in [39], a novel multivariable robust parametric technique was used for minimizing coupling effect in single inductor multiple output DC-DC converter operating in continuous conduction mode. Moreover, in [40] and [41], the use of Robust Parametric Control (RPC) techniques is proposed to stabilize oscillations at the output of a buck converter caused by parametric uncertainties.

Recently, the study developed in [44] addressed the important problem of parametric uncertainties in DC-DC converters by using μ analysis. However, their approach is focused only on a posterior analysis of system stability. The important subject of robust controller synthesis has been not addressed. In contrast, this paper is focused in the problem of robust controller synthesis, being thoroughly addressed from the onset, providing a practical and simple robust controller design algorithm with sufficient level of the detail in order to be easily implemented.

In this context, this paper proposes a robust controller based on RPC theory. The proposed controller is applied to source converter in order to mitigate oscillations effects due to CPL in multi-converter buck-buck (MCBB) system, aiming to reduce the control effort when the system is submitted to variation of power reference.

The main contributions of this work are briefly summarized in that following:

- By using the proposed robust technique, structured uncertainties of the type hyperbox, considering interval parametric type, are taking into account from the outset in the controller design process, incorporating available information about components (resistors, inductors, and capacitors) tolerances or defined by designer.
- The proposed robust technique leads to easy-to-implement controllers having fixed low-order structure, allowing the deployment of standard industry structures such as PID and Lead-Lag.
- Aiming to evaluate the performance of the proposed robust methodology under the instability problem caused by a CPL, the proposed robust methodology is compared with classical methodology carrying out several experimental and simulation tests. The performance index (ISE) is computed to analyze the control methodologies compared in this work. The results show the proposed methodology outperforms the other approach.

The remainder of this paper is organized as follows. Section II presents a brief review about the multi-converter buck-buck system; Section III presents a brief review about

parametric robust control background; Section IV proposes a mathematical model for multi-converter buck-buck system; Section V presents the proposed design methodology for interval robust controller; Section VI presents the experimental and simulation environment, describing the experiments to be performed in this paper; Section VII presents an assessment of the simulation results and experimental data. Finally, Section VIII presents the main conclusions.

II. SYSTEM DESCRIPTION AND PROBLEM FORMULATION

Multi-converter systems comprised of cascaded converters have a basic configuration that consists of two or more converters in series connection, where the first is a source converter that maintains a regulated DC voltage on the intermediate bus while remaining are load converters that transform the intermediate bus voltage to tightly regulated outputs for the next system stage or load.

In a cascaded buck converter a large variety of dynamic and static interactions are possible and these can lead to irregular behavior of a converter, a group of converters or the whole system.

A typical cascaded system with N DC-DC buck converters is shown in Fig. 1, where N represents the quantitative of buck converters.

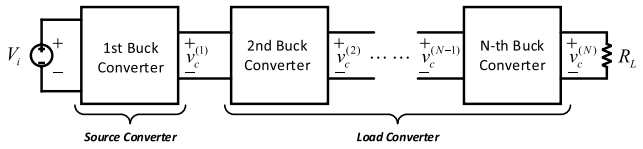


FIGURE 1. Buck Converters in series connection: Cascaded system with N-converters.

When a power converter tightly regulates its output, it behaves as a CPL [14]. CPLs have a negative incremental resistance, which tends to destabilize the system [19]–[21]. CPL approximation model describe the behavior at the input terminals of the load converter allows to capture its performance in a frequency range where its open-loop gain is high and an input voltage span where its controller is within its dynamic range.

A. BUCK CONVERTER WITH CONSTANT POWER LOAD

Cascaded buck converter system and its representation with CPL are shown in Figs. 2(a) and 2(b), respectively. It is assumed that the output of the load converter is tightly regulated as shown in Fig. 2(c).

CPLs introduce interesting nonlinear behavior to conventional buck-converter dynamics, but this behavior only exhibit above a certain voltage.

Fig. 3 shows the input "V-I" characteristics of load converter.

When the input voltage of the load converter, v_{c_1}, is lower than (v_{c_2}/d_2^{max}), the load converter behavior will be as the resistive load. Therefore, in this range of operation, load converter will be operates in a constant resistor zone (CRZ).

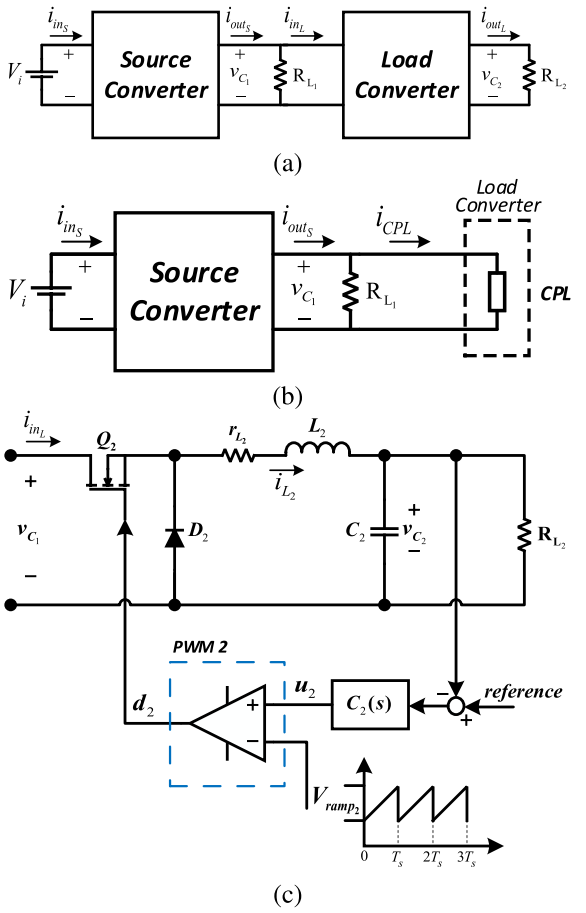


FIGURE 2. Multi-converter buck-buck system. (a) Cascaded system with two power stages. (b) Source converter loaded by a CPL. (c) Tightly regulated load converter.

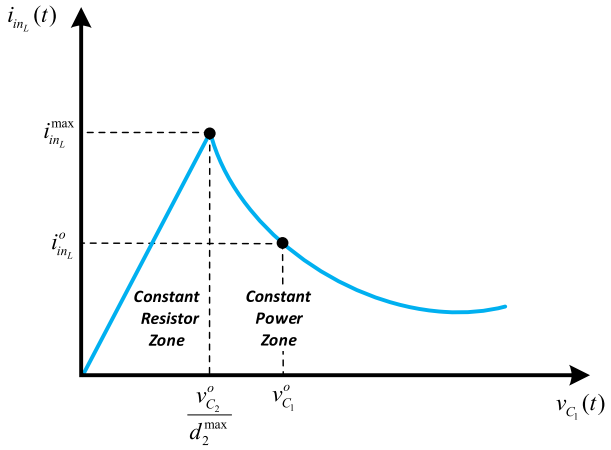


FIGURE 3. Input "V–I" characteristics of the CPL.

On the other hand, when v_{c_1} is higher than (v_{c_2}/d_2^{max}), load converter behavior will be as a CPL, thus, load converter will be operate in a constant power zone (CPZ).

Where $v_{c_1}^o$ is the input DC voltage of load converter; $v_{c_2}^o$ is the tightly regulated output voltage of load converter; $i_{in_L}^o$ is the input operation current of load converter; $i_{in_L}^{max}$ is the maximum input current of load converter; d_2^{max} is the maximum

operating duty cycle of load converter; and P_o is the operating power of CPL.

In order to maintain a constant power level, in a DC-DC converter when it acts as a CPL, input current increases when input voltage decreases, and vice versa, thus, the product of the input current and input voltage of the load converter, (i.e., $P_o = i_{in_L} v_{c_1}$) is a constant. The instantaneous value of the load impedance is positive (i.e., $v_{c_1}/i_{in_L} > 0$). However, the incremental impedance is always negative (i.e., $\Delta v_{c_1}/\Delta i_{in_L} < 0$) due to once appearing any disturbance, thus operating point will leave from previous point and never return. This negative incremental impedance has a negative impact on the power quality and stability of system. Fig. 4 shows the negative incremental impedance behavior of CPL.

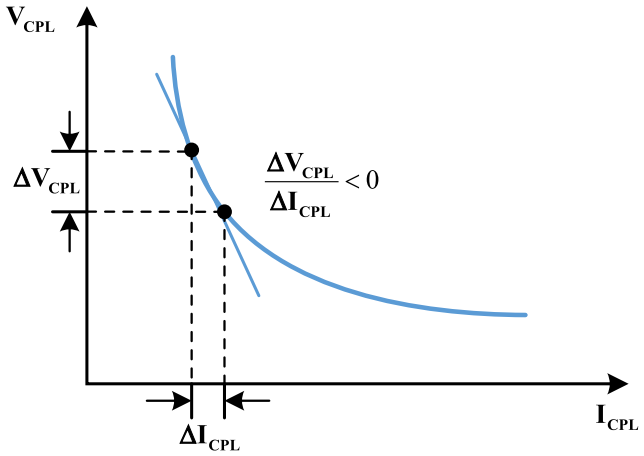


FIGURE 4. The negative incremental impedance behavior of CPL.

B. STABILITY ANALYSIS OF STUDIED SYSTEM

The system, showed in Fig. 2(b), is used to show the instability of a DC-DC converter feeding a CPL. To obtain the large-signal behavior of the load converter, the CPL is represented by a dependent current source [14], $i_{CPL} = P_o/v_{c_1}$, so the instantaneous current drawn from source converter is given by

$$\begin{aligned} i_{out_s}(t) &= i_{R_{L_1}}(t) + i_{CPL}(t) \\ i_{out_s}(t) &= \frac{v_{c_1}(t)}{R_{L_1}} + \frac{P_o}{v_{c_1}(t)} \\ i_{out_s} &= i_{L_1} \end{aligned} \tag{1}$$

Depending on switching of the source converter, the large-signal model of the converter in continuous conduction mode can be obtained based on the following equations:

$$\begin{cases} \dfrac{di_{L_1}}{dt} = -\dfrac{r_{L_1}}{L_1} i_{L_1} + \dfrac{1}{L_1}\left(V_i - v_{c_1}\right) \\ \dfrac{dv_{c_1}}{dt} = \dfrac{1}{C_1} i_{L_1} - \dfrac{1}{C_1}\left(\dfrac{v_{c_1}}{R_{L_1}} + \dfrac{P_o}{v_{c_1}}\right), \end{cases} \quad 0 < t < d_1 T_{s_1} \tag{2}$$

$$\begin{cases} \dfrac{di_{L_1}}{dt} = -\dfrac{r_{L_1}}{L_1} i_{L_1} + \dfrac{1}{L_1}\left(-v_{c_1}\right) \\ \dfrac{dv_{c_1}}{dt} = \dfrac{1}{C_1} i_{L_1} - \dfrac{1}{C_1}\left(\dfrac{v_{c_1}}{R_{L_1}} + \dfrac{P_o}{v_{c_1}}\right), \end{cases} \quad d_1 T_{s_1} < t < T_{s_1} \tag{3}$$

where d_1 and T_{s_1} are the duty cycle and switching period of the source converter, respectively. L_1, r_{L_1}, C_1 and R_{L_1} are the plant parameter of source converter. V_i is the input DC voltage of source converter. P_o is the output power of load converter that is constant. $i_{out_s} = i_{L_1}$.

Using the state-space averaging method [14], [20], the buck converter dynamics can be written as:

$$\begin{cases} \dfrac{di_{L_1}}{dt} = -\dfrac{r_{L_1}}{L_1} i_{L_1} + \dfrac{1}{L_1}\left(V_i d_1 - v_{c_1}\right) \\ \dfrac{dv_{c_1}}{dt} = \dfrac{1}{C_1} i_{L_1} - \dfrac{1}{C_1}\left(\dfrac{v_{c_1}}{R_{L_1}} + \dfrac{P_o}{v_{c_1}}\right) \end{cases} \tag{4}$$

Consider small perturbations in the state variables due to small disturbances in the input voltage and duty cycle

$$\begin{cases} V_i = \bar{V}_i + \tilde{V}_i \\ d_1 = \bar{d}_1 + \tilde{d}_1 \\ v_{c_1} = V_{C_1} + \tilde{v}_{c_1} \\ i_{L_1} = I_{L_1} + \tilde{i}_{L_1} \end{cases} \tag{5}$$

where, $\bar{V}_i$, $\bar{d}_1$, V_{C_1} and I_{L_1} are the average values of V_i, d_1, v_{c_1} and i_{L_1}, respectively.

Substituting (5) in (4) and neglecting the internal resistance of the inductor to simplify the calculations, the buck converter model becomes

$$\begin{cases} \dfrac{d\tilde{i}_{L_1}}{dt} = \dfrac{1}{L_1}\left(\bar{V}_i \tilde{d}_1 + \bar{d}_1 V_i - \tilde{v}_{c_1}\right) \\ \dfrac{d\tilde{v}_{c_1}}{dt} = \dfrac{1}{C_1}\left(\tilde{i}_{L_1} - \dfrac{P_o \tilde{v}_{c_1}}{V_{c_1}^2}\right) \end{cases} \tag{6}$$

Note that the following approximation was made in (6), $\bar{V}_i \gg \tilde{V}_i$ and $V_{c_1} \gg \tilde{v}_{c_1}$.

Therefore, the transfer function of the buck converter loaded with a CPL can be obtained from (6) as follows:

$$G(s) = \frac{\tilde{v}_{c_1}}{\tilde{V}_i} = \frac{\dfrac{\bar{d}_1}{L_1 C_1}}{s^2 - \left(\dfrac{P_o}{C_1 V_{c_1}^2}\right) s + \dfrac{1}{L_1 C_1}} \tag{7}$$

Due to CPL, the transfer function in (7) have poles in the right half-plane, thus, the buck converter, when it is loaded with a CPL, is unstable.

In (4), the nonlinear coefficient introduced by a CPL and the constraints on the state variables make the equation difficult to solve. Therefore, any unwanted dynamics introduced in (4) cannot be damped, so trajectories will tend to have cycling or unbounded behaviors [20], [21].

The simulation results in Fig. 5 confirm the intuitive behavior suggested by (4).

The system is analyzed by a phase-plane analysis, solving (plotting) the system differential equations giving

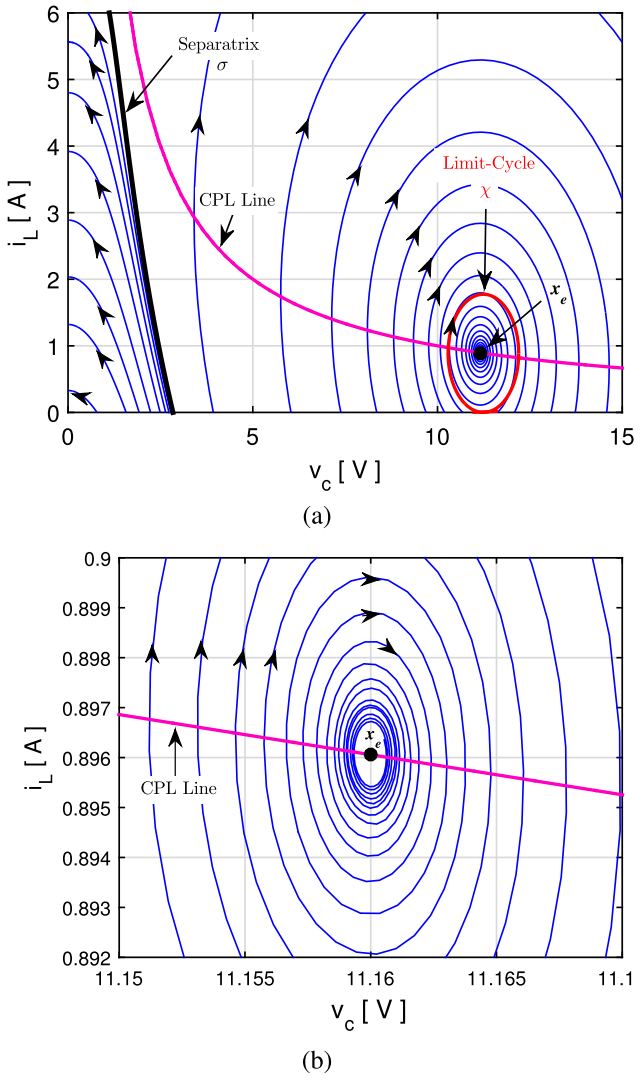


FIGURE 5. Phase-portrait obtained by simulating. (a) Phase-portrait of source converter loaded with a CPL. (b) Zoomed area near the operating condition.

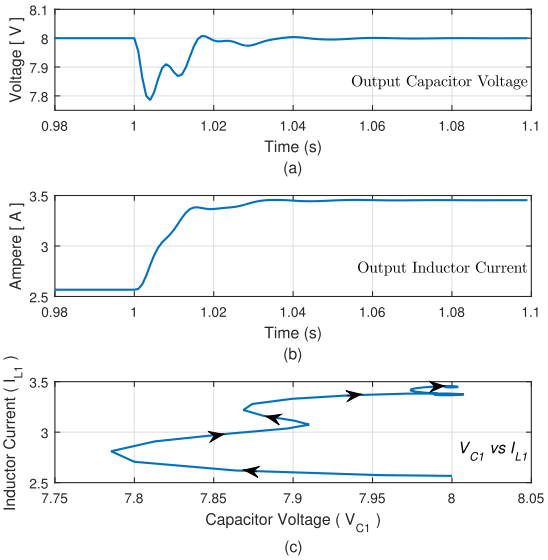


FIGURE 6. Closed-Loop system subjected to a variation of power CPL of 10 W. (a) Capacitor Voltage of Source Converter. (b) Inductor Current of Source Converter. (c) Phase-Plane of v_{c_1} *vs* i_{L_1} during the variation of power CPL.

an insight about how the system dynamics evolve with time [16], [20], [21].

The phase-portrait of source converter feeding a CPL (cf. Fig. 5) is simulated with the following parameters: $V_i = 15\ V$, $L_1 = 2mH$, $C_1 = 2000\ mF$, $P_o = 10\ W$, and $d_1 = 0.744$.

The phase-portrait (Fig. 5(a)) shows the state plane divided into two regions with distinct characteristics [16], [20]: one to the left of a separatrix σ, in which the bus voltage v_{c_1} collapses being an unstable region, and the other to the right of σ, in which v_{c_1} presents significant and undesirable oscillations because of the existence of a limit-cycle χ [16], [20]. These oscillations are caused by energy imbalances, which occur during the transient period when LC input filter and output powers are not equal as it occurs in steady state. Therefore, without resistive components in the system, which can dissipate the energy imbalance, this energy will resonate among the energy storage elements in the system. This oscillatory behavior is also observed when attempting regulation if the controller is not adequately designed [16].

Fig. 6 shows voltage and current oscillations when a buck converter is subjected ($t = 1\ s$) to a variation of power CPL (ΔP_o) of 10 W with $V_i = 15\ V$, $L_1 = 2mH$, $C_1 = 2000\ mF$, $P_o = 5\ W$, regulated for an output voltage of 8 V with a PID controller with integral gain of 2.41, proportional gain of 0.011 and derivative gain of $1.05e^{-5}$. Load converter acts as a CPL due to the incremental negative resistance behavior during the variation of CPL power as shown in Fig. 6(c).

III. ROBUST PARAMETRIC CONTROL BACKGROUND

Mathematical models naturally present errors that are neglected, depending on the type of study. An important consideration in model-based control systems is to keep the system stable, subject to parametric variations. However, generally in the classic controller design, models that ignore uncertainties are used [45]. In this way, it is common to use a nominal transfer function for the controller design. Although the controller is developed based on a nominal transfer function, the real system must be stable for all kinds of transfer functions that represent the whole set of uncertainties.

Thereby, uncertainty of a system can be classified as unstructured (non-parametric uncertainty) and structured (parametric uncertainty) [38], [43].

A. ROBUST STABILITY

A system with interval parametric uncertainties is generally described by uncertain polynomials $B(s, b)$ and $A(s, a)$, restricted within pre-specified closed real intervals,

as shown in (8) [38].

$$G(s,b,a)=\frac{B(s,b)}{A(s,a)}=\frac{\sum_{i=0}^{m}\left[b_i^-,b_i^+\right]s^i}{\sum_{i=0}^{n}\left[a_i^-,a_i^+\right]s^i} \tag{8}$$

Many robust stability tests under parametric uncertainty are based on analysis of uncertain characteristic polynomial assumed as an interval polynomial family [38], such as

$$P(s,p)=\sum_{i=0}^{n}\left[p_i^-,p_i^+\right]s^i \tag{9}$$

Polynomial $P(s,p)$ is stable if and only if all its roots are contained on the Left Half-Plane (LHP) of the s-plane. Then, $P(s,p)$ is robustly stable if and only if all its polynomials are stable for a set of operating point different from the nominal operating point within its minimum and maximum limits [46]. However, it is not necessary to check stability of an infinite number of polynomials to guarantee the robust stability. Robust stability can be checked through the analysis of four polynomials within $P(s,a)$; these polynomials can be found by Kharitonov Theorem [38], [47].

B. KHARITONOV STABILITY THEOREM

The Kharitonov Theorem is a test used in robust control theory to evaluate the stability of a dynamic system whose parameters vary within a closed real interval as follows:

$$\delta(s)=\delta_0+\delta_1 s+\delta_2 s^2+\delta_3 s^3+\cdots+\delta_n s^n \tag{10}$$

where, the coefficient vector $\bar{\delta}=[\delta_0,\delta_1,\delta_2,\delta_3,\cdots,\delta_n]$ ranges over a box:

$$\Delta=\left[\delta_0^-,\delta_0^+\right]\times\left[\delta_1^-,\delta_1^+\right]\times\cdots\times\left[\delta_n^-,\delta_n^+\right] \tag{11}$$

where, δ_n^- and δ_n^+ represent the lower and upper limit respectively. Therefore, the Kharitonov polynomials are defined as:

$$\begin{aligned}
K_1(s)&=\delta_0^-+\delta_1^- s+\delta_2^+ s^2+\delta_3^+ s^3+\delta_4^- s^4+\delta_5^- s^5+\delta_6^+ s^6+\cdots\\
K_2(s)&=\delta_0^-+\delta_1^+ s+\delta_2^+ s^2+\delta_3^- s^3+\delta_4^- s^4+\delta_5^+ s^5+\delta_6^+ s^6+\cdots\\
K_3(s)&=\delta_0^+ +\delta_1^- s+\delta_2^- s^2+\delta_3^+ s^3+\delta_4^+ s^4+\delta_5^- s^5+\delta_6^- s^6+\cdots\\
K_4(s)&=\delta_0^+ +\delta_1^+ s+\delta_2^- s^2+\delta_3^- s^3+\delta_4^+ s^4+\delta_5^+ s^5+\delta_6^- s^6+\cdots
\end{aligned} \tag{12}$$

Theorem 1 (Robust Stability): The interval polynomial family delimited by Δ is robustly stable if and only if its four Kharitonov polynomials are stable [38], [47], i.e., all roots of the interval polynomial are in the SPL of the complex plane [48].

C. ROBUST CONTROLLER DESIGN BY INTERVAL POLE-PLACEMENT

To design the controller, a region of uncertainty is previously defined, considering that the uncertainty is contained in the parameter variation of the plant-model. The controller is designed according to Keel and Bhattacharyya [45], associated with a linear goal programming formulation, which will lead to a set of linear inequality constraints.

Consider $G(s,p)$ a uncertain plant of order n and $C(s,x)$ the controller of order r, defined in (13) and (14) respectively.

$$G(s,p)=\frac{n(s)}{d(s)}=\frac{b_1 s^{n-1}+\cdots+b_{n-1}s+b_n}{s^n+a_1 s^{n-1}+\cdots+a_{n-1}s+a_n} \tag{13}$$

$$C(s,x)=\frac{n_c(s)}{d_c(s)}=\frac{x_0 s^r+x_1 s^{r-1}+\cdots+x_{r-1}s+x_r}{s^r+y_1 s^{r-1}+\cdots+y_{r-1}s+y_r} \tag{14}$$

Let p be the vector of parameters that represent the plant and x the vector of real parameters representing the controller defined in (15) and (16) respectively. In addition, p^o represents the nominal value of plant parameters defined in a hyperbox region of uncertainties.

$$p:=[\,b_1\;\;b_2\;\;\cdots\;\;b_{n-1}\;\;b_n\;\;a_1\;\;a_2\;\;\cdots\;\;a_{n-1}\;\;a_n\,] \tag{15}$$

$$p:=[\,x_0\;\;x_1\;\;\cdots\;\;x_{r-1}\;\;x_r\;\;y_1\;\;y_2\;\;\cdots\;\;y_{r-1}\;\;y_r\,] \tag{16}$$

According to [45], the solution of the Diophantine equation (17) summarizes the pole-placement problem

$$d(s)=d(s)d_c(s)+n(s)n_c(s) \tag{17}$$

where, $d(s)$ is the closed-loop characteristic polynomial. Therefore, the parameters of the closed-loop characteristic polynomial are represented as follows:

$$d_i=d_i(x,p) \tag{18}$$

Assuming that the desired dynamic of closed-loop system is represented by

$$\Delta_d(s)=s^i+\phi_1 s^{i-1}+\cdots+\phi_{i-1}s+\phi_i \tag{19}$$

where, ϕ_i represent the parameters of the closed-loop desired polynomial.

In order to tune the controller, the closed-loop polynomial parameters are compared with the desired closed-loop polynomial, which represent the desired dynamics of the system follow as

$$d_i(x,p^o)=\phi_i,\quad i=1,2,\ldots,l \tag{20}$$

This problem can be written in its matrix format, presenting the following relationship [38], (21), as shown at the bottom of the next page.

When the system is subject to parametric uncertainties, the controller performance may deteriorate. Therefore, the controller must guarantee robust performance within an acceptable region of closed-loop parameters variation, so that the closed-loop poles are located in a certain region. Thereby, a desired region is defined as follows:

$$\Phi:=\left\{\phi_i^-\le\phi_i\le\phi_i^+\right\} \tag{22}$$

Therefore, according to [46], replacing the parameters of (22) in (20), it is possible to formulate a linear inequalities set, which restricted the controller and desired polynomial coefficients in the predefined intervals, as shown in (23). Thus, the closed-loop system has its poles within the roots

space of interval-desired polynomial, ensuring the robust stability [49].

$$\phi_i^- \leq d_i(x,p) \leq \phi_i^+, \quad \forall i = 1,2,\ldots,l \tag{23}$$

The robust design problem is summarized in the choice of X (if possible) to satisfy the set of inequalities (23) for all $p \in P$. The aforementioned robust performance control design problem for the pre-established conditions can be rewritten as the following optimization problem:

$$\begin{aligned} X &= \arg\left(\min f(X)\right) \\ s.t. &\begin{bmatrix} A(p) \\ -A(p) \end{bmatrix} X \leq \begin{bmatrix} B(\phi^+) \\ -B(\phi^-) \end{bmatrix} \end{aligned} \tag{24}$$

where, $f(X)$ is a linear cost function that must be built and minimized according to the control goals. In this study, the cost function $f(X)$ has been chosen to be the sum of the elements of vector of the controller parameter X, such as suggested by Keel and Bhattacharyya [45] and Bhattacharyya *et al.* [50].

IV. MATHEMATICAL MODEL FOR MULTI-CONVERTER BUCK-BUCK SYSTEM

In order to represent the dynamical behavior of DC Multi-converter buck-buck System, a small signal approximation model is employed as an effective mathematical model.

Fig. 7 represents the DC MCBB system with two decoupled outputs, V_{C_1} and V_{C_2}, such that $V_{C_2} < V_{C_1}$, and a topology employed to control the system. The main characteristic of this system is that it has two DC-DC buck converters connected in series where the output of the first one converter is the DC source of the second one.

Each converter can be considered an independent subsystem; therefore, the dynamics of the system can be simplified to the analysis of two independent converters. The dynamic behavior of buck converter, in Continuous Conduction Mode (CCM), can be found in [40] and [41].

The following equations involving the state variables of buck converters are written based on the analysis of their

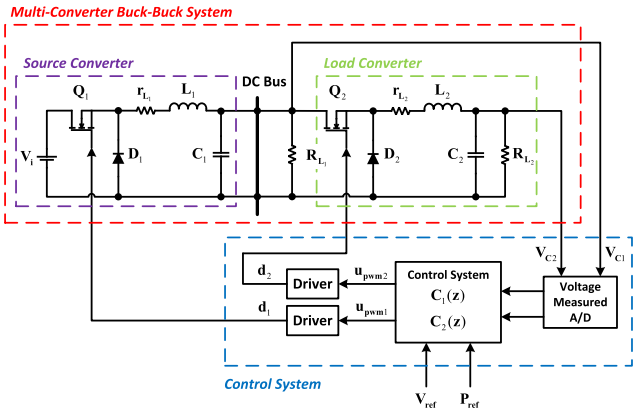


FIGURE 7. Multi-Converter Buck-Buck System.

respective equivalent circuits.

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = d_1 V_i - V_{C_1} - r_{L_1} i_{L_1} \\ C_1 \dfrac{dV_{C_1}}{dt} = i_{L_1} - \dfrac{V_{C_1}}{R_{L_1}} \\ L_2 \dfrac{di_{L_2}}{dt} = d_2 V_{C_1} - V_{C_2} - r_{L_2} i_{L_2} \\ C_2 \dfrac{dV_{C_2}}{dt} = i_{L_2} - \dfrac{V_{C_2}}{R_{L_2}} \end{cases} \tag{25}$$

The duty cycle d_1 regulates the output voltage (V_{C1}) of source converter, i.e. the DC bus voltage, and the duty cycle d_2 regulates the output power of load converter, i.e., ${V_{C2}}^2/R_{L2}$. Thereby, the outputs of system are described below.

$$\begin{aligned} y_1 &= \begin{bmatrix} 0 & V_{C_1} \end{bmatrix} \\ y_2 &= \begin{bmatrix} 0 & \frac{{V_{C2}}^2}{R_{L2}} \end{bmatrix} \end{aligned} \tag{26}$$

Assuming that the electronic switches and diodes are ideal, the linearized model that describes the dynamic behavior of

$$\underbrace{\left[\begin{array}{ccccc|ccccc} [b_1] & 0 & \cdots & 0 & 0 & 1 & 0 & \cdots & 0 & 0 \\ [b_2] & [b_1] & \ddots & \vdots & 0 & [a_1] & 1 & \ddots & \vdots & 0 \\ \vdots & [b_2] & \ddots & 0 & \vdots & \vdots & [a_1] & \ddots & 0 & \vdots \\ [b_{m-1}] & \vdots & \ddots & [b_1] & 0 & [a_{n-1}] & \vdots & \ddots & 1 & 0 \\ [b_m] & [b_{m-1}] & \ddots & [b_2] & [b_1] & [a_n] & [a_{n-1}] & \ddots & [a_1] & 1 \\ 0 & [b_m] & \ddots & \vdots & [b_2] & 0 & [a_n] & \ddots & \vdots & [a_1] \\ \vdots & 0 & \ddots & [b_{m-1}] & \vdots & \vdots & 0 & \ddots & [a_{n-1}] & \vdots \\ 0 & \vdots & \ddots & [b_m] & [b_{m-1}] & 0 & \vdots & \ddots & [a_n] & [a_{n-1}] \\ 0 & 0 & \cdots & 0 & [b_m] & 0 & 0 & \cdots & 0 & [a_n] \end{array}\right]}_{\text{A}} \underbrace{\left[\begin{array}{c} x_0 \\ x_1 \\ \vdots \\ x_{r-1} \\ x_r \\ - \\ y_0 \\ y_1 \\ \vdots \\ y_{r-1} \\ y_r \end{array}\right]}_{\text{X}} = \underbrace{\left[\begin{array}{c} [\phi_1] - [a_1] \\ [\phi_2] - [a_2] \\ \vdots \\ [\phi_n] - [a_n] \\ [\phi_{n+1}] \\ \vdots \\ [\phi_m] \end{array}\right]}_{\text{B}} \tag{21}$$

the converter is represented as follows:

$$\frac{V_{C_1}(s)}{V_i(s)} = \frac{\frac{d_1^o}{L_1C_1}}{s^2 + \left(\frac{1}{R_{L_1}C_1} + \frac{r_{L_1}}{L_1}\right)s + \left(\frac{1}{L_1C_1} + \frac{r_{L_1}}{R_{L_1}L_1C_1}\right)} \quad (27)$$

$$\frac{V_{C_2}(s)}{V_{C_1}(s)} = \frac{2\left(\frac{d_2^o}{L_1C_1}\right)\left(\sqrt{\frac{P_o}{R_{L_2}}}\right)}{s^2 + \left(\frac{1}{R_{L_2}C_2} + \frac{r_{L_2}}{L_2}\right)s + \left(\frac{1}{L_2C_2} + \frac{r_{L_2}}{R_{L_2}L_2C_2}\right)} \quad (28)$$

where, d_1^o and d_2^o are operational point for duty cycle of outputs 1 and 2, respectively. P_o is the operating power of output 2.

The nominal values of the parameters, operational point and the meaning of each symbol in (27) and (28) are presented in Table 1.

TABLE 1. Values for the physical parameters of the DC multi-converter buck-buck board test system.

Par.	Uni.	Var. (%)	Nom. Val.	Description
V_i	V	15	15.0	Source input voltage
R_{L_1}	Ω	50	4.0	Loading at output 1
R_{L_2}	Ω	–	4.0	Loading at output 2
C_1	μF	10	2000	Capacitor at output 1
C_2	μF	–	2200	Capacitor at output 2
L_1	mH	10	2.0	Inductor at source subsystem
L_2	mH	–	2.0	Inductor at CPL
r_{L_1}	Ω	15	0.05	Internal resistance of L_1
r_{L_2}	Ω	–	0.05	Internal resistance of L_2
d_1^o	%	–	74.4	Operating duty cycle of output 1
d_2^o	%	–	63.2	Operating duty cycle of output 2
$V_{C_1}^o$	V	–	8.0	Output voltage of source subsystem
P_{CPL}	p.u.	–	0.3	Output power of CPL
f_{sw1}	kHz	–	1.0	Switching frequency of duty cycle d_1
f_{sw2}	kHz	–	5.0	Switching frequency of duty cycle d_2
P_{max}	W	–	20.0	Maximum power at CPL
f_s	kHz	–	1.0	Sampling frequency

V. ROBUST CONTROLLER DESIGN METHODOLOGY

This section presents a method to design a fixed order robust controller that provides robust stability and performance for a predetermined uncertain family of models with parameters bounded in a hyperbox region. This study only considers uncertainties in the parameters of source converter (see Table 1) because oscillations, caused by a CPL, occur in the LC filter of the converter. Therefore, only output 1 will be regulated by a robust controller. A classic controller, based on Classical Pole-Placement (CPP), will regulate output 2. The robust controller is designed according to presented by Bhattacharyya *et al.* [50]. In this paper, this method is denominated as "Control Based on Kharitonov's Rectangle (CKR". The proposed controller must ensure robust stability and performance for the entire region of parametric variation.

Fig. 8 illustrates a simplified flowchart of the methodology for designing the robust controller. The process starts in step 1, by defining the nominal plant (20) with its operating conditions; in step 2, the box region of uncertainties is built based on a previously specified uncertainty range delimited by the designer. Since box region of uncertainties influence on the delimitation of the convex region where the control gains will be determined, the correct selection of this box region is an important point to have success of the proposed methodology. The lower-and upper-bound of each parameter are provided in Table 1.

The characteristic closed-loop polynomial is obtained (Step 3) by using the controller parameter and the nominal model (20) selected in step 1, then by replacing the nominal and interval values, defined in step 2, the interval closed-loop polynomial is calculated.

The controller function depends on the chosen control structure. In this work, a controller with a PID structure is selected. The transfer function is given below.

$$C_{PID}(s) = \frac{U(s)}{E(s)} = \frac{k_d s^2 + k_p s + k_i}{s} \quad (29)$$

For simplification, transfer function presented in (20) can be represented as follows:

$$G_1(s) = \frac{V_{C1}(s)}{V_i(s)} = \frac{b_0}{s^2 + a_1 s + a_0} \quad (30)$$

where

$$a_1 = \left(\frac{1}{R_{L_1}C_1} + \frac{r_{L_1}}{L_1}\right) \quad (31)$$

$$a_0 = \left(\frac{1}{L_1C_1} + \frac{r_{L_1}}{R_{L_1}L_1C_1}\right) \quad (32)$$

$$b_0 = \frac{d_1^o}{L_1C_1} \quad (33)$$

Finally, closed-loop interval polynomial is obtained by using the controller parameters (22) and plant parameters (23).

$$P_{cl}(s) = s^3 + \left[\varphi_2^-, \varphi_2^+\right]s^2 + \left[\varphi_1^-, \varphi_1^+\right]s + \left[\varphi_o^-, \varphi_o^+\right] \quad (34)$$

The nominal parameters of P_{cl} depend on the parameters of source converter (cf. Table 1), resulting in the following nominal parameters:

$$\varphi_0^o = b_0 k_i \quad (35)$$

$$\varphi_1^o = a_0 + b_0 k_p \quad (36)$$

$$\varphi_2^o = a_1 + b_0 k_d \quad (37)$$

The lower- and upper-limits for these parameters must be computed by replacing the nominal and interval presented in Table 1 by using interval analysis for (23)-(26). The region defined by the closed-loop interval polynomial of (27) must be inside the region determined by the desired performance polynomial (chosen in Step 4). Particularly, it was chosen for a maximum settling time of less than 0.15 sec and a damping factor greater than 0.9, defining the desired performance region (38). Note that an auxiliary pole must be added that does not affect the desired dynamics of system to satisfy (20).

$$\Phi = s^3 + [\phi_2]s^2 + [\phi_1]s + [\phi_o] \quad (38)$$

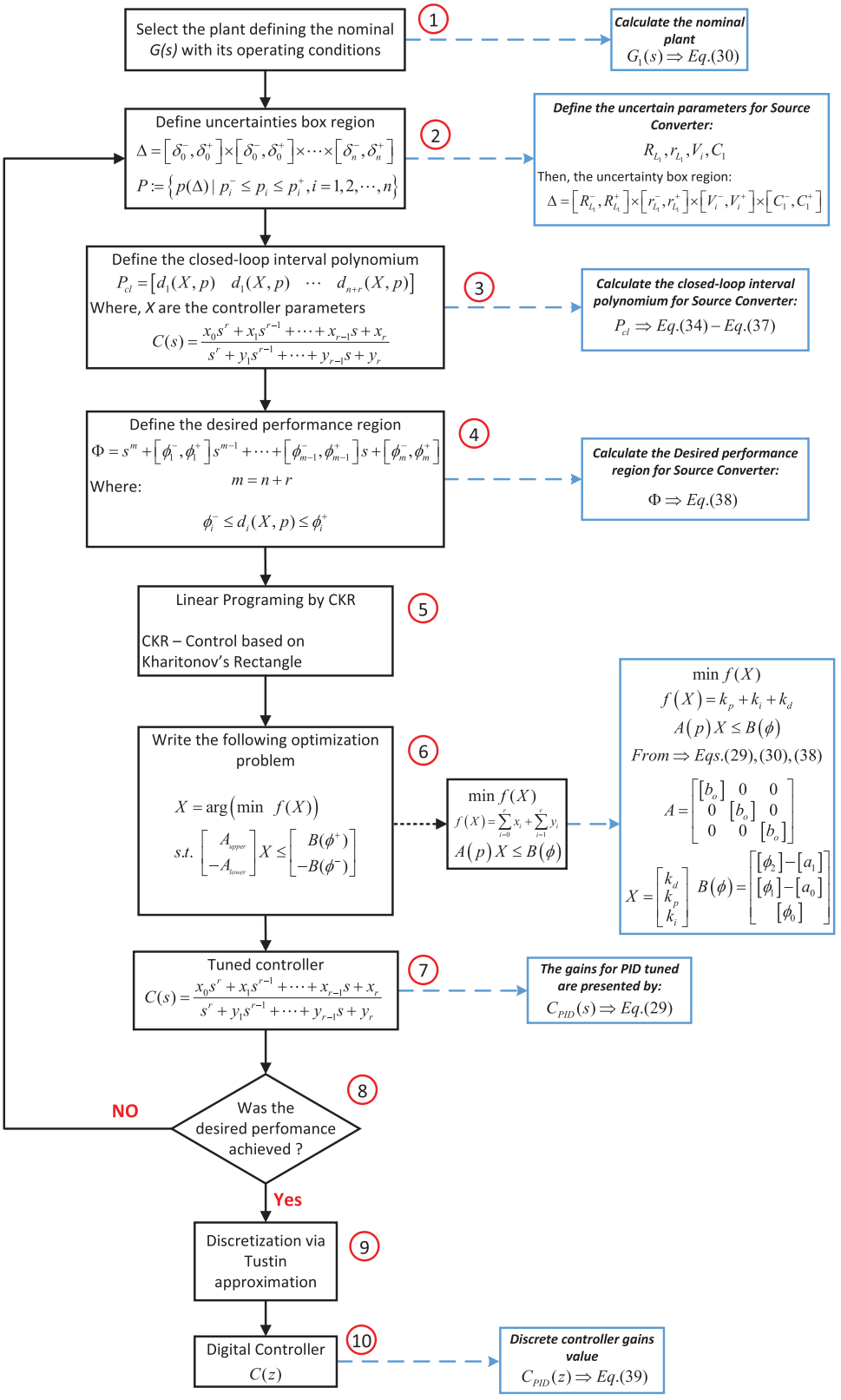


FIGURE 8. Flowchart of methodology for designing of robust controller.

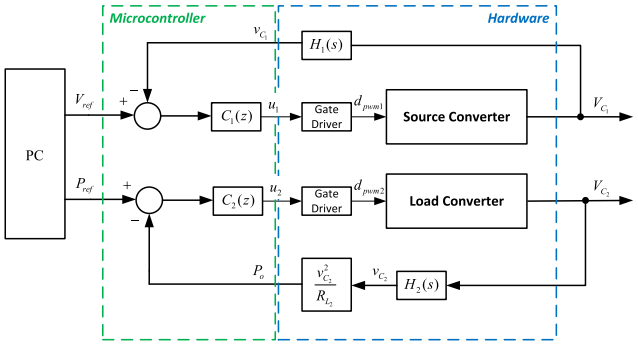


FIGURE 9. Block diagram of the developed hardware system and actuation of the system control signal.

The optimization problem is selected in step 5 and solved in step 6, where the cost function is defined as the sum of controller gains and the parameter vector X. The feasible solution X^* (obtained in step 6) is used to set the control structure (step 7).

The performance condition is verified in step 8 in case of achieving it, advance to step 9, if not, go back to step 2, where you must redefine the system's uncertainties.

In order to obtain a discrete equivalent controller the Tustin Method [51] was used (Step 9). A sampling period of 1ms was chosen in order to comply with a sampling frequency between 2 to 10 greater than the frequency band of the system.

$$C_{PID}(z) = \frac{h_0 z^2 + h_1 z + h_2}{z^2 - 1} \tag{39}$$

VI. DESCRIPTION OF TEST ENVIRONMENTS

A. DESCRIPTION OF THE MULTI-CONVERTER BUCK-BUCK SYSTEM TEST BOARD

Fig. 9 presents a control-generalized block diagram applying to multi-converter buck-buck system using filters in the outputs of system to avoid that ripples of the outputs interfere in the performance of the designed controller. These filters, $H_1(s)$ and $H_2(s)$, must be designed so that they do not affect the system dynamics. Two SISO controllers are used to regulate system outputs.

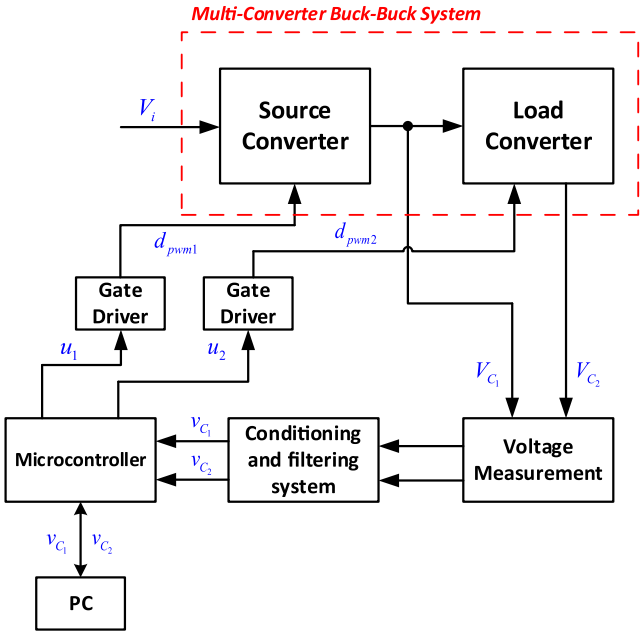
Fig. 10(a) presents a diagram of the subsystems used in the experimental tests and Fig. 10(b) shows the developed laboratory setup.

A DC Multi-Converter buck-buck (Fig. 10(b)) is developed for the experimental evaluation of the proposed control approach. The controller has been implemented by using a 32-bit ARM core microcontroller AT91SAM3X8E (Fig. 10(b)). The desired set point values are provided by a microcomputer system via USB communication.

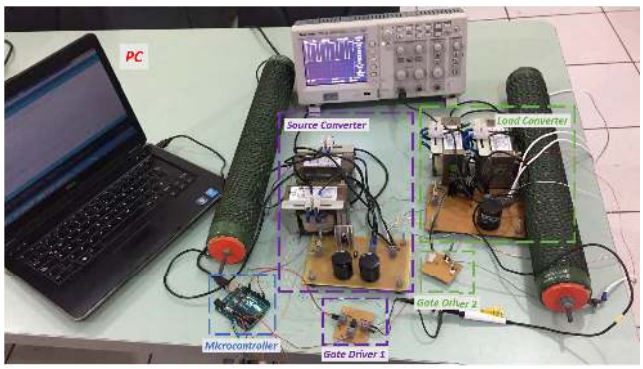
B. DESCRIPTION OF EXPERIMENTS

The Integral Square Error (ISE) is used to evaluate the performance of the proposed control strategy.

In order to design the controllers, the following (nominal) requirements are chosen to regulate output 1: settling time less or equal than 0.1 s and damping factor greater or equal



(a)



(b)

FIGURE 10. (a) Block diagram of the Multi-converter buck-buck test system developed for our experiments. (b) DC Multi-Converter buck-buck experimental setup.

than 0.9. To regulate output 2, requirements are: settling time less or equal than 0.05 s and damping factor greater or equal than 0.9. Note that the dynamics of output 2 is faster than output 1, being this a necessary condition for the load converter acts as a CPL.

The experiments compare performance of controllers tuned by CKR and CPP methodologies using PID control structure.

Table 2 shows the controllers gains for the controllers designed to regulate outputs 1 and 2. Note that only for the output 1 is considered the robust control methodology.

The first experiment is performed to check the closed-loop performance for positive variation of power reference. The source converter is set to its initial operating condition, as mentioned in Table 1, until the steady state is achieved. Then, source converter starts feeding load converter. Thereafter the steady state is achieved, the multi-converter is subjected to 0.5 p.u. a positive variation of power reference.

TABLE 2. Values of parameters for the designed controllers.

	Controller gains	CKR Method	CPP Method
$C_1(z)$	k_d	$1.0588e^{-5}$	$1.2024e^{-5}$
	k_p	0.010814	-0.009997
	k_i	2.6783	2.4169
$C_2(z)$	k_d	–	$2.49916e^{-5}$
	k_p	–	-0.025413
	k_i	–	51.6969

The second experiment evaluates the closed-loop performance for negative variation of power reference. The system starts to operate in the same way as for the positive variation test until the system achieves its steady state. After that, the system operates at an operating point of 0.7 p.u. in order to obtain a 0.5 p.u. negative variation.

The third experiment evaluates the closed-loop performance for positive and negative variation of power reference. After the multi-converter system reaches its stable state, a positive variation of 0.5 p.u. is performed at the operating point of power reference. Then, a negative variation of 0.5 p.u. is performed to return to the initial condition.

These experiments aim to show that the proposed robust controller is able to compensate oscillations caused by a CPL at output 1 when the system is submitted to positive and negative variations in its power operating condition, maintaining the desired performance for the uncertainty region and consequently different operation points. All the experiments are performed in experimental environment using the developed DC MCBB system and simulation environment using MATLAB/Simulink.

VII. ASSESSMENT OF RESULTS

A. EVALUATION OF SYSTEM UNDER A POSITIVE VARIATION OF POWER REFERENCE

Figs. 11 and 12 show the simulated responses performed in the multi-converter model, using a PID control with a positive variation of power reference. Figs. 13 and 14 shows the experimental evaluation performed in the multi-converter buck-buck system.

The multi-converter buck-buck system stars with load converter disconnected until source converter achieves its steady state (see Table 1), then the load converter is connected (t = 0.5 s) causing a load disturbance at the output of source converter. When the multi-converter buck-buck system is operating in its steady state (8V and 0.3 p.u.), the system is subjected to a positive variation of power reference (t = 1.0 s) within amplitude range from 0.1 to 0.5 p.u..

Figs. 11 and 13 show the simulated and experimental results, respectively, of source converter performance, when the system is subjected to a positive variation of 0.5 p.u. of its power reference (see Figs. 12(c) and 14(c)) using a PID control based on CPP and CKR approaches.

Fig. 12 and 14 show the simulated and experimental results, respectively, of load converter performance, using a PID control based on CPP approach, when the output of source converter is regulated by a PID control based on CPP and CKR approaches.

Note that all information about transient response, reference tracking and load perturbation are given in Figs. 11 to 14, obtaining a better performance of multi-converter buck-buck

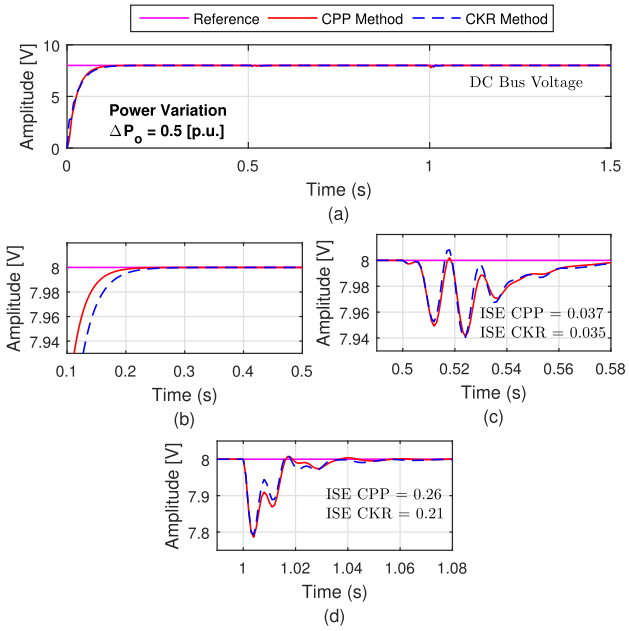


FIGURE 11. Source converter performance. (a) Simulated results for positive variations on the value of power reference of the Multi-converter buck-buck system using PID control structures. (b) Transient response. (c) Oscillations caused by the connection of load converter. (d) Oscillations caused by the variation of power reference of system.

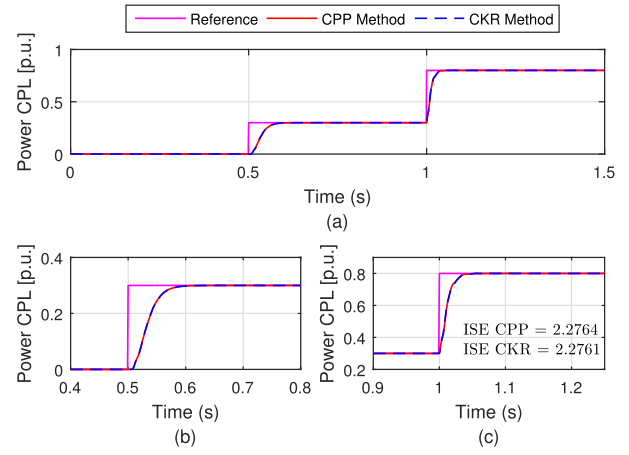


FIGURE 12. Load converter performance. (a) Simulated results for positive variations on the value of power reference of the Multi-converter buck-buck system using PID control structures. (b) Transient response. (c) Variation of power reference of system.

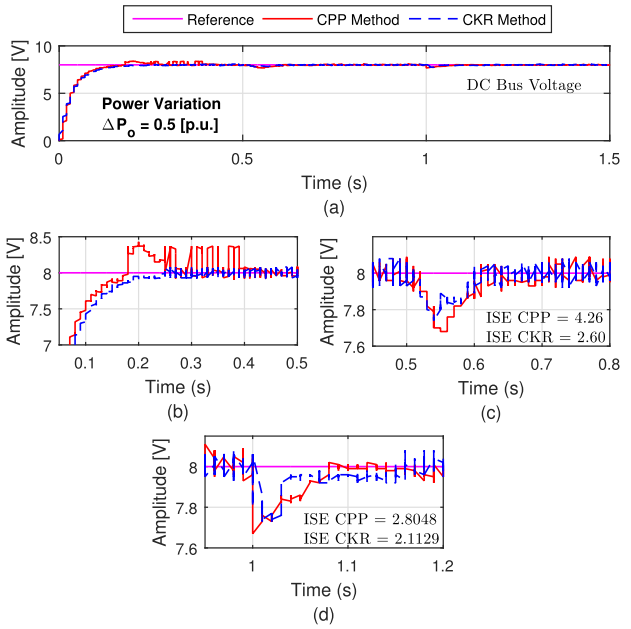


FIGURE 13. Source converter performance. (a) Experimental results for positive variations on the value of power reference of the Multi-converter buck-buck system using PID control structures. (b) Transient response. (c) Oscillations caused by the connection of load converter. (d) Oscillations caused by the variation of power reference of system.

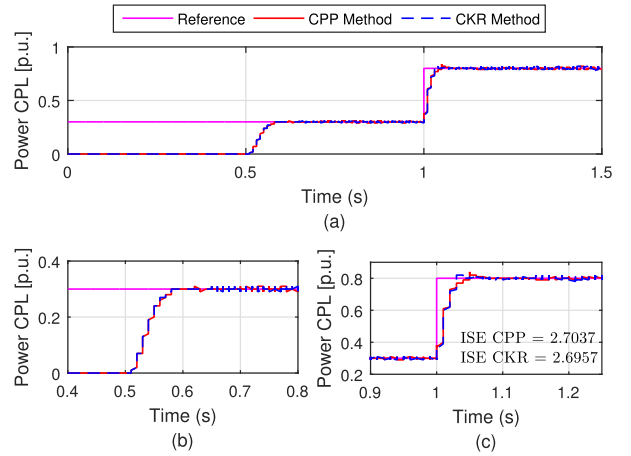


FIGURE 14. Load converter performance. (a) Experimental Results for positive variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures. (b) Transient Response. (c) Variation of power reference of system.

system when the source converter is regulated by CKR approach.

Figs. 15 and 16 show, respectively, the simulated and experimental evaluation performed in the multi-converter buck-buck system, using a PID control structures for different values of positive variation of power reference.

The simulated and experimental results demonstrate that both controllers of source converter can compensate oscillations at output 1 caused by positive variations in the power operating condition of system.

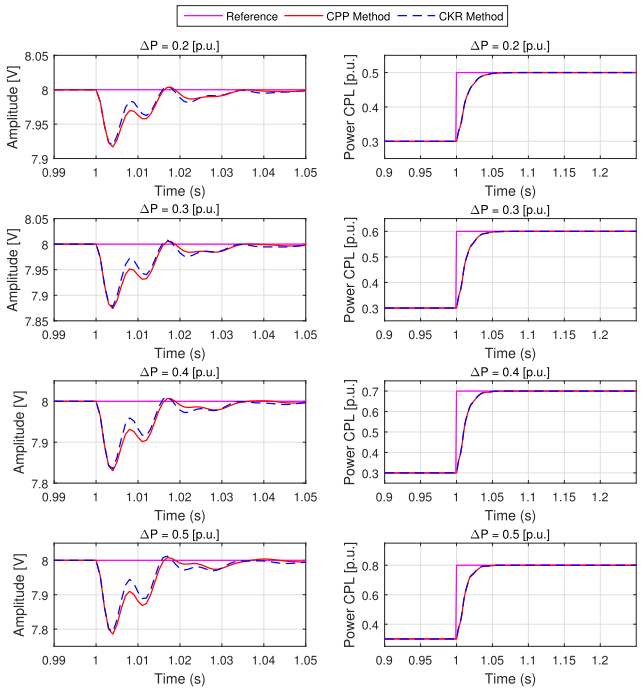


FIGURE 15. Simulated Results for positive variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures.

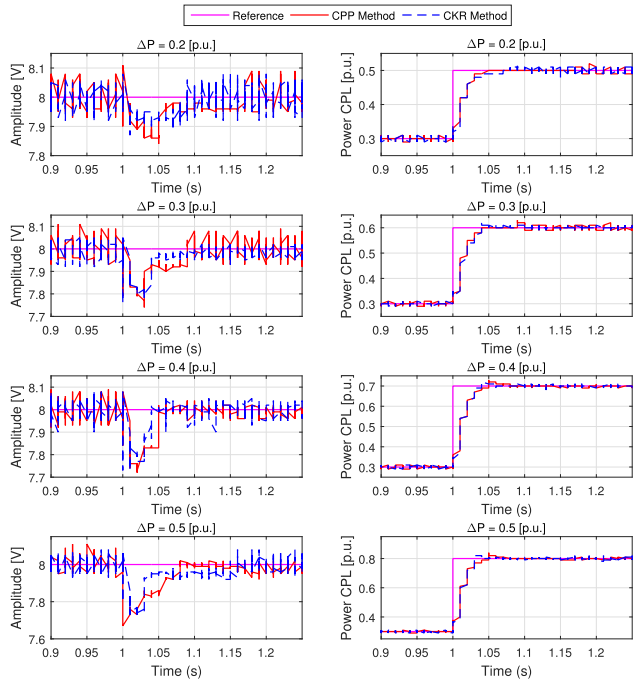


FIGURE 16. Experimental Results for positive variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures.

However, the interval robust (CKR Method) controller proposed in this paper provides a better performance in comparison with classical controller (CPP Method). Therefore, the impact of positive power variation is lower for the

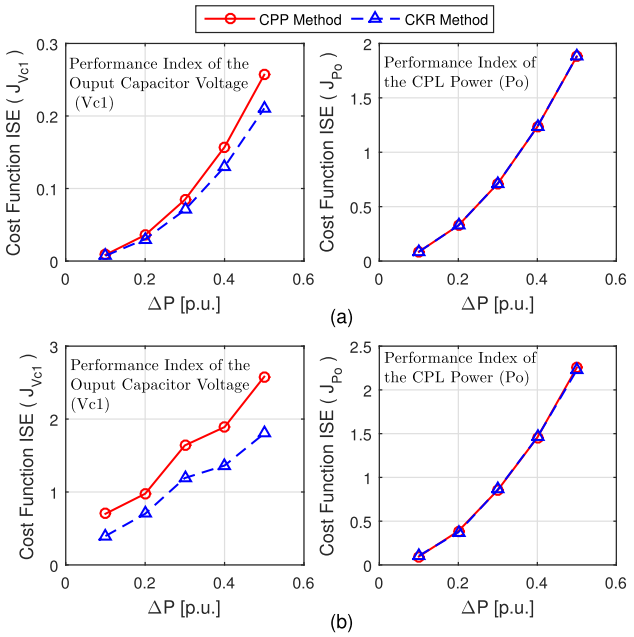


FIGURE 17. The cost function ISE of system outputs for positive variations of power reference. (a) Simulation assessment. (b) Experimental assessment.

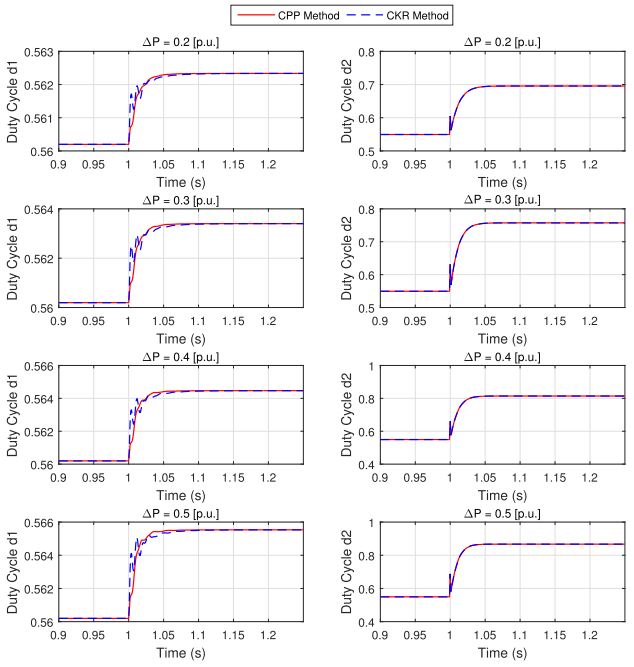


FIGURE 18. The control effort test of simulated system, when the system is subjected to positive variations on the value of power reference.

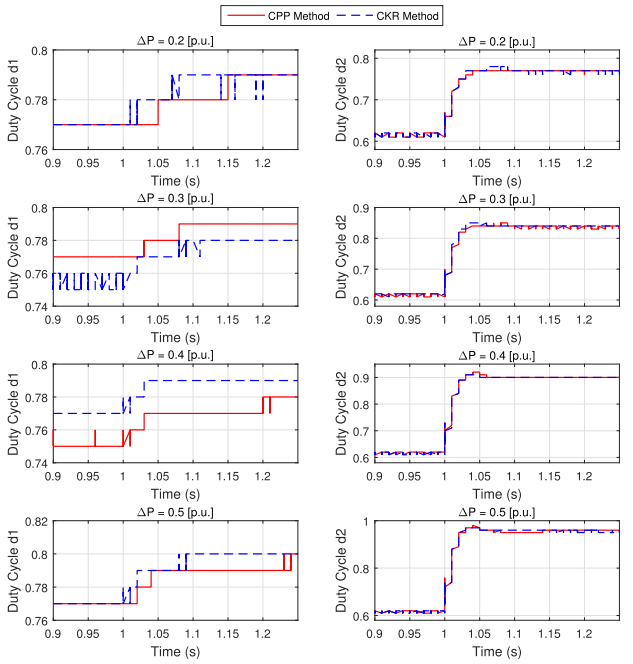


FIGURE 19. The control effort test of experimental system, when the system is subjected to positive variations on the value of power reference.

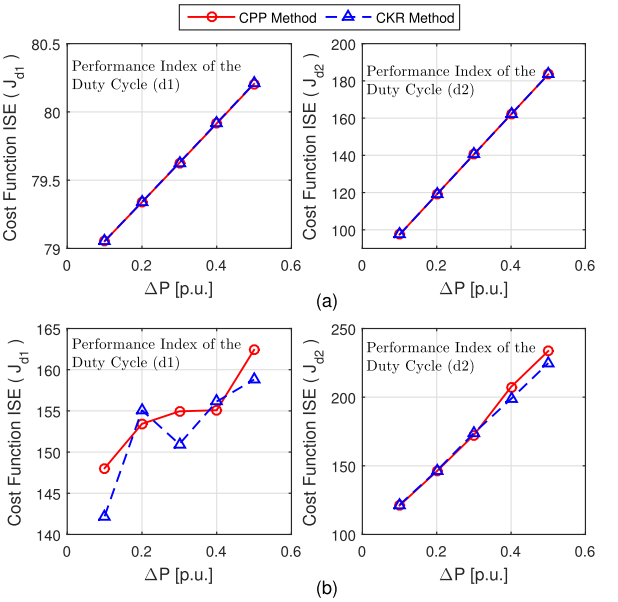


FIGURE 20. The cost function ISE of effort control system for positive variations of power reference. (a) Simulation assessment. (b) Experimental assessment.

controller by CKR method as shown by the ISE performance indices in Figs. 17(a) and 17(b), ratifying the robustness of the proposed methodology.

Figs. 18 and 19 show the control effort of controllers for simulated and experimental tests, respectively, using a PID control structures.

Note that the saturation of the control signal does not occur at any time.

For the simulated case, the control effort obtained was almost similar for controllers of system as shown their ISE performance indices in Fig. 20(a). However, the performance presented by controllers in experimental tests was different as shown in Fig. 20(b).

The DC multi-converter buck-buck system obtained less degradation in the control system performance when the robust proposed controller controls the output 1 of

multi-converter buck-buck system. Fig. 20 shows the ISE index performance of control effort of signal.

Although the control strategy to regulate the load converter does not change, different performances can be observed (see Fig. 20(b)) due to the oscillation in the output voltage of source converter caused by the variation of power reference. Thereby, the controller of the voltage regulation stage that better compensates for the oscillations will cause less deterioration in the performance of the controller of the power control stage.

In the MCBB system, the load converter is considering a load for the source converter, thus, any change in the operating conditions of load converter affects as a load disturbance at the output of the source converter. Therefore, the greater the reference variation at output 2 (Power CPL), the greater the voltage oscillation at output 1 as shown in simulated (see Fig. 15) and experimental (see Fig. 16) assessment.

The simulated and experimental tests performed show that the robust proposed (CKR) approach outperforms the classical (CPP) approach for several values of power variations (P_o). Therefore, the controller proposed provides a better performance with reduced oscillation amplitude at output 1 in comparison with the classical controller.

Fig 17 shows the comparison of ISE performance index for the multi-converter test system between robust and classical approaches. For most of the operating value of P_o, the ISE indices for CPP method shows higher values in comparison with CKR method.

B. EVALUATION OF SYSTEM UNDER A NEGATIVE VARIATION OF POWER REFERENCE

Figs. 21 and 22 show the simulated evaluation performed in the MCBB model, using a PID control with a negative variation of power reference. Figs. 23 and 24 shows the experimental evaluation performed in the multi-converter buck-buck system.

According to Figs. 21 to 24, the experiment begins in the same way that the experiment described in Section VII(A) until the MCBB system achieves its steady state (8V and 0.3 p.u.). Then, a variation in operating condition at output 2 (P_o) occurs at t = 1 s, as explain in Section VI(B), so the system will operate with the following conditions: ${V_{C_1}}^o = 8\ V$ and $P_o = 0.7\ p.u.$, after that, the system is subjected to a negative variation of power reference (t = 1.5 s) within an amplitude range from 0.1 to 0.5 p.u..

Fig. 21 shows the simulated results of source converter performance, when the system is subjected to a negative variation of 0.5 p.u. of its power reference (see Figs. 22(d) and 24(d)) using a PID control based on CPP and CKR approaches, while Fig. 23 shows the experimental results of the same test.

Fig. 22 shows the simulated results of load converter performance, using a PID control based on CPP approach, when the output of source converter is regulated by a PID control based on CPP and CKR approaches, while Fig. 24 shows the experimental results of the same test.

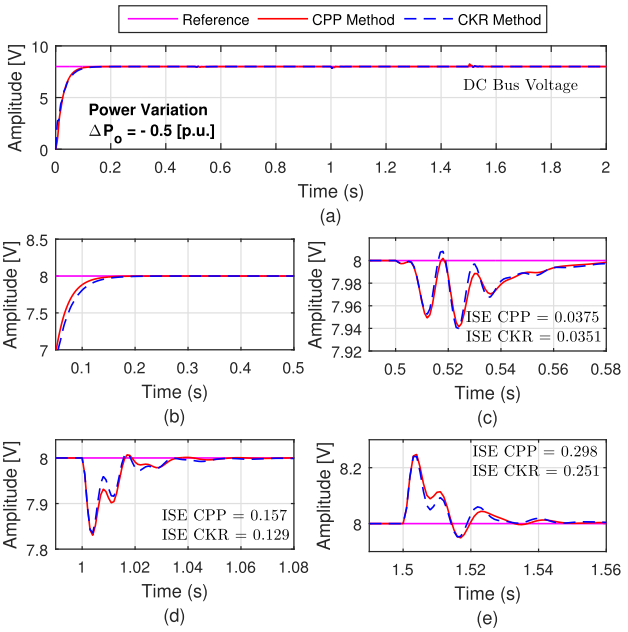


FIGURE 21. Source converter performance. (a) Simulated Results for negative variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures. (b) Transient Response. (c) Oscillations caused by the connection of load converter. (d) Oscillations caused by a positive variation of power reference of system. (e) Oscillations caused by a negative variation of power reference of system.

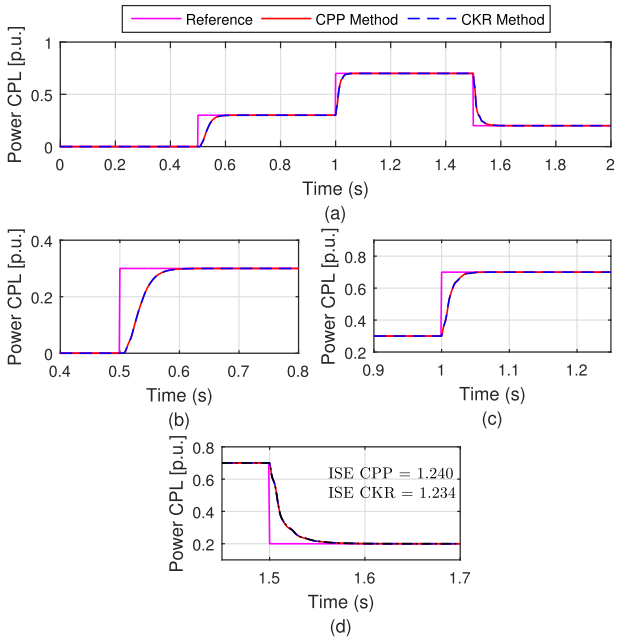


FIGURE 22. Load converter performance. (a) Simulated Results for negative variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures. (b) Transient Response. (c) Positive Variation of power reference of system. (d) Negative Variation of power reference of system.

Note that all information about transient response, reference tracking and load perturbation are given in Figs. 21 to 24, obtaining a better performance of multi-converter buck-buck

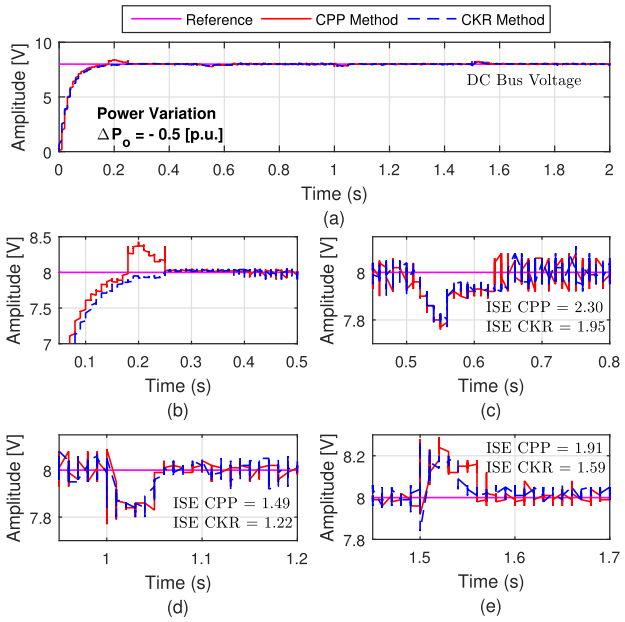


FIGURE 23. Source converter performance. (a) Experimental Results for negative variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures. (b) Transient Response. (c) Oscillations caused by the connection of load converter. (d) Oscillations caused by a positive variation of power reference of system. (e) Oscillations caused by a negative variation of power reference of system.

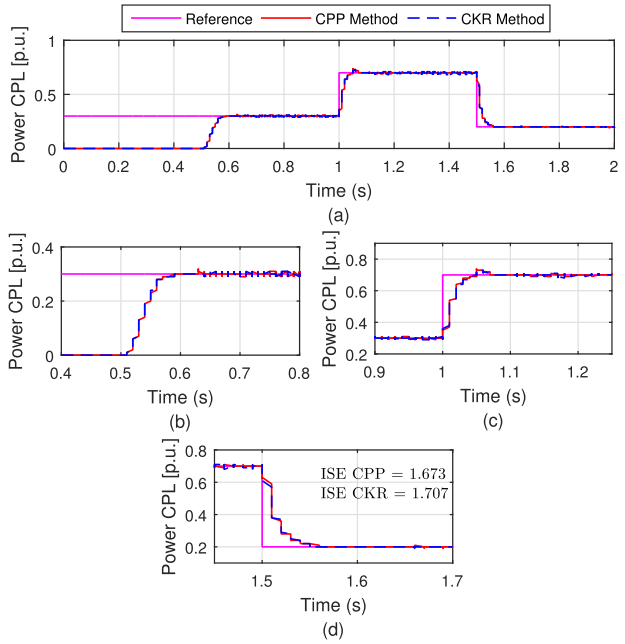


FIGURE 24. Load converter performance. (a) Experimental Results for negative variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures. (b) Transient Response. (c) Positive Variation of power reference of system. (d) Negative Variation of power reference of system.

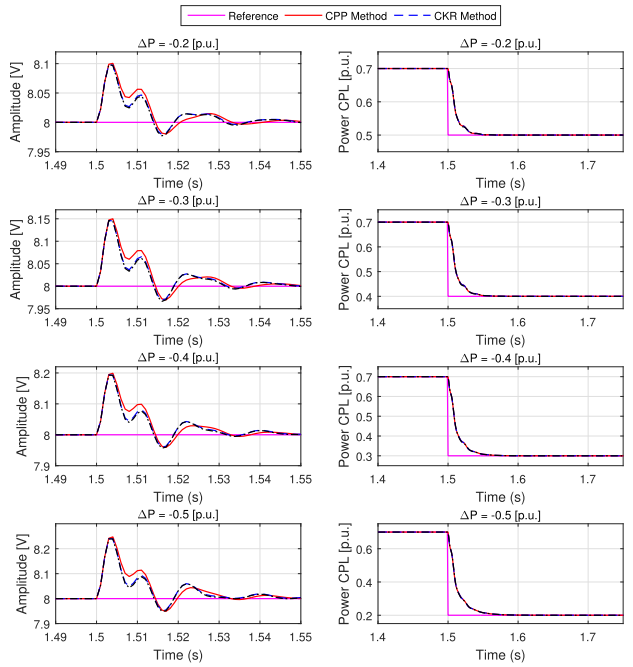


FIGURE 25. Simulated Results for negative variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures.

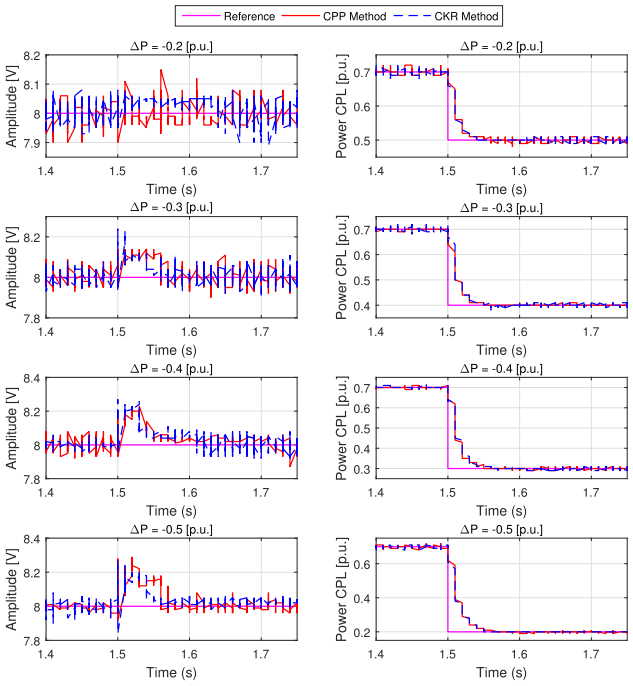


FIGURE 26. Experimental Results for negative variations on the value of power reference of the Multi-Converter buck-buck system using PID control structures.

system for negative variation of power reference when the source converter is regulated by CKR approach.

Figs. 25 and 26 show, respectively, the simulated and experimental evaluation performed in the multi-converter buck-buck system, using a PID control structures for negative variations in operating condition at output 2 (P_o).

The simulated and experimental results that both controllers have succeeded in correcting the load disturbance at output 1 (V_{C_1}) caused by negative variations in the power

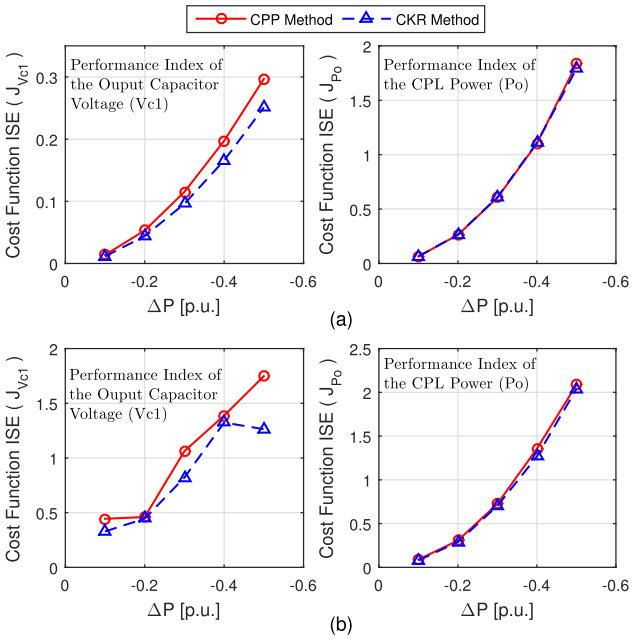


FIGURE 27. The cost function ISE of system outputs for negative variations of power reference. (a) Simulation assessment. (b) Experimental assessment.

operating condition (P_o) of multi-converter buck-buck system. However, the proposed robust controller (CKR Method) more effectively compensates the oscillations in comparison with the classical controller (CPP Method). Therefore, the impact of negative variation of power reference (P_o) is lower for the CKR Method as shown in Figs. 27.

Figs. 27(a) and 27(b) show the comparison of ISE performance index of classical and robust controllesr for simulated and experimental assessment, respectively. The ISE index evaluates the impact of negative variation of power reference (P_o) on system performance. Therefore, the robust controller (CKR) shows the best performance under negative variation of power reference (P_o) for simulated and experimental tests confirming the robustness of the proposed robust control methodology.

According to results while the greater the reference variation at output 2 (Power CPL), the greater the voltage oscillation at output 1 as shown in simulated (see Fig. 25) and experimental (see Fig. 26) assessment.

Figs. 28 and 29 show the control effort of controllers for simulated and experimental tests, respectively, under power reference (P_o). Note that the saturation of the control signal does not occur at any time.

Note that for the simulated case, the obtained control effort was almost similar for controllers of system as shown their ISE performance indices in Fig. 30(a). However, the performance presented by controllers was different.

The multi-converter buck-buck system obtained less degradation in the control system performance when the robust proposed controller controls output 1.

Fig. 30(b) shows the ISE index performance of control effort signal.

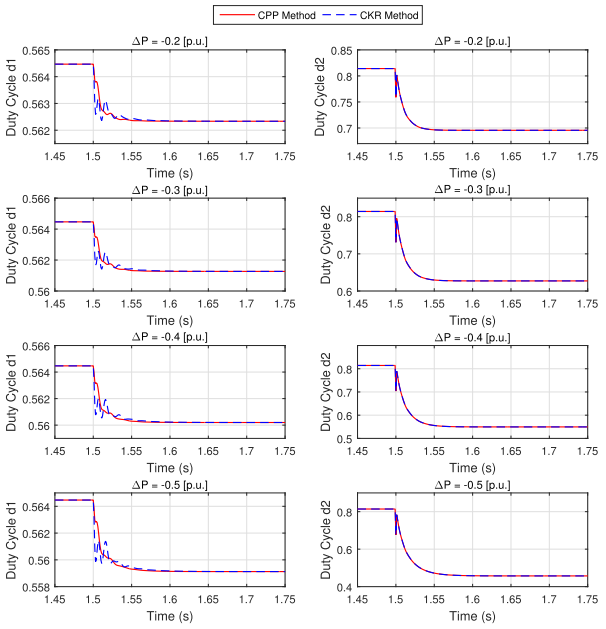


FIGURE 28. The control effort test of simulated system, when the system is subjected to negative variations on the value of power reference.

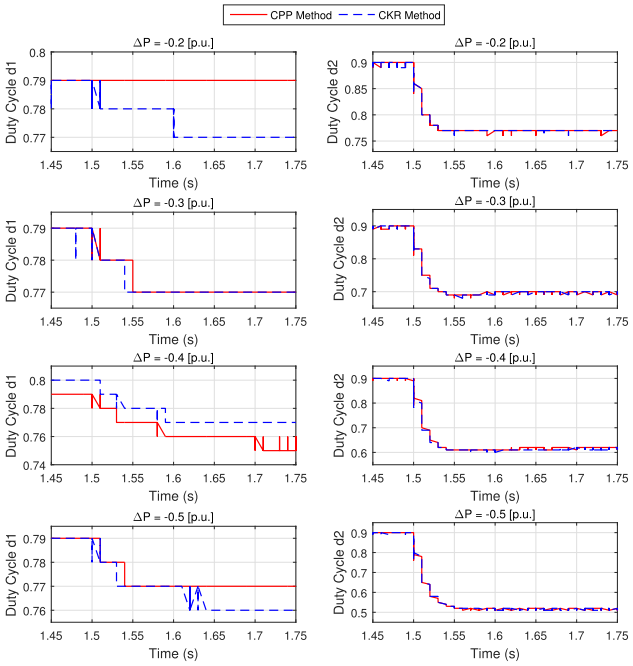


FIGURE 29. The control effort test of experimental system, when the system is subjected to negative variations on the value of power reference.

C. PERFORMANCE EVALUATION UNDER CPL POWER VARIATION

Fig. 31 shows the experimental evaluation performed in the MCBB system, using a PID control based on CPP approach. Fig. 32 shows the experimental evaluation performed in the MCBB system, using a PID control based on CKR approach.

According to Figs. 31 and 32, the experiment begins in the same way that the experiment described in Section VII(A) and VII(B) until the MCBB system achieves

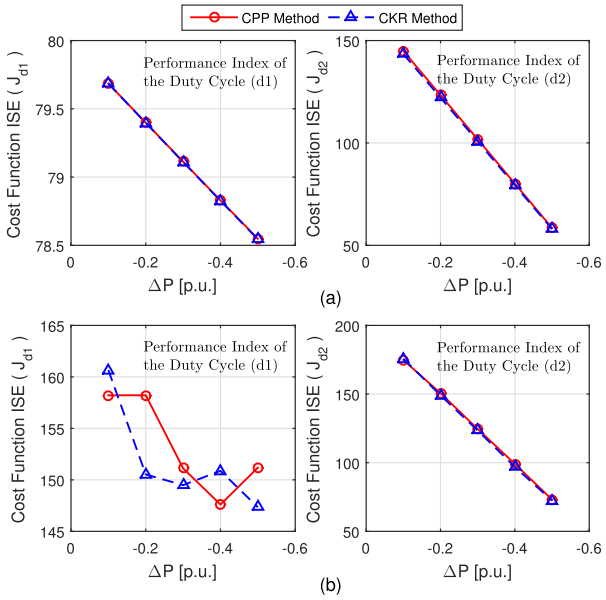


FIGURE 30. The cost function ISE of effort control system for negative variations of power reference. (a) Simulation assessment. (b) Experimental assessment.

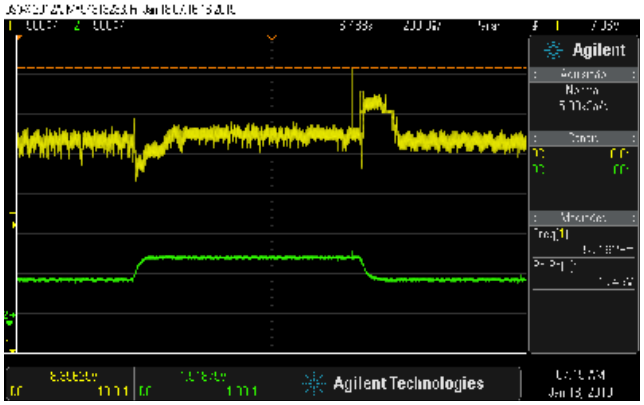


FIGURE 31. MCBB system performance, using a PID control based on CPP approach.

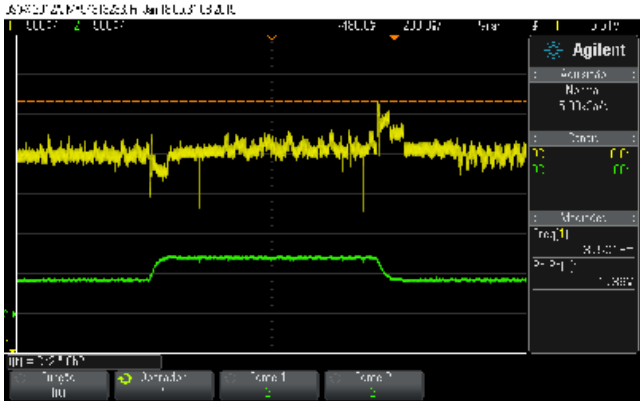


FIGURE 32. MCBB system performance, using a PID control based on CKR approach.

its steady state (8V and 0.3 p.u.). Then, a variation in operating condition at output 2 (P_o) occurs at $t = 0.75\ s$, as explain in Section VI(B), so the system will operate with the following conditions: ${V_{C_1}}^o = 8\ V$ and $P_o = 0.8\ p.u.$, after that, the system is subjected to a negative variation of power reference ($t = 1.25\ s$) returning to the initial condition (8V and 0.3 p.u.).

Figs. 31 and 32 show the CPL power variation and the voltage oscillations in the feeder converter by using the classical control methodology and robust control methodology, respectively. It is worth note that the CKR approach outperforms the other approach due to the minimum voltage oscillation occurrence, in addition, the oscillation is quickly corrected in comparison with the CPP approach, furthermore the CKR methodology presents the smaller voltage ripple than the CPP approach. In order to ratify these results, the integral index of this oscillation for all approaches was calculated. the CKR approach presents 1.42 of the ISE value and the CPP approach presents 2.16 ISE value, therefore, it was ratified that the CKR approach outperform the CPP approach when there is variation of a CPL power variation in the system.

VIII. CONCLUSION

This paper proposes to use a robust parametric control technique for designing fixed order robust controller, in order to minimizing oscillations effects caused by constant power load in a DC Multi-converter buck-buck system guaranteeing robust stability and robust performance for an entire predefined uncertainty region.

The proposed technique has been exhaustively evaluated in both computational simulations as well as by means of experiments performed in a 20 W DC Multi-converter. The proposed robust controller (CKR Method) performance is compared with a classical controller based on pole-placement (CPP Method).

According to the results obtained via simulations and experiments, it is concluded that when the multi-converter buck-buck system is subjected to a certain variation of reference power (P_o), the CKR method more effectively compensates the oscillations at output voltage of source converter (V_{C_1}) improving the performance of the whole system as shown by the performance indicators obtained in this work.

Therefore, the results indicate that the proposed robust controller is justified and presents relevant improvements in the Multi-converter control, offering robust performance and stability.

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