Intra-Chip Wireless Interconnect for Clock Distribution Implemented With Integrated Antennas, Receivers, and Transmitters

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***Abstract*—A wireless interconnect system which transmits and receives RF signals across a chip using integrated antennas, receivers, and transmitters is proposed and demonstrated. The transmitter consists of a voltage-controlled oscillator, an output amplifier, and an antenna, while the receiver consists of an antenna, a low-noise amplifier, a frequency divider, and buffers. Using a 0.18-μm CMOS technology, each of these individual circuits is demonstrated at 15 GHz. Wireless interconnection for clock distribution is then demonstrated in two stages. First, a wireless transmitter with integrated antenna generates and broadcasts a 15-GHz global clock signal across a 5.6-mm test chip, and this signal is detected using receiving antennas. Second, a wireless clock receiver with an integrated antenna detects a 15-GHz global clock signal supplied to an on-chip transmitting antenna located 5.6 mm away from the receiver, and generates a 1.875-GHz local clock signal. This is the first known demonstration of an on-chip clock transmitter with an integrated antenna and the second demonstration of a clock receiver with an integrated antenna, where the receiver's frequency and interconnection distance have approximately been doubled over previous results.**

***Index Terms*—15 GHz, clock distribution, frequency divider, injection locking, integrated antenna, low noise amplifier (LNA), on-chip antenna, RF CMOS, voltage-controlled oscillator (VCO), wireless clock distribution, wireless interconnect, zigzag antenna.**

I. Introduction

TRADITIONAL interconnect systems have been projected to be limited in their ability to meet the performance needs of microprocessors at the 0.1-μm technology node and beyond. This limit is due to the global interconnect delay becoming significantly larger than the gate delay [1], [2]. While copper and low-κ dielectrics have been introduced to decrease the global interconnect delay, they only extend the lifetime of conventional interconnect systems a few technology generations. The global interconnect delay is particularly detrimental to global clock distribution, since these signals need to be distributed across the microprocessor with skews of less than 10% of the global clock period. With each succeeding generation of microprocessors, the clock frequency increases, decreasing the clock period and thus the skew requirement in absolute time. This is in contrast to chip area and total delay through the clock distribution network, which are both increasing [1]. Hence, techniques are required to equalize the increasingly large delays of each distributed clock signal to even greater accuracies or lower clock skews. To address this need, advanced interconnect systems capable of distributing high-frequency signals with short propagation delays while dissipating minimal power must be investigated and developed.

The improved radio-frequency (RF) capability and projected increase in die size for CMOS circuits have led to the concept of wireless interconnect systems [3]–[6]. The wireless interconnect system consists of integrated receivers and transmitters with on-chip antennas which communicate across a single chip or between multiple chips at the speed of light via electromagnetic waves. Wireless interconnects can be used for both data and clock signals. However, for wireless data, a modulation scheme is required, while for a wireless clock, only a single tone is required. Therefore, wireless clock distribution is a natural first step for evaluating the potential of wireless interconnects in general as well as for developing the key components of a wireless interconnect system.

A conceptual illustration of an intra-chip wireless interconnect system for clock distribution is shown in Fig. 1(a). A signal is generated on-chip at $\sim$8 times the local clock frequency and applied to an integrated transmitting antenna which is located at one part of the integrated circuit (IC). Clock receivers distributed throughout the IC detect the transmitted signal using integrated antennas, and then amplify and synchronously divide it down to the local clock frequency. These local clock signals are then buffered and distributed to adjacent circuitry. Fig. 1(b) shows an illustration of an inter-chip wireless clock distribution system. Here, the transmitter is located off-chip, utilizing an external antenna, potentially with a reflector. Integrated circuits located on either a board or a multichip module each have integrated receivers which detect the transmitted global clock signal and generate synchronized local clock signals. Note that the inter-chip system with an off-chip transmitter results in equalized phases and amplitudes of the received global clock signals, greatly reducing clock skew caused by phase or amplitude mismatch.

Wireless interconnects can provide multiple benefits. As with optical interconnects, signals propagate at the speed of light in wireless interconnects. However, optical components are not

Manuscript received August, 2001; revised December, 2001. This work was supported by the Semiconductor Research Corporation under Contract 885.002.

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Publisher Item Identifier S 0018-9200(02)03664-8.

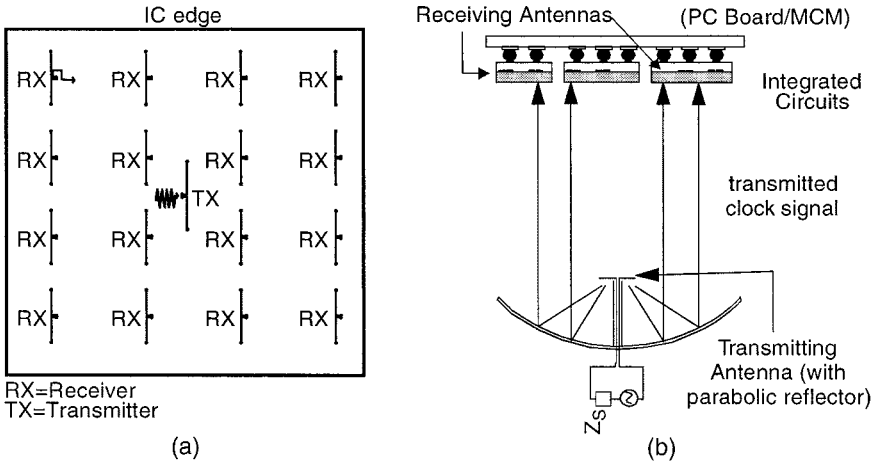

Fig. 1. Conceptual system illustrations of (a) intra-chip and (b) inter-chip wireless interconnect systems for clock signal distribution.

needed and the system should therefore be easier to integrate into CMOS ICs. Wireless interconnect should also provide an additional means for global communications, freeing up conventional wires for other uses. Also, using wireless interconnects in a clock distribution system should reduce the latency in the clock tree, which should help reduce clock skew and should eliminate the frequency dispersion problem that may ultimately limit the maximum clock frequency [7].

This paper demonstrates 15-GHz on-chip wireless interconnects consisting of a clock transmitter and clock receivers, integrated with antennas [6]. The circuits are implemented in a 0.18-μm CMOS technology with six layers of copper interconnects and a substrate resistivity of 15–25 $\Omega\cdot$cm. The paper is organized as follows. Sections II and III present the circuitry used in the clock transmitter and receiver, respectively. Section IV presents the wireless interconnect results, including on-chip antennas, a clock transmitter with integrated antenna, and a clock receiver with integrated antenna. Section V presents conclusions, assessing the potential of intra-chip wireless interconnects and the potential of 0.18-μm CMOS for RF applications above 10 GHz.

II. Transmitter Circuitry

A simplified block diagram for the clock transmitter is shown in Fig. 2(a). The 15-GHz signal is generated using a differential voltage-controlled oscillator (VCO). The VCO is required to have low phase noise to decrease the clock jitter. The signal from the VCO is then amplified by a two-stage output amplifier and delivered to the transmitting antenna. In the final clock distribution system implementation, the VCO will be phase locked to an external reference. However, to ease the implementation requirements for this chip, the transmitter was operated open-loop, where the frequency of the VCO was controlled directly with its dc input.

A. Voltage-Controlled Oscillator

A schematic of the VCO and output amplifier is shown in Fig. 3. Cross-coupled transistors M_1 and M_2 form a positive feedback loop, providing negative resistances to the *LC* tanks.

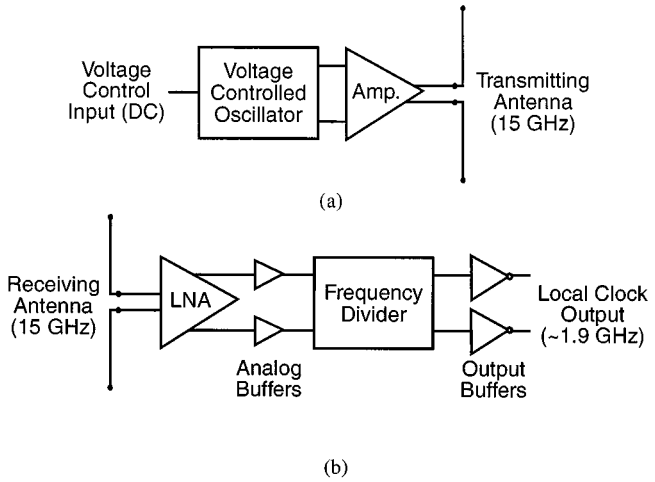

Fig. 2. Block diagram of (a) the open-loop clock transmitter and (b) the clock receiver.

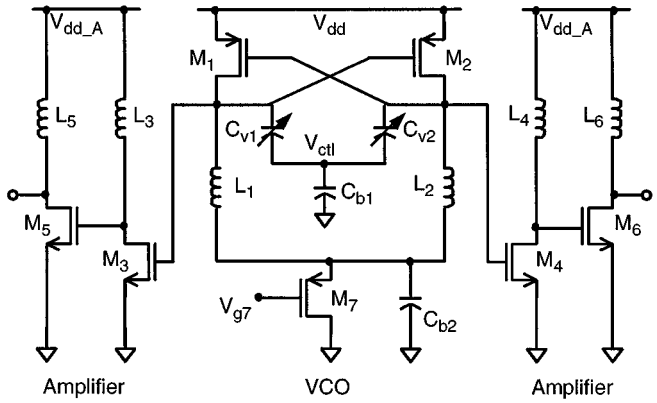

Fig. 3. Schematic of the VCO and the output amplifier.

PMOS transistors are exclusively used in this VCO design, due to their reduced $1/f$ noise and lower hot-carrier noise, resulting in improved phase noise [8]–[10]. The inductors for the *LC* tank are implemented in metal layers 5 and 6, above a polysilicon patterned ground shield. The measured Q is 10 at 15 GHz. The varactor is implemented using an accumulation-mode MOS capacitor, whose measured Q is approximately 47 at 15 GHz.

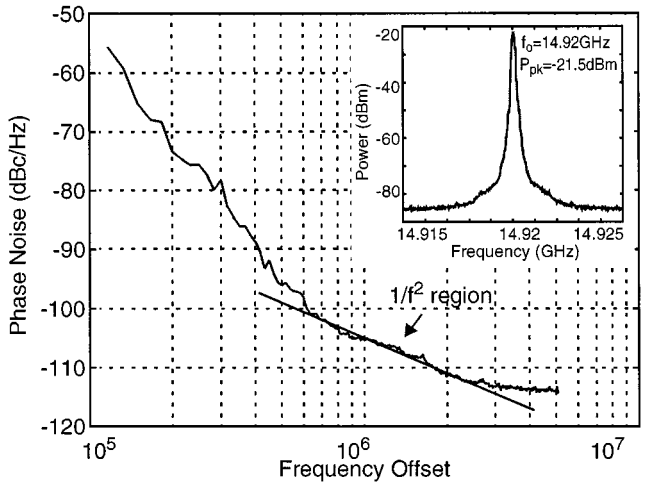

Fig. 4. Single-sideband plot for the 0.18-μm VCO with an output spectrum inset.

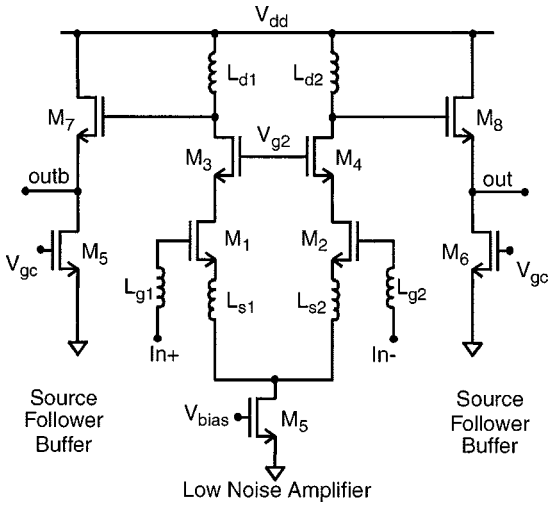

Fig. 5. Schematic of the differential 14-GHz LNA with source-follower buffers.

A test structure consisting of the VCO core plus a single-stage 50-Ω output buffer was connected to a spectrum analyzer, yielding the output single-sideband phase-noise plot and spectrum shown in Fig. 4. With $V_{\rm ctl} = 1.2$ V, the measured center frequency is 14.92 GHz, with an output power level of -21.5 dBm. The VCO core consumes 7.2 mW from a 1.5-V supply. The phase noises at 1-MHz and 3-MHz offsets are -105 and -113 dBc/Hz, respectively. To understand the competitiveness of this VCO result with previously published results, the phase noise can be scaled to a 5-GHz regime, using Leeson's formula [11]. Thus, for a given inductor Q, the 15-GHz VCO would correspond to a 5-GHz VCO achieving a phase noise of -114.5 dBc/Hz at a 1-MHz offset. This result is $\sim$2.5 dB worse than that achieved in [9] at 5.35 GHz. The tuning range of the VCO is 690 MHz, for $V_{\rm ctl}$ between 0 and 1.8 V. The linear portion of this curve reveals a VCO gain of approximately 600 MHz/V.

B. Output Amplifier

The output amplifier consists of two stages of inductively loaded common-source amplifiers. Since the transistor noise in the amplifier does not significantly degrade the VCO phase-noise performance, nMOS transistors are used. The first class-A stage serves as a preamplifier for the final output amplifier stage. The second stage acts as a pseudo class-E amplifier without a bandpass filter (traditionally used to select the fundamental), and is tuned together with the antenna impedance. As the amplifier switches, the fundamental is transmitted. Higher order harmonics are greatly attenuated due to the impedance mismatch between the antenna and the amplifier at these frequencies. The transistor widths of stage 1 are only 2/3 of that of M_1 in the VCO core, which avoids significantly loading the VCO output. At the tuned frequency, the single-sided output has an amplitude approximately equal to the supply voltage, with an offset voltage of $V_{{\rm dd},A}$; hence, the output power can be controlled by varying $V_{{\rm dd},A}$. The simulated power efficiency is $\sim$60%. At 1.3 V, measurements show that the amplifier delivers -13.2 dBm to the antenna at 15 GHz, while the peak gain occurs at 18 GHz.

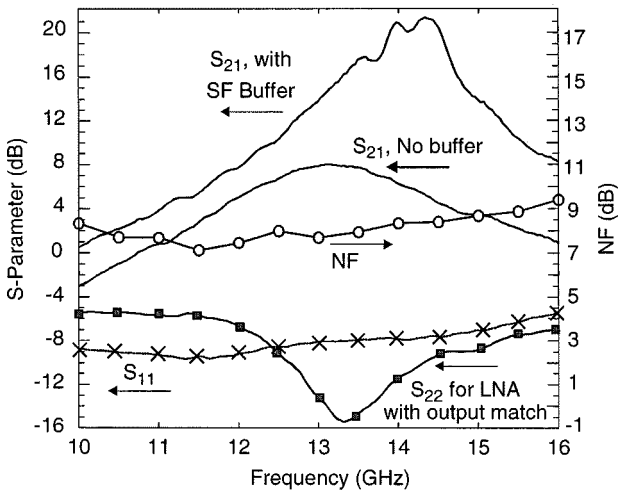

Fig. 6. Measured S-parameters and noise figure of the LNA with source-follower buffers.

III. Receiver Circuitry

A block diagram for the clock receiver is shown in Fig. 2(b). The received signal is amplified using a low-noise amplifier (LNA) and divided down to the local clock frequency, and then the signal is buffered to provide the local clock signal. The amplifier is tuned to the clock transmission frequency to reduce interference and noise. Since the microprocessor is extremely noisy at the local clock frequency and its harmonics, transmitting the global clock at a frequency higher than the local clock frequency provides an increased noise immunity for the system [12]. Also, operating at a higher frequency decreases the required antenna size. The receiver is implemented in a fully differential architecture, which rejects common-mode noise (such as substrate noise), obviates the need for a balanced-to-unbalanced conversion at the input, and provides dual-phase signals to the frequency divider.

A. Low-Noise Amplifier

A schematic of a fully differential LNA [13], [14] with source follower buffers [5] is shown in Fig. 5. The LNA is input

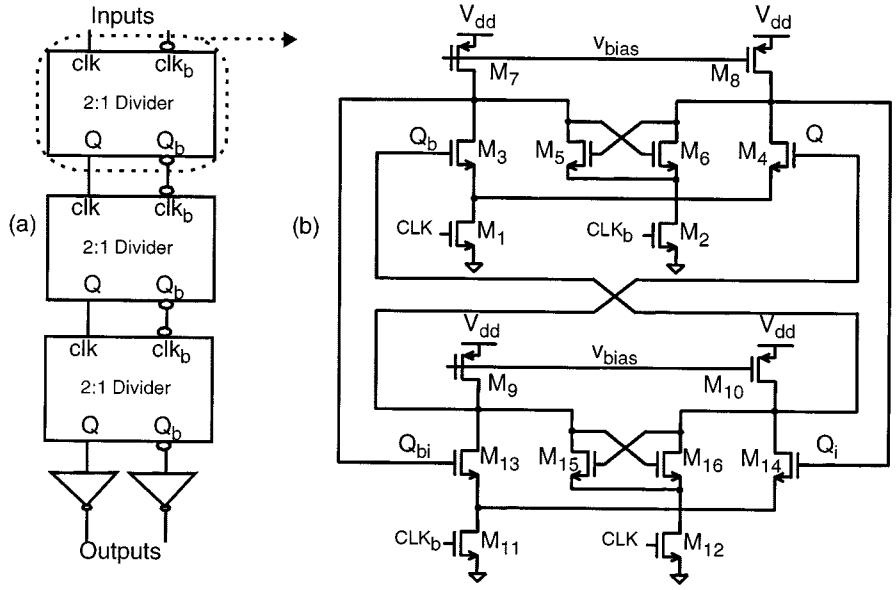

Fig. 7. (a) Block diagram of the 8:1 frequency divider and (b) circuit schematic of each 2:1 frequency divider.

matched to the projected antenna impedance of 125–j55 Ω at 15 GHz. Due to size constraints, the antenna is not designed to be resonant, hence its reactance is nonzero, and additional series inductance in the LNA is used to complete the match. A single-stage cascode amplifier topology with gate, source, and drain inductors is used for each half circuit. The use of inductive degeneration allows both the input power and noise matching conditions to nearly coincide. Following the LNA are source-follower buffers, used to provide a dc level shift and to isolate the LNA from the divider. When driving a capacitive load, a source follower has tunable negative input conductance. By adjusting the current through the buffer (i.e., $V_{\rm gc}$), the total conductance at the output of the LNA can be decreased, increasing the overall circuit gain. However, the total conductance must remain positive, else oscillations can occur.

The measured (on-wafer) S_{21}, S_{11}, and noise figure for the differential LNA and buffers ($V_{\rm gc} = 0.5$ V) are 21 dB, -8 dB, and 8 dB, respectively, at the resonant frequency of 14.4 GHz, as shown in Fig. 6. The circuit consumes 28 mW from a 1.5-V supply. The LNA inductor Q's are $\sim$15 at 15 GHz. By increasing $V_{\rm gc}$ to 0.9 V, the gain can be increased to 25 dB, however, S_{22} becomes positive and the circuit is unstable, demonstrating the effect of negative conductance on gain and stability. Finally, the S_{21} and S_{22} for an LNA test circuit output matched differentially to 100 Ω using a capacitive transformer are 8 and -15 dB, respectively, also shown in Fig. 6.

B. Injection-Locked Frequency Divider (ILFD)

An 8:1 (divide-by-eight) injection-locked frequency divider is implemented by cascading three 2:1 dividers [5], [9], [15], as shown in Fig. 7(a). A schematic of the 2:1 divider is shown in Fig. 7(b), consisting of two source-coupled-logic (SCL) D-latches in a master–slave configuration. Fig. 8(a) shows the maximum input frequency and power consumption (for the 8:1 divider core) versus supply voltage for a 64:1 divider, consisting of an 8:1 SCL divider and an 8:1 true-single-phase clocked divider [16]. For a 1.5-V $V_{\rm dd}$, the maximum input frequency is 15.8 GHz, and the power consumption is 4.5 mW, while for a 2.1-V $V_{\rm dd}$, the maximum input frequency is 20.4 GHz and the power consumption is 12.2 mW.

Injection locking is the process of synchronizing a free-running oscillator to an input signal [17]–[19]. Before injection locking can be understood, the divider's free-running oscillation must first be described. The 2:1 SCL divider topology will self-oscillate when $\rm CLK$ and $\rm CLK_B$ are close to their common-mode values. This turns on both D-latches simultaneously, and the circuit becomes a two-stage ring oscillator (equivalent to a regenerative oscillator). The period of self-oscillation for the outputs of the 2:1 divider is equal to $4\tau_{\rm pd}$, where $\tau_{\rm pd}$ is the propagation delay for a single D-latch. During design, $\tau_{\rm pd}$ can be controlled by adjusting the transistor dimensions, as well as by adjusting the common-mode voltage on the $\rm CLK$ lines. During testing, $\tau_{\rm pd}$ can be controlled by adjusting the divider's $V_{\rm dd}$. Due to the differential structure of the latch, the source nodes of $M_{3,4}$ and $M_{5,6}$ oscillate at twice the natural frequency, or at a period of $2\tau_{\rm pd}$. This is the input-referred self-oscillation frequency (herein termed $f_{\rm iSO}$). The gates of the clock transistors (M_1 and M_2) are therefore an ideal place to inject signals close to $f_{\rm iSO}$, and lock this "double-frequency" oscillator (drain of M_1). Accordingly, the outputs of the 2:1 ILFD are injection locked at half the input frequency.

A benefit of injection locking is the high input sensitivity of the circuit. In other words, an ILFD exhibits conversion gain. This property is ideally suited for wireless interconnects, since the receiver's minimum detectable signal (MDS) can be improved. Fig. 8(a) shows $f_{\rm iSO}$ versus $V_{\rm dd}$, while Fig. 8(b) shows the measured divider input sensitivity. The input sensitivity dips at the self-resonance frequency, meaning that the divider provides conversion gain and selectivity. To achieve the maximum operating frequency, a very large input signal swing is required, while smaller input swings can be used to injection lock the divider close to its $f_{\rm iSO}$. For the wireless interconnect application,

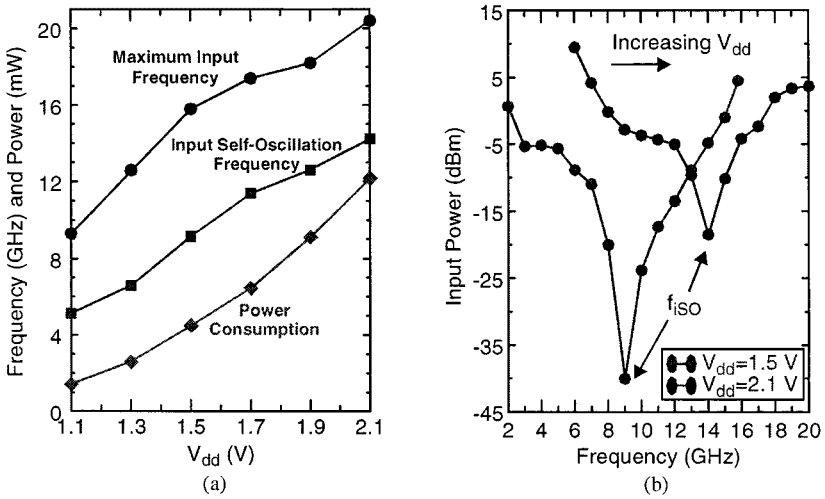

Fig. 8. Measured results for the 0.18-μm frequency divider. (a) Maximum input frequency and self-oscillation frequency versus $V_{\rm dd}$. (b) Input sensitivity versus frequency for $V_{\rm dd} = 1.5$ and 2.1 V.

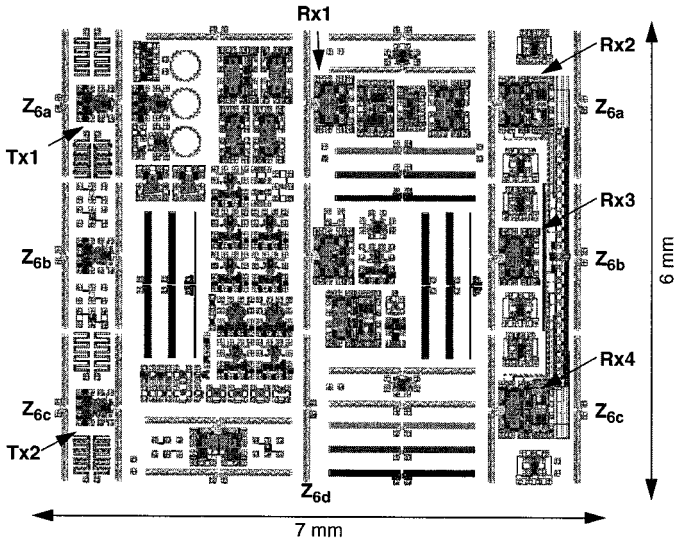

Fig. 9. Layout of the 0.18-μm CMOS test chip showing locations of relevant zigzag antennas (Z_i), clock transmitters (Tx), and clock receivers (Rx).

the input power level to the divider is large enough such that the divider can be locked over approximately 2 GHz. Thus, the system does not rely on the peak conversion gain of the divider for system operation.

IV. Wireless Interconnects

The layout of the 0.18-μm test chip [6] is shown in Fig. 9. The chip area is 7×6 mm^2. Multiple antenna test structures, LNAs, frequency dividers, clock receivers, and clock transmitters have been included. The locations of relevant zigzag antennas (Z_i) have been noted. Clock transmitters (Tx1, Tx2) and receivers (Rx1–Rx4) have been labeled as well. Located in between the antennas are test structures which should interfere with the clock transmission and reception. These test structures contain multiple metal interconnects, vias, substrate connections, passivation openings, and metal-fill patterns (not shown)

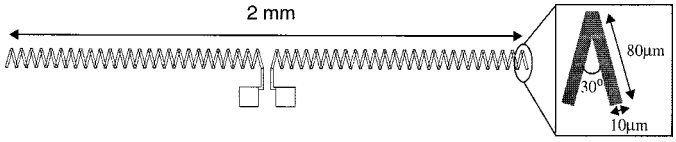

Fig. 10. Layout of a 2-mm-long zigzag dipole antenna.

for metal layers 1–6. Therefore, the density of structures between the antennas is high.

A. On-Chip Antennas

For on-chip antennas, the antenna size is limited by the size of the chip. Therefore, to maximize the antenna's radiation while limiting the physical size of the antenna requires operating at higher frequencies (e.g., $>$15 GHz), corresponding to smaller λ. The dipole antenna length has been limited to 2 mm, corresponding to $\lambda/5$ and $\sim\lambda/3$ at 15 GHz, in silicon dioxide and silicon substrate, respectively. As mentioned earlier, since the antenna is not operating at resonance (i.e., the length is not $\lambda/2$), the antenna impedance has a reactive component. Therefore, this reactance has to be conjugately matched with the impedances of the transmitter and receiver.

The implemented antennas are 2-mm-long zigzag dipole antennas, labeled Z_X in Fig. 9. The zigzag antennas, illustrated in Fig. 10, have a 10-μm trace width, an 80-μm arm element length, and a 30° bend angle. These values were based on the best results currently available from antenna design experiments [20], [21]. Antennas Z_{6a} to Z_{6d} are implemented in metal 6 at various locations throughout the chip, with spacings of $d = \{6.7, 6.7, 6.7, 3.2\}$ mm, for antenna pairs $Z_{\{6a,\,6b,\,6c,\,6d\}}$, respectively. The separation from metal 6 to the 15–25 $\Omega \cdot$ cm substrate is $\sim$7.2 μm. Although the lateral field components partially cancel each other in a zigzag structure, the longitudinal components reinforce each other. Indeed, compared to a linear dipole antenna having the same axial length, a zigzag dipole antenna will have higher gain [20].

The gain between a transmitting/receiving antenna pair can be determined using Friis transmission equation [22], which

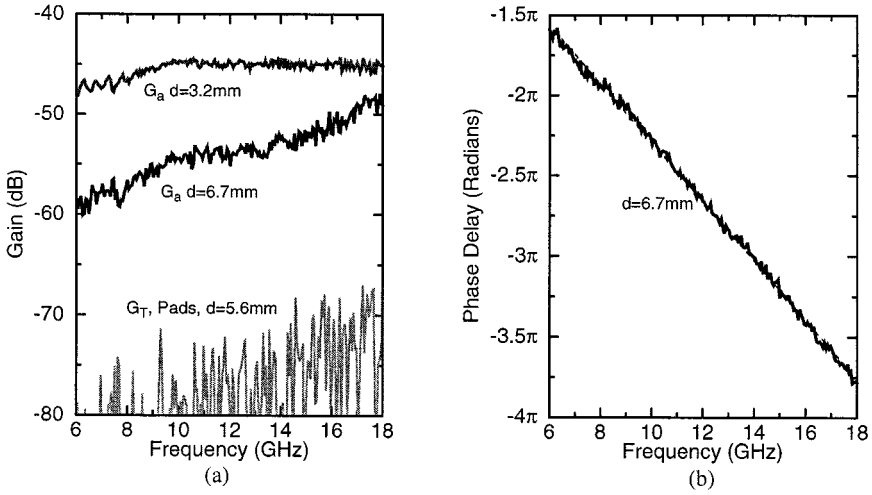

Fig. 11. (a) Antenna transmission gains for $d = 6.7$ mm (Z_{6b}) and 3.2 mm (Z_{6c-6d}). Also shown for reference is the pad transducer gain ($|S_{21}|^2$) at $d = 5.6$ mm. (b) Phase delay of the antenna voltage wave versus frequency for $d = 6.7$ mm.

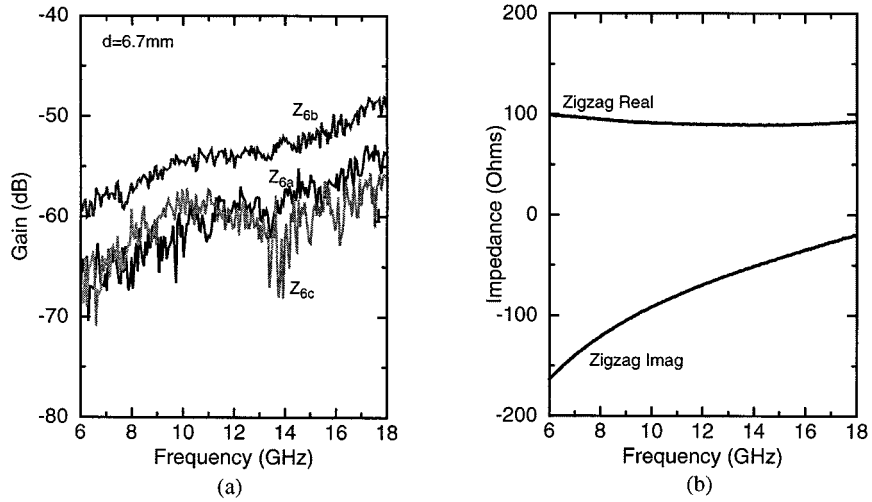

Fig. 12. (a) Antenna transmission gains of metal-6 zigzag antennas ($Z_{6a,6b,6c}$) for $d = 6.7$ mm, demonstrating the effects of interference structures on gain. (b) Zigzag antenna impedance versus frequency.

describes the power received to the power transmitted between two antennas as follows:

$$\frac{P_r}{P_t} = e_t e_r \cdot \left(1 - |\Gamma_t|^2\right)\left(1 - |\Gamma_r|^2\right) D_t D_r \left(\frac{\lambda}{4\pi r}\right)^2 \quad (1)$$

where e_i is an efficiency representing loss in the conductors and dielectrics, Γ_i is the reflection coefficient at the antenna terminals, D_i is the directivity, and λ and r are the wavelength and separation distance, respectively. When characterizing an antenna pair using S-parameters, this Friis transmission equation is equal to $|S_{21}|^2$ [20], which is equal to the transducer gain G_T, when the antennas are measured with 50-Ω transmission lines and termination impedances [23]. To characterize the antenna performance under matched conditions, a transmission gain G_a is defined as

$$G_a = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}. \quad (2)$$

Referring to (1), G_a is equal to the quantity $e_t e_r D_t D_r (\lambda/4\pi r)^2$, and is equal to the power available at the output divided by the power delivered to the input, where both antennas are conjugately matched. Note that in actual system implementations, the antennas would only be matched for a limited frequency range; thus, G_a would only be equal to the actual gain over those frequencies.

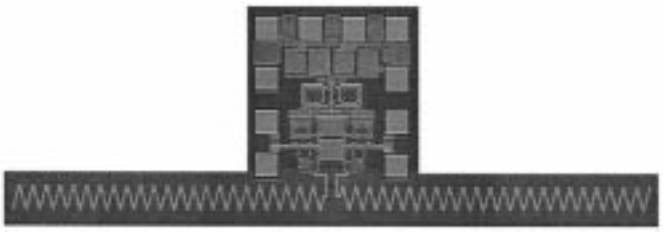

Fig. 13. Die photograph of a 0.18-μm clock transmitter with a zigzag dipole antenna.

A test setup for antenna characterization utilizing a network analyzer has been developed [20]. This setup converts the unbalanced signals from the network analyzer to balanced signals used to excite the antennas. Semi-rigid cables are used to

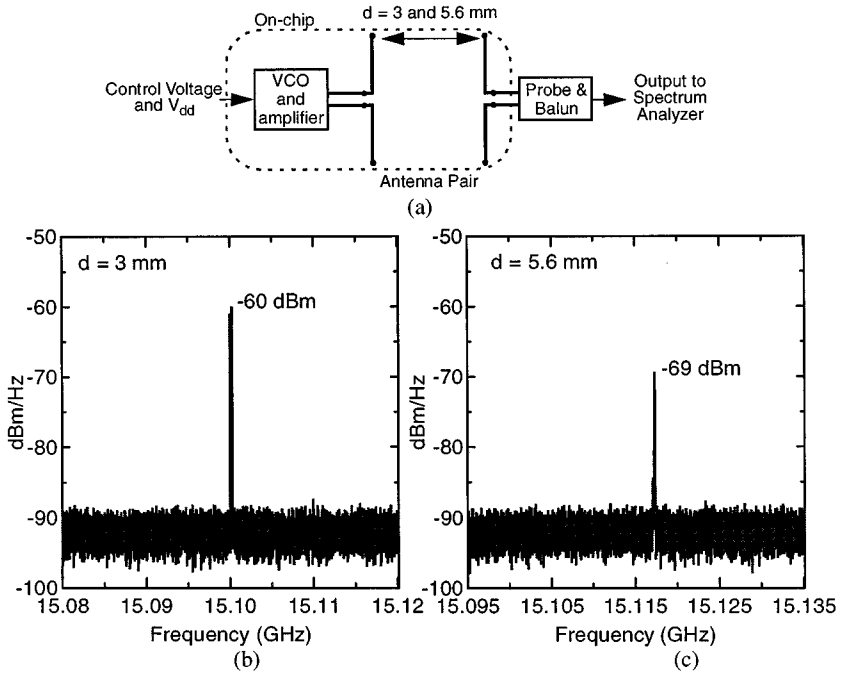

Fig. 14. (a) Diagram of the measurement setup used to characterize the wireless clock transmitters. (b), (c) Received spectra from the clock transmitter across 3- and 5.6-mm separation distances.

increase measurement reliability. The dies are mounted on a glass slide, which is then placed on a 1-cm-thick insulator with κ of 2.

Fig. 11(a) shows the measured zigzag–zigzag transmission gain G_a versus frequency for 6.7- and 3.2-mm separations, corresponding to antenna pairs Z_{6b} and Z_{6b-6d}, respectively. The gain increases with frequency and decreasing separation. At 15 GHz, G_a is -53 and -45 dB for 6.7- and 3.2-mm separations, respectively. Also shown is the transducer gain between two sets of pads separated by 5.6 mm, which is about 20 dB below the transmission gain at 15 GHz. For this measurement situation, the pad-to-pad gain is close to the instrument noise floor. The phase delay between the voltage at the receiving and transmitting antennas for 6.7-mm separation is shown in Fig. 11(b). The phase delay decreases linearly with frequency $(\phi = -\omega l/c_{\text{eff}})$, indicating wave propagation rather than some type of lumped element *RC* coupling [20]. This fact, along with the low pad-to-pad gain, shows conclusively that the signal is propagating from one antenna to the other, and that these waves are launched much more efficiently from the antennas than from the pads alone.

Fig. 12(a) shows G_a versus frequency for three pairs of zigzag antennas. Each pair is separated by 6.7 mm, corresponding to antennas $Z_{6a,6b,6c}$. These results demonstrate the effect of interference structures on antenna gain. As can be seen from Fig. 9, each pair has different types and densities of metal and active structures located in between. The transmission gain changes by 5–10 dB, depending on the antenna and frequency. Also, the antennas have slightly different impedances (not shown), since the reflection coefficient is a function of the metal structures reflecting the transmitted signal back into the antenna. This clearly shows that the structures located around the antenna affect the antenna performance [24].

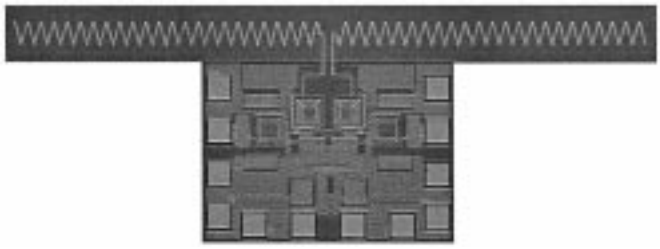

Fig. 15. Die photograph of a 0.18-μm clock receiver with a zigzag dipole antenna.

Fig. 12(b) shows the measured antenna impedance. The zigzag impedance is $\sim$100 Ω with a capacitive reactance. The mismatch loss between the receiving zigzag antenna and the LNA input (which was matched to $\sim$100 Ω) is approximately 0.3 dB at 15 GHz. Therefore, virtually all of the power from the receiving antenna is transferred to the LNA.

B. Clock Transmitter With Integrated Antenna

A die photograph of the clock transmitter with a zigzag antenna is shown in Fig. 13 [6]. The size of the transmitter, including the "unused" portions on either side of the circuit, is 0.64×2 mm^2, while the active areas (excluding pads) is 0.4×0.29 mm^2. The layout is symmetric left-to-right. Multiple substrate connections are included throughout the circuit.

Referring back to Fig. 2, the clock transmitter consists of a VCO connected to an amplifier, which then drives the transmitting antenna. Operation of the clock transmitter is demonstrated by on-chip generation of a global clock signal and reception of this signal using receiving antennas. Fig. 14(a) shows a block diagram of the measurement setup used to test the clock transmitter. The dc control and supply voltages were supplied to a

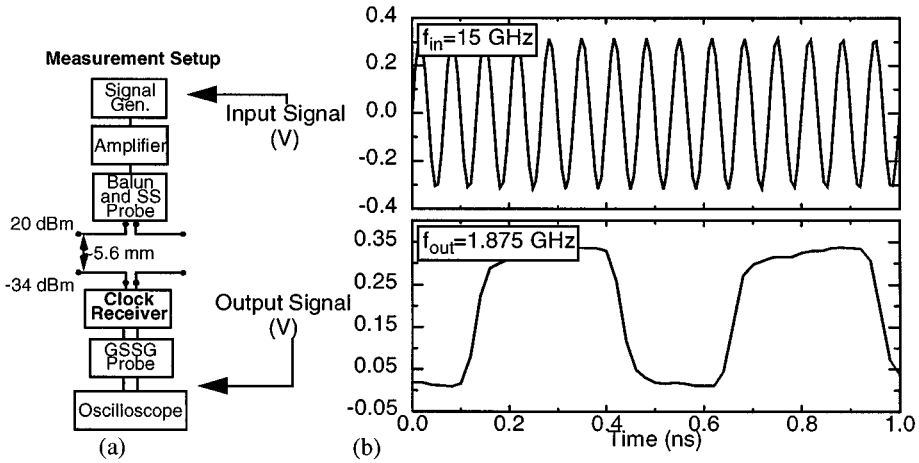

Fig. 16. (a) Diagram of the measurement setup used to characterize the wireless clock receivers. (b) Input and output waveforms for the clock receiver, demonstrating operation of the receiver for a 5.6-mm separation distance at a 15-GHz input frequency.

transmitter driving a zigzag dipole antenna. The output spectrum was then obtained by probing receiving antennas located at 3- and 5.6-mm separations from the transmitting antenna. Fig. 14(b) and (c) show the resultant output spectra measured at 3- and 5.6-mm distances, respectively, having peak output power levels of -60 and -69 dBm at $\sim$15 GHz. The transmitter consumes $\sim$48 mW of power. This is the first demonstration of an on-chip clock transmitter with an integrated antenna.

C. Clock Receiver With Integrated Antenna

A die photograph of the 0.18-μm clock receiver with an integrated zigzag dipole antenna is shown in Fig. 15 [5], [6]. The size of the receiver, including the antenna, is 0.66×2 mm^2, while the active area is 0.37×0.58 mm^2. The receiver consists of a zigzag dipole antenna, a differential LNA with source-follower buffers, an 8:1 frequency divider, and output buffers. To decrease the minimum detectable signal of the receiver, the peak LNA/buffer gain should coincide with f_{iSO} of the frequency divider. To achieve this, the supply voltage of the frequency divider was increased from 1.5 to 2.1 V, increasing f_{iSO} from 9.2 to 14.2 GHz. Operation of the clock receiver is demonstrated by transmission of a global clock signal across the chip, detection of this signal, and generation of a local clock signal by a single clock receiver.

The measurement setup shown in Fig. 16(a) was used to test the clock receiver. The input signal is generated off-chip and externally amplified (note that the input signal plotted in Fig. 16(b) is taken before the external amplifier). The input signal is then transformed into a balanced signal and injected into the on-chip transmitting antenna, with an available power level of $+20.3$ dBm. The output of the receiver located across the chip is then probed and examined using an oscilloscope. Due to driving the 50-Ω load of the oscilloscope, the output swing is reduced.

Two clock receivers (Rx1 and Rx3 from Fig. 9) were tested, having antenna separations of 3.2 and 5.6 mm, respectively. Fig. 16(b) shows plots of the input voltage to the transmitting antenna and the output voltage of the wireless clock receiver, for a 5.6-mm transmission distance (Rx3). This demonstrates operation of the clock receiver with integrated antenna. The input global clock frequency is 15 GHz, and the output local clock frequency is 1.875 GHz (15 GHz divided by 8). Sensitivity measurements show that the MDS of the receiver is -40 dBm. The total power consumption for the receiver is 40 mW. Inferring from the measured zigzag–zigzag antenna pair transmission gain (~ -53 dB) and accounting for mismatch loss in the system, the power delivered to the input of the receiver is -34.3 dBm. As expected, for the 3.2-mm separation, the input power level to the transmitting antenna can be 10 dB lower, since the antenna transmission gain is 10 dB higher.

Previously, using a 0.25-μm CMOS technology, a wireless receiver interconnect with 2-mm *linear* dipole antennas was demonstrated across 3.3 mm at 7.4 GHz [5]. The 0.25-μm receiver had an MDS of -43 dBm, while the available power at the transmitting antenna was $+21$ dBm. Thus, in advancing the technology one generation, the interconnection distance and operating frequency have both been approximately doubled. Using a more advanced CMOS technology allowed the operating frequency to increase, leading to improved antenna performance, which in turn leads to increased interconnection distance.

D. Simultaneous Transmitter and Receiver Operation

By comparing the results from both the transmitter and receiver circuits with integrated antennas, it can be seen that simultaneous operation of these two circuits (i.e., integrated transmitter communicating across the chip to integrated receiver) is *currently* not possible. The MDS of the receiver is -40 dBm, while the power received from the transmitter is -60 and -69 dBm for half-chip and full-chip transmission, respectively. Thus, there is a 20- and 29-dB deficit in "system gain" for achieving a fully integrated half- and full-chip wireless clock distribution system, respectively. The primary reason for this deficit is a reduction in the thicknesses of metals 5 and 6. The thicknesses of these metal layers were half that expected, reducing the inductor Q's by approximately half. According to simulations, this 50% Q degradation reduces the system gain by approximately 20 dB, described as follows. The voltage gain of an inductively loaded amplifier is proportional to the inductor Q. Hence, a 50% Q reduction will decrease the S_{21} of the LNA by 6 dB. Likewise, the gain of the class-A preamplifier in the

output amplifier is also decreased by 6 dB. Simulations show that the gain of the pseudo class-E stage in the output amplifier is reduced by 1 dB, since the inductive load is shunted by the antenna impedance. Finally, the VCO bias current is adjusted to maximize the voltage swing across the tank; thus, its g_m and, hence, power consumption are increased as Q decreases. To increase the VCO power consumption, V_{g7} was decreased, which also decreased the dc bias point of the output amplifier. Simulations show that this decreased the gain by another 7.5 dB. All of these yield a 20.5-dB degradation in system gain. Therefore, with the planned metal 5 and 6 thicknesses, a fully integrated half-chip wireless interconnection should have been possible. Despite the reduced metal thickness, reasonable circuit performance is obtained, demonstrating the benefits of copper metallization over aluminum.

V. Conclusion

In this paper, both 15-GHz RF CMOS circuits and wireless interconnects have been presented. Individual RF circuit blocks operating at $\sim$15 GHz have been demonstrated, including a 14.4-GHz LNA with 21 dB of gain, a frequency divider with maximum input frequencies of 15.8 GHz at 1.5-V $V_{\rm dd}$ and 20.4 GHz at 2.1-V $V_{\rm dd}$, a 15-GHz VCO with -113 dBc/Hz phase noise at a 3-MHz offset, and an output amplifier capable of delivering -13 dBm of power at 15 GHz. These circuits are commonly found in conventional transceiver architectures; thus, these results show that 0.18-μm CMOS technology can potentially be used for RF applications operating above 10 GHz.

In addition to the 15-GHz RF circuit results, a 15-GHz wireless interconnect system has been demonstrated. Measured antenna characteristics for both chips show that antenna gain increases with frequency where the antenna becomes electrically longer. Also, the presence of interference structures between the antennas can alter the gain by 5–10 dB. Additionally, the phase versus frequency response for the antennas is linear, indicating wave propagation, while the gain between two sets of pads is at least 20 dB less than that for the antennas. These two facts together show that the signal coupling is due to wave propagation, and that these waves are launched much more efficiently from the antennas than from just the pads. A wireless transmitter with an integrated antenna generated and transmitted a 15-GHz global clock signal across a 5.6-mm test chip, and this signal was detected using receiving antennas. A wireless clock receiver with an integrated antenna detected a 15-GHz global clock signal supplied externally to an on-chip transmitting antenna located 5.6 mm away from the receiver, and generated a 1.875-GHz local clock signal. These results demonstrate wireless interconnection at 15 GHz for a 5.6-mm distance. This is the first known demonstration of an on-chip clock transmitter with an antenna and the second demonstration of a clock receiver. Finally, this result has basically doubled the distance and frequency of wireless interconnection presented in [5], by advancing the technology one generation. In summary, this paper has shown that it is possible to use integrated antennas and CMOS circuits to send signals from one side of a chip to another. Such a wireless system can enable transmission of high frequency signals with little to no dispersion over large distances at the speed of light using conventional CMOS technology

Acknowledgment

The 0.18-μm CMOS technology was obtained through the 2000 SRC Copper Design Contest, sponsored by the Semiconductor Research Corporation (SRC), Novellus, Speed-Fam IPEC, and United Microelectronics Corporation (UMC). The authors are grateful to the sponsors for providing access to this technology. Special recognition is merited by D. Edwards (SRC) and M. Lu (UMC) for their efforts with the contest. The authors would also like to acknowledge K. Kim, formerly with the University of Florida and currently with RF Micro Devices, for his antenna development.

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