Intrinsic Fluctuations in Sub 10-nm Double-Gate MOSFETs Introduced by Discreteness of Charge and Matter

Andrew R. Brown, Asen Asenov, and Jeremy R. Watling

***Abstract*—We study, using numerical simulation, the intrinsic parameter fluctuations in sub 10 nm gate length double gate MOSFETs introduced by discreteness of charge and atomicity of matter. The employed "atomistic" drift-diffusion simulation approach includes quantum corrections based on the density gradient formalism. The quantum confinement and source-to-drain tunnelling effects are carefully calibrated in respect of self-consistent Poisson-Schrödinger and nonequilibrium Green's function simulations. Various sources of intrinsic parameter fluctuations, including random discrete dopants in the source/drain regions, single dopant or charged defect state in the channel region and gate line edge roughness, are studied in detail.**

***Index Terms*—Charge carrier processes, lithography, MOSFETs, semiconductor device doping, semiconductor device modeling, stochastic processes.**

I. Introduction

ACCORDING to the 2001 edition of the International Technology Roadmap for Semiconductors [1], MOSFETs will reach sub 10-nm physical channel length by 2016. This is supported by simulation studies, which indicate that the field effect control of the gate current can be maintained to channel lengths below 5 nm where direct source-to-drain tunnelling may dominate, reducing the gate control particularly in the subthreshold region [2], [3]. Properly scaled MOSFETs with 15-nm channel length and conventional architecture have already been demonstrated by leading semiconductor manufacturers [4]. There is, however, a broad agreement that the scaling of the field effect transistor below the 15-nm barrier requires an intolerably thin gate oxide and unacceptably high channel doping, and therefore advocates a departure from the conventional MOSFET concepts [5]. One of the most promising new device structures, scalable to dimensions below 10 nm, is the double-gate MOSFET studied extensively in the last couple of years [2], [3], [6]. The double-gate devices do not require channel doping to operate and therefore are considered to be inherently resistant to random dopant induced parameter fluctuations, which might reach an unacceptable level in their conventional counterparts.

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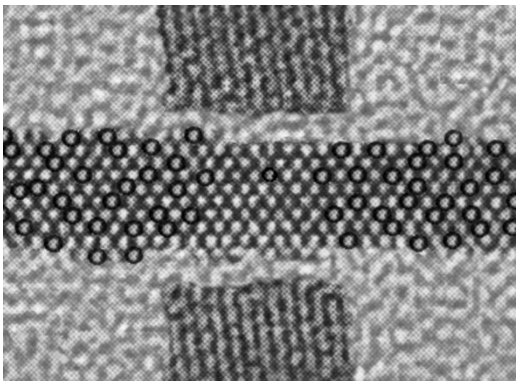

Fig. 1. Impression of a 4-nm gate length double gate MOSFET illustrating the various sources of intrinsic parameter fluctuations.

In this paper, we carefully examine, using three-dimensional (3-D) 'atomistic' drift-diffusion simulations [7], intrinsic parameter fluctuations in sub-10-nm double-gate MOSFETs introduced by the discreteness of charge and atomicity of matter. The quantum confinement effects in the thin silicon body of the double-gate MOSFETs and the source-to-drain direct tunnelling are taken into account using the density gradient formalism [8], which has been carefully calibrated in respect of rigorous quantum simulations based on self-consistent Poisson-Schrödinger [9] and nonequilibrium Green's functions [2] simulations.

An impression of a 4-nm gate length double-gate MOSFET which illustrates some of the atomic scale sources of intrinsic parameter fluctuations is presented in Fig. 1. We consider: 1) the random discrete dopants in the source and drain regions [10]–[12]; 2) individual charges in the active region of the device associated with the background doping, fixed interface charge and interface states [13]; and 3) the line–edge roughness (LER) of the gate edge [14]–[16].

II. Simulation Approach

The simulation experiments in this study were performed using the Glasgow "atomistic" device simulator which is described in detail elsewhere [7], [11]. Our 3-D drift-diffusion simulator includes the density gradient formalism, to account for quantum mechanical effects [17]. Although the drift-diffusion approach does not properly represent the nonequilibrium carrier dynamics in nanometer scale devices it is a useful approximation when looking at relative fluctuations in the device parameters introduced by the electrostatics of random

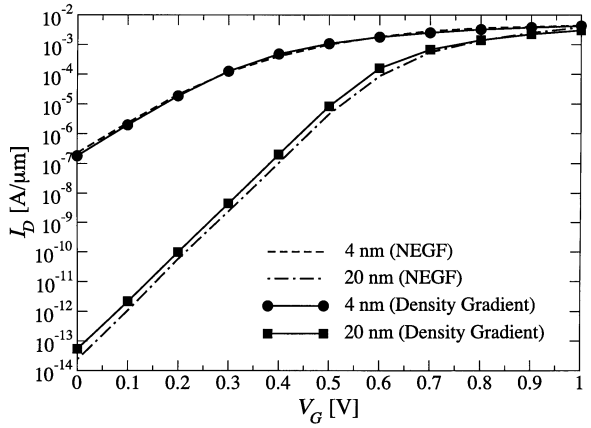

Fig. 2. Current-voltage characteristics for 20 and 4-nm channel length double-gate MOSFETs. Comparison between density gradient and nonequilibrium Green's function simulations.

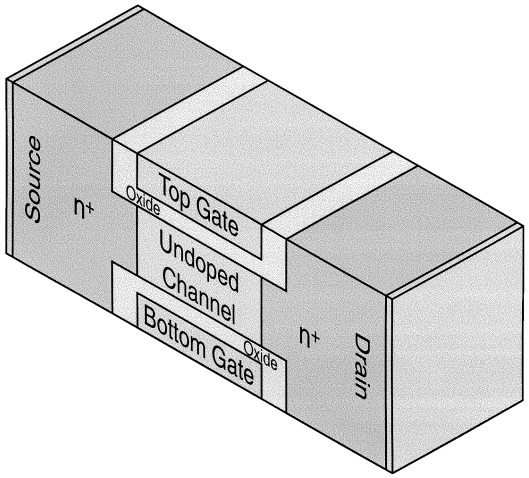

Fig. 3. Schematic illustration of the simulated double-gate MOSFETs.

discrete dopants, LER, and interface roughness. At present, it remains the only practical technique for studying the statistical distribution of parameters of interest such as threshold voltage, ON and OFF current by 3-D simulation of large ensembles of devices with different discrete dopant distributions or gate shapes.

It is well known that the density gradient approach requires calibration against more rigorous quantum mechanical simulations [8], [17]. In the simulations of sub 10-nm double-gate MOSFETs presented here, the calibration was carried out independently in respect of the confinement effects in the inversion layer and in respect of the source-to-drain tunnelling using the components of the effective mass which are normal, $m_\perp$, and parallel, $m_{||}$, to the Si/SiO_2 interface in a modified density gradient equation

$$\frac{2\hbar^2}{12q\sqrt{n}}\left[\frac{1}{m_{||}}\left(\frac{\partial^2\sqrt{n}}{\partial x^2}+\frac{\partial^2\sqrt{n}}{\partial y^2}\right)+\frac{1}{m_\perp}\frac{\partial^2\sqrt{n}}{\partial z^2}\right] = \phi_n-\psi+\frac{kT}{q}\ln\left(\frac{n}{n_i}\right) \quad (1)$$

where z is the direction normal to the interface, ψ is the electrostatic potential, ϕ_n is the quasi-fermi potential, n is the electron concentration and n_i is the intrinsic electron concentration.

The right-hand side of (1) represents Boltzmann statistics which, in this case, are used for modeling the heavily doped source and drain regions of the device. This certainly overestimates the screening in our simulations and will therefore result in lower figures for the fluctuations of the device parameters. There are other uncertainties which have also to be resolved conceptually in the atomistic simulation of heavily doped regions, including bandgap narrowing, which also remain outside the scope of this paper. Due to the sheer computational intensity of this work, we have restrained ourselves to Boltzmann statistics, which are computationally more efficient and give a lower estimate to the fluctuations which might be expected in these devices.

The vertical effective mass $m_\perp$ has been adjusted to reproduce the threshold voltage shift and the inversion layer charge distribution obtained using one-dimensional full-band Poisson-Schrödinger simulations [9]. Due to the quantum confinement the peak in concentration occurs in the middle of the channel, compared to the classical distribution, which peaks at both oxide interfaces. It is therefore important to correctly account for vertical quantum confinement in the double-gate MOSFETs.

TABLE I

DIMENSIONS OF THE DOUBLE-GATE MOSFETS USED FOR THIS INVESTIGATION, SCALING FROM A 10-NM CHANNEL LENGTH DOWN TO 4 NM

Channel length [nm]	Channel width [nm]	Silicon body thickness [nm]	Oxide thickness [nm]
10	10	4.0	1.0
8	8	3.7	0.8
6	6	3.3	0.6
4	4	3.0	0.4

Recently, we have demonstrated that the density-gradient approach can, at least qualitatively, reproduce the impact of the direct source-to-drain tunnelling on the subthreshold characteristics of double-gate MOSFETs [18], and the tunnelling component of the current is sensitive to the lateral effective mass $m_{||}$. For the simulation presented in this work we have calibrated $m_{||}$[19] with respect to rigorous quantum simulations based on the nonequilibrium Green's functions formalism performed at NASA Ames Research Center [20]. Current-voltage characteristics, showing the agreement between the calibrated drift-diffusion simulations with density gradient quantum corrections and nonequilibrium Green's function results are shown in Fig. 2.

III. RESULTS AND DISCUSSION

We investigate a family of well-scaled double-gate MOSFETs, schematically illustrated in Fig. 3. The channel lengths range from 10 nm down to 4 nm with the scaled dimensions given in Table I. A fine discretization mesh is required to resolve the fluctuations in potential resulting from discrete dopants and LER. A maximum grid spacing of 0.5 nm is used in the active region of the simulated devices.

A. Random Discrete Dopants in the Source/Drain

While there may be no dopants within the channel region of the double-gate MOSFETs there are unavoidable random

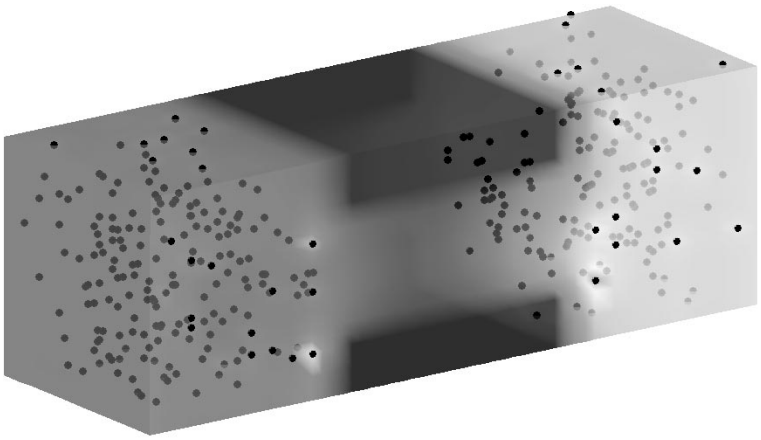

Fig. 4. Impact of the discrete dopants in the source and drain region of a 10 × 10 × 4-nm double-gate MOSFET on the potential distribution. The location of the random dopants are also shown.

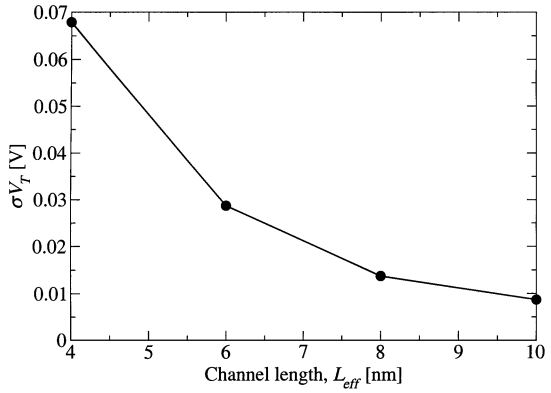

Fig. 5. Standard deviation in threshold voltage, σV_T, due to random discrete dopants in the source and drain of double-gate MOSFETs with different channel lengths.

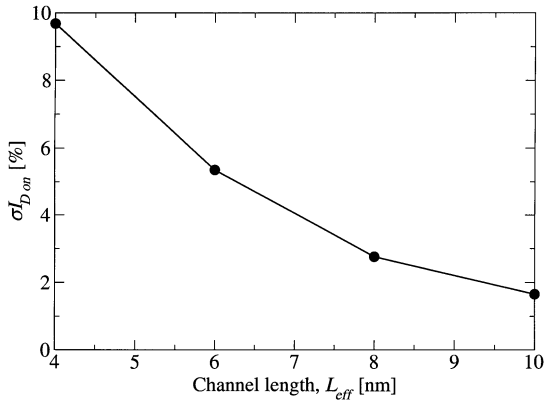

Fig. 6. Standard deviation in on-current, σI_{on}, due to random discrete dopants in the source and drain of double-gate MOSFETs with different channel lengths.

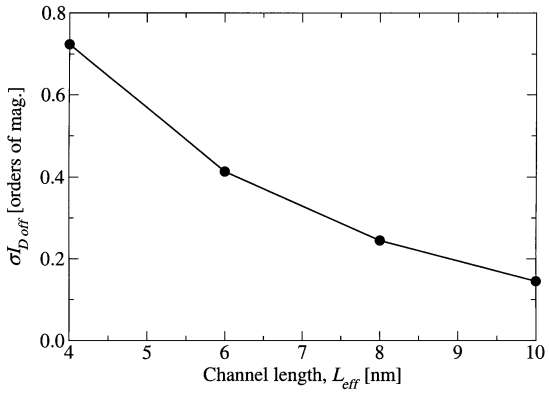

Fig. 7. Standard deviation in off-current, $\sigma \mathrm{Log}_{10}(I_{\mathrm{off}})$ expressed in orders of magnitude, due to random discrete dopants in the source and drain of double-gate MOSFETs with different channel lengths.

discrete dopants in the source/drain regions. The individual dopants are introduced in the simulation using a rejection technique described in [7]. Fig. 4 illustrates their impact on the potential distribution in the 10-nm device. In conventional MOSFETs, where fluctuations due to the discrete nature of the channel doping dominate, the additional effect of the atomistic doping in the source and drain is usually small [10]. The placement of random discrete dopants in the source/drain regions results in fluctuations in the effective channel length along the width of the device on a scale comparable to the average distance between the dopants. At typical source/drain doping concentrations in the range of 10^{20} cm^{-3} the average distance between the dopants is about 2 nm. When devices are scaled below 10 nm, these variations constitute a large proportion of the channel length and become accountable for significant variations in the device parameters.

The dependence of the standard deviation in threshold voltage, σV_T, on-current, σI_{on}, and off-current, σI_{off}, as a function of the channel length are shown in Figs. 5–7 respectively, for the double-gate MOSFETs described in Table I. In each case, the magnitude of the fluctuations increases dramatically as the channel length reduces from 10 nm to 4 nm. For the 4-nm device the standard deviation in threshold voltage is approximately 0.07 V. Assuming a $\pm 3\sigma$ spread around the mean in a normal distribution of V_T this gives a range of approximately ± 0.2 V around the nominal threshold voltage of $V_T \approx 0.2$ V. This means that a significant fraction of the devices on a chip with a billion transistors will not turn OFF.

The dependence of σV_T on channel length and width is stronger than the classical $1/\sqrt{W \times L}$ relationship expected for threshold voltage fluctuations induced by random dopants in the channel region. This could be attributed to short-channel

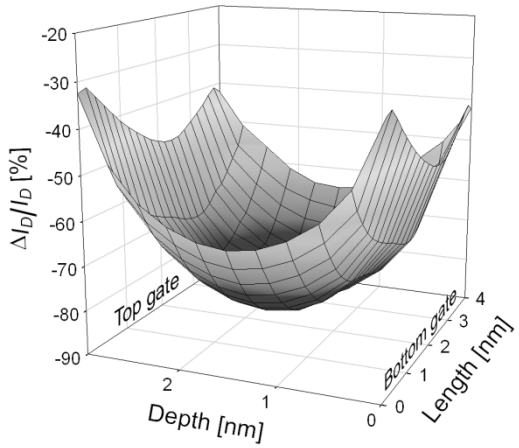

Fig. 8. Percentage change in current when an negative discrete charge is present at a particular location within the channel in a $4 \times 4 \times 3$-nm device. The maximum reduction in current is 84%.

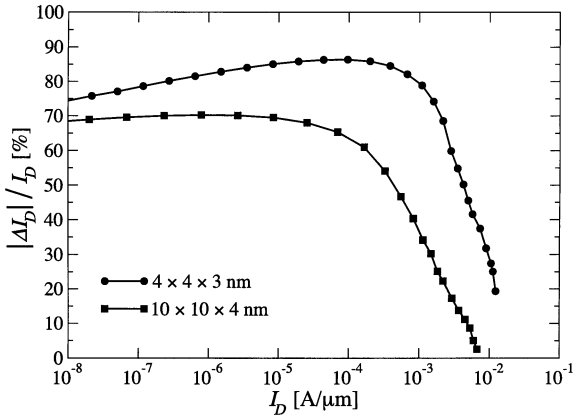

Fig. 9. Magnitude of the reduction in current associated with a negative discrete charge (e.g., an acceptor) present in the middle of the channel as a function of the current itself.

effects in our devices. For example, it has been shown in [21] that short-channel effects are responsible for an increase in the fluctuations in conventional MOSFETs.

In the subthreshold region where the drain current, I_D, depends exponentially on the applied gate voltage, V_G, such large variations in threshold voltage will lead to massive fluctuations in I_{off}. This exponential dependence also means that while V_T follows a normal distribution, I_{off} does not and one has to perform statistical analysis on $\log(I_{\text{off}})$. For this reason, Fig. 6 shows the standard deviation of $\log_{10}(I_{\text{off}})$ expressed in terms of orders of magnitude. Again, considering a $\pm 3\sigma$ spread this means that I_{off} varies over a four orders of magnitude range in the 4-nm device.

B. Single Charges in the Channel Region

Even in undoped channel devices the unavoidable background doping introduces a finite possibility of at least one ionised dopant (acceptor or donor) being present at a random location within the channel. Also, if an electron/hole becomes trapped in a defect state at the interface or in the silicon body it will introduce a fixed charge in the channel region [22]. These potential sources of localized single charge will have an electrostatic effect on the channel potential introducing, for example, in the case of acceptor or trapped electron in *n*-channel double-gate MOSFET, a localized barrier to current flow, and a corresponding shift in the threshold voltage [13].

The change in the drain current at threshold as a function of the position of a single negative charge in the device (either acceptor or trapped electron) is mapped for the 4-nm double-gate MOSFET in Fig. 8. The mapping is done for a vertical cross section running through the middle of the channel from source to drain. Due to the quantum distribution, resulting in the majority of current flowing in the plane through the middle of the device, a charge trapped in the centre of the channel produces the largest effect. For the range of MOSFETs investigated here the maximum reduction in the current increases from 69% in the 10-nm device to 84% in the 4-nm one, where the additional charge has more influence on the channel of the device due to a thinner Silicon body.

The relative reduction in the current as a function of the current itself is plotted in Fig. 9, for the 'worst possible case' scenario where the additional charge is in the centre of the channel. It is clear that the largest effect is in the subthreshold regime where the density of mobile charge in the channel is low. Above threshold, at higher drain currents in Fig. 9, the electrons in the channel screen the potential of the additional fixed charge, reducing its impact on the current flow, but not eliminating it completely.

C. LER

LER inherent to the lithography process and the subsequent pattern transfer is not a new phenomenon. Yet, the imperfections caused by LER effects have caused little worry for production lines over the years since the critical dimensions of devices were more than an order of magnitude larger than the roughness. However, it becomes increasingly difficult to reduce LER below the few nanometers limit determined by the molecular structure of commonly used resists. Due to the continuing aggressive scaling to the sub 100-nm regime it becomes an increasingly significant fraction of the gate length. At the dimensions being considered here for double-gate MOSFETs LER is of the same order of magnitude as the channel length, introducing significant intrinsic parameter fluctuations.

Since the formation of LER is a stochastic event, a proper description and analysis of this phenomenon requires a statistical approach. Realistic "rough" lines produced by a lithography process can be statistically described by their rms amplitude, Δ, and correlation length, Λ, which indicate the vertical and lateral extent of the roughness respectively. In the following simulations, we assume a Gaussian autocorrelation function for the random line edge as the very high frequency components that are characteristic of an exponential autocorrelation function would be smoothed by diffusion and annealing. The power spectrum of this function, obtained by Fourier transform, is used to generate the amplitudes in a complex array. The phases are chosen randomly, which produces the random nature of the generated line obtained by inverse Fourier transform of the complex array [16]. We also assume that the LER of the gate results in the p-n junctions in the MOSFET exhibiting the same

Fig. 10. Potential distribution in a double-gate MOSFET illustrating the effect of LER on the source and drain junctions. LER is defined statistically by its rms amplitude, Δ, and correlation length, Λ.

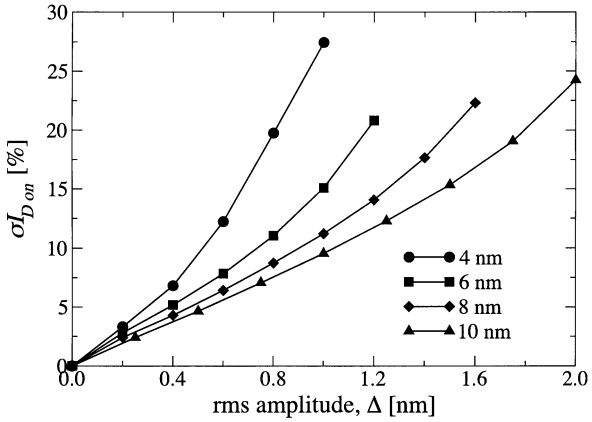

Fig. 12. Standard deviation in on-current, σI_{on}, due to LER with rms amplitude Δ for double-gate MOSFETs with different channel lengths.

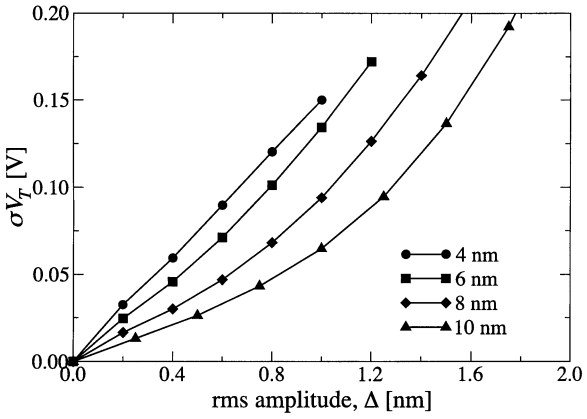

Fig. 11. Standard deviation in threshold voltage, σV_T, due to LER with rms amplitude Δ for double-gate MOSFETs with different channel lengths.

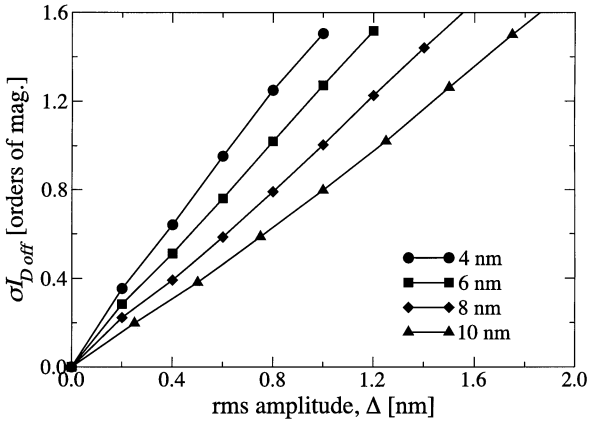

Fig. 13. Standard deviation in off-current, $\sigma \mathrm{Log}_{10}(I_{\mathrm{off}})$ expressed in orders of magnitude, due to LER with rms amplitude Δ for double-gate MOSFETs with different channel lengths.

rms amplitude and correlation length. The random lines used to describe the source and drain junctions are assumed to be uncorrelated. The typical potential distribution in a double-gate MOSFET with LER is illustrated in Fig. 10.

The analysis of published LER data from advanced lithography processes in various labs [16] found that the current value of LER (which is defined as being 3Δ) is 5 to 6 nm (i.e., $\Delta \approx 2$ nm) and, rather worryingly, is not reducing for shorter channel length technologies. The requirements from the International Technology Roadmap for Semiconductors for the devices investigated here is for an LER of less than 1 nm.

The dependence of the standard deviation in threshold voltage, σV_T, the on, σI_{on}, and the off current, σI_{off}, on the rms amplitude, Δ is illustrated in Figs. 11–13 respectively for the set of double-gate MOSFETs with different channel length. For the data presented in all three figures the correlation length is $\Lambda = 5$ nm. σI_{off} is again shown in terms of orders of magnitude. As one would expect, the fluctuations increase as Δ increases. It is clear that LER must be reduced from its current level if sub 10-nm devices are to be of practical use near the end of the Roadmap. Even if roadmap requirements are met (i.e., $\Delta \approx 0.3$ nm) the fluctuations are still of a significant magnitude, with V_T covering a range of approximately ± 0.15 V for the 4-nm device.

IV. Conclusion

Double-gate MOSFETs are proving to be a promising architecture for the scaling of devices to sub-15-nm dimensions. The undoped nature of the channel means that they are less susceptible to intrinsic parameter fluctuations due to the random number and location of dopants in the channel region, which is an increasing problem accompanying the scaling of the conventional MOSFET.

However, we have shown that double-gate MOSEFTs are susceptible to other sources of intrinsic parameter fluctuations. The effect of random dopants within the source and drain, while not a significant contributor to fluctuations in current conventional MOSFETs, will become one of the dominating sources of fluctuations when the double-gate devices are scaled below 10 nm.

Random telegraph noise due to the trapping and de-trapping of electrons in lattice defects may result in large current fluctuations, which will be different for each device within an integrated circuit. The presence of even a single dopant within the silicon body will produce significant variations from device to device.

LER inherent to current fabrication processes will be reflected in roughness of the p-n junctions of the device. As such, each device will have a randomly varying channel length. If

the present apparent limit of LER of approximately 5 nm is not reduced drastically then this will cause serious problems for devices with 10-nm channel lengths. Even if roadmap requirements are achieved LER will probably be the major contributor to parameter fluctuations in sub-10-nm double-gate MOSFETs.

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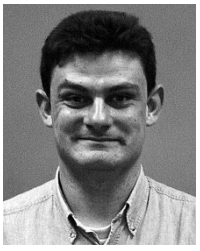
He has ten years of industry experience as the Head of the Process and Device Modeling Group, Institute of Microelectronics, Sofia, developing one of the first integrated process and device CMOS simulators IMPEDANCE. During 1989–1991 he was a Visiting Professor at the Physics Department, Technical University, Munich, Germany. In 1991, he joined the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow, U.K., and is currently a Professor of Device Modeling and the Head of Department. As a Leader of the Device Modeling Group and Academic Director of the new Atomistic and Device Simulation Centre, he co–ordinates the development of 2-D and 3-D device simulators and their application in the design of advanced semiconductor devices. He has over 200 publications in process and device modeling and simulation, semiconductor device physics, "atomistic" effects in ultra-small devices and parallel computing.



Jeremy R. Watling was born in Norwich, Norfolk, U.K., in 1973. He received the Bachelor's degree in physics and the Ph.D degree from the University of East Anglia, Norwich, U.K., in 1995 and 1998, respectively.

Since then, he has been with the University of Glasgow, Glasgow, U.K., working on a large EPSRC collaborative grant. His research interests include Monte Carlo and drift diffusion device simulation, especially the use of quantum corrections in both drift diffusion and particle simulations. He has authored and coauthored over 30 papers in the area of semiconductor simulation.

Dr. Watling was awarded the physics prize for his undergraduate studies and the Best Paper Award at the 1998 International Society for Optical Engineers (SPIE) Conference.