Intrinsic Threshold Voltage Fluctuations in Decanano MOSFETs Due to Local Oxide Thickness Variations

Asen Asenov, *Member, IEEE*, Savas Kaya, and John H. Davies

***Abstract*—Intrinsic threshold voltage fluctuations introduced by local oxide thickness variations (OTVs) in deep submicrometer (decanano) MOSFETs are studied using three-dimensional (3-D) numerical simulations on a statistical scale. Quantum mechanical effects are included in the simulations employing the density gradient (DG) formalism. The random Si/SiO$_2$ and gate/SiO$_2$ interfaces are generated from a power spectrum corresponding to the autocorrelation function of the interface roughness. The impact on the intrinsic threshold voltage fluctuations of both the parameters used to reconstruct the random interface and the MOSFET design parameters are studied using carefully designed simulation experiments. The simulations show that intrinsic threshold voltage fluctuations induced by local OTV become significant when the dimensions of the devices become comparable to the correlation length of the interface. In MOSFETs with characteristic dimensions below 30 nm and conventional architecture, they are comparable to the threshold voltage fluctuations introduced by random discrete dopants.**

***Index Terms*—MOSFETs, numerical simulation, oxide thickness fluctuation, quantum effects, 3-D threshold.**

I. Introduction

THE scaling of the MOSFET to decanano (sub-50-nm) dimensions near the end of the International Technology Roadmap for Semiconductors [1] involves aggressive reduction in the gate oxide thickness [2]. Prototype MOSFETs with conventional architecture, gate length of 30 nm, and oxide thickness below 10 Å have already been successfully demonstrated [3]. In such devices, not only the discrete and random dopant charge [4]–[6], but also the atomic scale roughness of the Si/SiO$_2$ and gate/SiO$_2$ interfaces will introduce significant intrinsic parameter fluctuations. Indeed, when the oxide thickness is equivalent to only a few silicon atomic layers, the atomic scale interface roughness steps [7] will result in significant oxide thickness variation (OTV) within the gate region of an individual MOSFET. The unique random pattern of the gate oxide thickness and interface landscape makes each decanano MOSFET different from its counterparts and leads to variations in the surface roughness limited mobility, gate tunnelling current [8], [9], and real [10] or apparent threshold voltage [11] from device to device.

Manuscript received May 14, 2001; revised September 20, 2001. This work was supported by NASA-Ames Grant NAG 2-1241. The review of this paper was arranged by Editor J. Vasi.

A. Asenov and J. H. Davies are with the Device Modeling Group, Department of Electronics and Electrical Engineering, The University of Glasgow, Glasgow G12 8LT, U.K. (e-mail: A. Asenov@elec.gla.ac.uk).

S. Kaya was with the Device Modeling Group, Department of Electronics and Electrical Engineering, The University of Glasgow, Glasgow G12 8LT, U.K. He is now with the Russ College of Engineering, Ohio University, Athens, OH 45701 USA.

Publisher Item Identifier S 0018-9383(02)00240-X.

Similar to the simulation of random dopant fluctuation effects [12], the numerical study of local oxide thickness fluctuation effects requires three-dimensional (3-D) statistical simulations of ensembles of MOSFETs with macroscopically identical design parameters but with microscopically different oxide thickness/interface patterns. It is also important to include quantum mechanical confinement effects [13], which push the inversion layer away from the rough interface and smooth the spatial inversion charge variations [14] compared to classical simulations.

In this paper, we use 3-D numerical simulations on a statistical scale to investigate intrinsic threshold voltage fluctuations induced by random local OTV in decanano MOSFETs with gate oxide thickness in the range 1–3 nm. We demonstrate the importance of this phenomenon in carefully designed simulation examples, and explore the extent of its impact on the next generation decanano MOSFETs. Quantum mechanical corrections are included in the simulations using the density gradient (DG) formalism [14], [15]. At this stage, the simulations reflect the electrostatic effects associated with the OTVs, but do not include variation in the interface-roughness limited mobility and the gate tunnelling current.

Section II describes in detail our simulation approach. After a brief introduction of the simulator itself, we give details about the generation of the random oxide interface. The importance of the quantum corrections introduced using the DG algorithm is also illustrated in a specifically designed simulation experiment. The results of the systematic simulation study are presented and discussed in Section III. They highlight both the impact of the parameters used to generate the random interface and the device design parameters on the intrinsic threshold voltage fluctuations induced by random OTVs. The scale of this phenomenon is compared with the random dopant induced threshold voltage fluctuations in identical devices. The conclusions are drawn in section IV.

II. Simulation Approach

The results presented in this paper are obtained using a hierarchical 3-D drift-diffusion simulator [12] with DG quantum corrections [15], originally designed for studying random dopant fluctuation effects in decanano MOSFETs. Bearing in mind that, depending on the silicon substrate orientation [7], the interface roughness steps are on the scale of 0.2–0.3 nm, the proper resolution of the OTV effects in the simulation of individual MOSFETs require a 3-D solution with very fine discretization near the interface. Continuous doping charge is used in most of the simulations instead of random

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discrete dopants in order to isolate the threshold voltage fluctuation effects associated with OTV. The requirement for statistical analysis and interpretation of the results transforms the problem effectively into a four-dimensional one, where the fourth dimension is the size of the statistical sample of devices with identical design parameters but microscopically different pattern of gate oxide thickness/interface. Statistical samples of 200 MOSFETs are simulated and analyzed for each combination of device design and interface roughness parameters producing typically one data point on the graphs, which will be presented later. In order to save computational time in the laborious statistical simulation experiments, similarl to [15], the simulations are restricted to low drain voltage. Current criterion $I_T = 10^{-8} W_{\mathrm{eff}}/L_{\mathrm{eff}}[A]$, where W_{eff} and L_{eff} are the effective channel width and length, respectively, is used to estimate the threshold voltage of an individual device. Since the threshold voltage is extracted in the subthreshold region, where the current depends exponentially on the gate voltage, the choice of the mobility model has a negligible effect on the accuracy of the presented results.

A. Modeling the Interface

The exact details of the Si/SiO_2 interface are still the subject of intensive research despite a constant interest from industry and academe over the last couple of decades. Some of the difficulties in the past stemmed from employing transmission electron microscopy (TEM) which is a two-dimensional (2-D) projection technique to study an inherently 3-D and chemically incoherent interface [16], [17]. In addition, sensitivity to the ambient conditions during fabrication, and to the material quality on either side of the interface, can often create further complications. However, the significant advance during the last decade in ultra-high-resolution analytic techniques, including atomic force microscopy (AFM) [18], scanning reflection electron microscopy (SREM) [19], surface second harmonic generation, and X-ray scattering analysis [20], has advanced significantly the understanding of the Si/SiO_2 interface.

The random 2-D surfaces used to represent the boundary between the oxide and the silicon and/or between the oxide and the gate material in our simulation are constructed using standard assumptions for the auto-correlation function of the interface roughness. Generally, the interface is described by a Gaussian or exponential auto-correlation function with a given correlation length Λ and rms height Δ [17]. The corresponding power spectrum can be obtained by 2-D Fourier transformation (in radial coordinates). In order to reconstruct the interface, we generate in the Fourier domain a complex $N \times N$ matrix. The magnitude of the elements of this matrix follows the power spectrum of the chosen correlation function, while the phase is selected at random. Several conditions [21] must be satisfied to ensure that the corresponding 2-D surface in real space, obtained by inverse Fourier transformation, represents a real function. The "analog" random 2-D surface obtained using this procedure is than quantized in steps to take into account the discrete nature of the interface roughness steps associated with the atomic layers in the crystalline silicon substrate [7]. The step height is approximately 0.3 nm for the (001) interface.

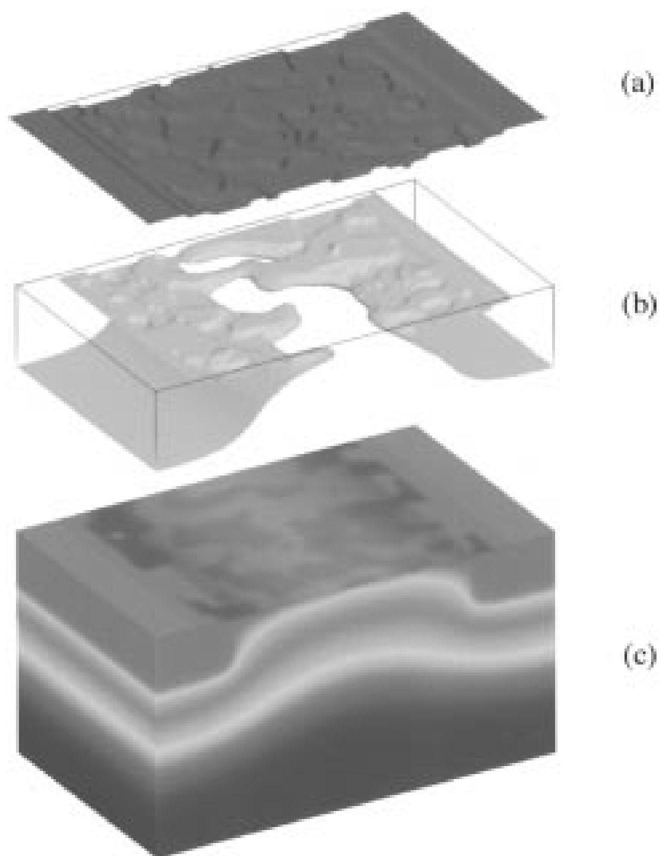

Fig. 1. (a) Typical profile of the random Si/SiO_2 interface in a 30×30 nm^2 MOSFET, followed by (b) an equiconcentration contour obtained from DG simulations, and (c) the potential distribution.

A typical random Si/SiO_2 interface, generated according to the above described procedure and used in the simulation of a 30×30 nm^2 MOSFET described in detail in Section III, is shown at the top of Fig. 1. The interface has been reconstructed using a power spectrum corresponding to a Gaussian correlation function. Only the roughness of the Si/SiO_2 interface was introduced in the simulations and the gate/SiO_2 interface was flat. The potential distribution at threshold voltage is shown at the bottom of Fig. 1. The oxide thickness fluctuations introduce surface potential fluctuations similar to the fluctuations introduced by random impurities. DG quantum corrections are included in the simulation. One equiconcentration surface corresponding to electron charge density 1×10^{17} cm^{-3} is plotted in the middle, illustrating the quantum confinement effects in both vertical and lateral directions.

B. Quantum Mechanical Effects

As described in [15], the DG quantum corrections have been carefully calibrated in the direction normal to the channel against rigorous one-dimensional (1-D) full-band Poisson–Schrödinger simulations [13]. Excellent agreement has been achieved both in terms of threshold voltage shift and inversion layer charge distribution. It has been also demonstrated in 2-D examples [14] that DG simulations give a qualitatively correct result in respect to lateral confinement effects associated with the roughness of the Si/SiO_2 interface. However, the rigorous

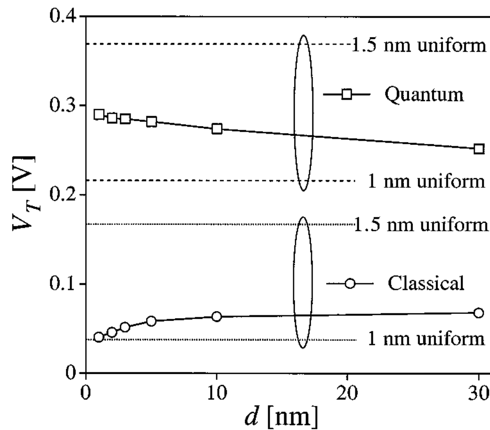

Fig. 2. Threshold voltage of a 30×30 nm^2 MOSFET as a function of the period d of the variations in the oxide thickness at the Si/SiO$_2$ interface. The thick (1.5 nm) and the thin (1 nm) oxide strips are aligned with the direction of the current flow in the channel. Results from classical and DG simulations are compared.

calibration of the DG simulations in respect to quantum confinement in the plane of the channel is still an open issue.

In order to illustrate the importance of quantum confinement when studying OTV effects, simulation experiments were carried out in a 30×30 nm^2 MOSFET with periodical gate oxide structure with alternating thin (1 nm) and thick (1.5 nm) oxide strips in the direction parallel to the current flow in the channel. The dependence of the threshold voltage on the period d of the gate stripes, calculated classically and with DG quantum corrections, is illustrated in Fig. 2. Completely opposite trends are observed in the two sets of simulations. The classical results show reduction in the threshold voltage as d decreases, while the quantum mechanical results show an increase in the threshold voltage.

The explanation of the opposite trends becomes apparent in Fig. 3. The top of the figure illustrates the Si/SiO$_2$ interface followed by two equiconcentration surfaces obtained from classical and DG simulations. The bottom of the figure illustrates the potential distribution. In the classical simulations, there is an increase in the carrier concentration at the corners of the inverted silicon wells due to field crowding there. Such field crowding is responsible, for example, for the inverse narrow channel effect observed in MOSFETs with shallow trench isolation [22]. The increasing numbers of high current density contributions from the corners, when the period of the stripes decreases, results in a reduction of the threshold voltage in the classical case. However, due to 2-D confinement effects, the quantum mechanical charge distribution cannot follow the local increase in the potential in the corners and the maximum in the charge distribution moves to the middle of the wells, resulting in an effective narrowing of the current filaments. This is causing an increase in the threshold voltage when d becomes smaller.

Similar 2-D confinement effects, pushing the maximum of the inversion charge distribution to the middle of the current filaments formed by the random pattern of the interface roughness, are noticeable in the equiconcentration contour shown in Fig. 1. In this case, the height of the interface roughness steps responsible for the lateral confinement is only 0.3 nm.

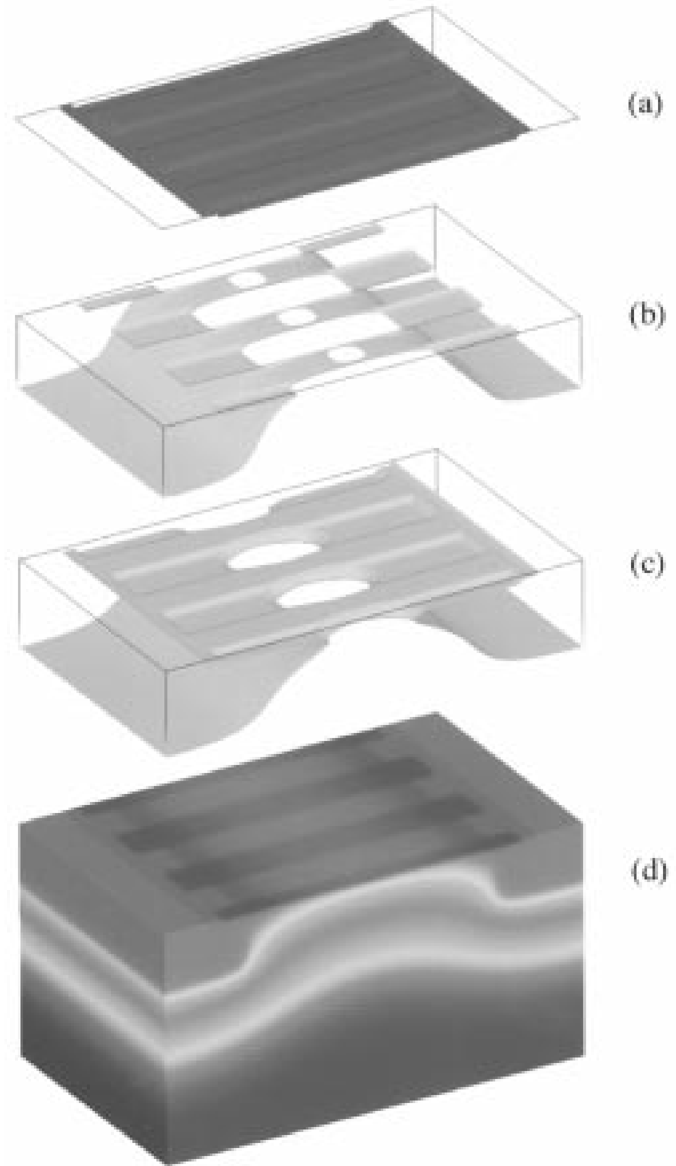

Fig. 3. (a) Profile of the Si/SiO$_2$ interface in a 30×30 nm^2 gate oxide "superlattice" MOSFET, followed by two equiconcentration surfaces obtained from (b) classical and (c) DG simulations, and (d) the potential distribution.

III. Results and Discussion

The generic device simulated in this study is an n-channel 30×30 nm^2 MOSFET with simplified, but well-scaled, architecture. The typical average oxide thickness $\langle t_{\rm ox} \rangle$ is 1.05 nm. The junction depth x_j is 7 nm. The acceptor doping concentration N_A, which is constant in the channel region, is 5×10^{18} cm^{-3}. Continuous doping distribution instead of random discrete dopants is used in most of the simulations. In the simulation experiments, one design parameter is typically varied while the rest remain as specified above. The polysilicon depletion effects are excluded and the gate potential is fixed at the gate/SiO$_2$ interface.

The choice of autocorrelation function and the corresponding power spectrum when generating the random interface is controversial. Early attempts to fit surface roughness limited mobility

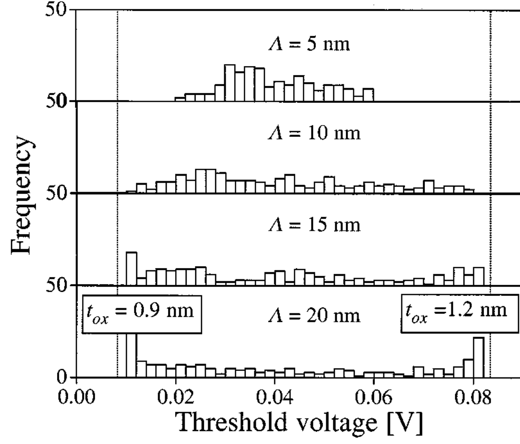

Fig. 4. Threshold voltage variation in a 30×30 nm^2 MOSFET with average oxide thickness $\langle t_{\rm ox}\rangle = 1.05$ nm for different correlation lengths of the Gaussian power spectrum used to generate the Si/SiO_2 interface.

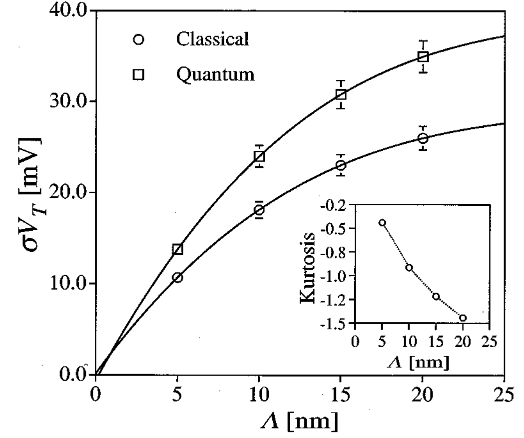

Fig. 5. Dependence of the threshold voltage standard deviation σV_T on the correlation lenght Λ for the 30×30 nm^2 MOSFETs as in Fig. 4. Classical and DG simulation results are compared.

to experimental data were used a Gaussian autocorrelation function [23]. Later, the preference changed to an exponential one [17]. The most recent studies show that both Gaussian and exponential autocorrelation functions can fit the experimental mobility data but need different parameters for electrons and holes [24]. It was also demonstrated in [24] that electron and hole mobility data could be fitted using identical parameters, if a power spectrum, which has a Gaussian shape for small wave vector exchange q but a steeper decay for large q, is used. In this paper, we have adopted a Gaussian power spectrum for generating the random interface. The corresponding 2-D surface is smoother compared to the one generated using an exponential autocorrelation function and less demanding from a grid generation point of view.

A. Correlation Length Dependence

There is a relatively close agreement in the rms values, Δ, of the interface roughness reported by different sources. In the same time there is more than one order of magnitude difference in the reported values for the correlation length Λ. Correlation lengths in the range of 1–3 nm are reported from TEM measurements [17] and are typically used to fit surface roughness limited mobility to experimental data [24]–[26]. At the same time, the values of Λ reported from AFM measurements vary from 10 to 30 nm [18], [26]. Bearing in mind this uncertainty, we first study the impact of Λ on the threshold voltage variation.

The threshold voltage variation in the generic 30×30 nm^2 MOSFET is illustrated in Fig. 4 for different values of Λ. Only roughness at the Si/SiO_2 interface is considered in this case. The sample size in all histograms is 200. The average oxide thickness $\langle t_{\rm ox}\rangle$ is 1.05 nm. The interface roughness is quantized allowing only one step of 0.3 nm, which results in the generation of random oxide regions with thickness 0.9 nm and 1.2 nm, respectively. For small values of Λ, the distribution of the threshold voltage is close to a Gaussian. With the increase of Λ a broadening of the distribution occurs. When Λ becomes comparable with the characteristic dimensions of the MOSFET, two peaks corresponding to the 0.9 nm and 1.2 nm oxide thickness become apparent. It is clear that, for correlation lengths much larger than the characteristics device dimension, there is a high probability that in the whole gate region the oxide will be either 0.9 nm or 1.2 nm thick and most of the devices will have the corresponding uniform oxide threshold voltages. There will be, however, threshold voltages in between associated with MOSFETS in which a boundary between thin and thick oxide regions divides the channel along the direction of the current flow.

The dependence of the threshold voltage standard deviation σV_T on Λ obtained from classical and DG simulations is compared in Fig. 5. The introduction of quantum corrections results in an increase in the threshold voltage variation. We believe that this is related to the lateral confinement effects, which narrow the current percolation paths. In both cases, the dependence of σV_T on Λ is linear for correlation lengths much smaller than the characteristic MOSFET dimensions and saturates for large Λ. The dependence of the kurtosis as a function of Λ in the DG case is shown in the inset of the same figure. The increasingly negative values of the kurtosis are indication for the flattening of the V_T distribution with the increase of the correlation length.

The shape of the σV_T dependence on Λ can be easily understood qualitatively. The binary distribution of the threshold voltage at $\Lambda \gg L_{\rm eff}, W_{\rm eff}$ result in σV_T saturation at a value $\sigma V_T^{\max} \approx (V_T(t_{\rm ox} = 12\ \text{Å}) - V_T(t_{\rm ox} = 9\ \text{Å}))/2$. This gives, for example, $\sigma V_T^{\max} = 49$ mV in the DG case. In the case where $\Lambda \ll L_{\rm eff}, W_{\rm eff}$, we assume as a simplification that gate area $W_{\rm eff} \times L_{\rm eff}$ is divided into uniform $\Lambda/2$-sided squares, each with thin or thick oxide at random. Averaging the contribution of a total of N cells, where $N = 4W_{\rm eff}L_{\rm eff}/\Lambda^2$, the standard deviation of threshold is reduced by a factor of $\sqrt{N}$. Therefore

$$\sigma V_T = \frac{\Lambda \sigma V_T^{\max}}{2\sqrt{W_{\rm eff} L_{\rm eff}}}. \tag{1}$$

Thus, for very small values of Λ, the standard deviation should increase linearly.

Bearing in mind the strong dependence of σV_T on Λ, and the uncertainties in this parameter, we have carried out further investigations for two characteristic correlation lengths. The first

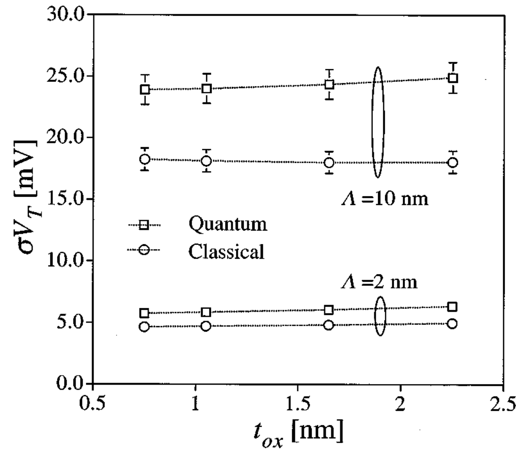

Fig. 6. Dependence of threshold voltage standard deviation σV_T on the average oxide thickness $\langle t_{\rm ox}\rangle$ for a 30×30 nm^2 MOSFET with random Si/SiO_2 interface.

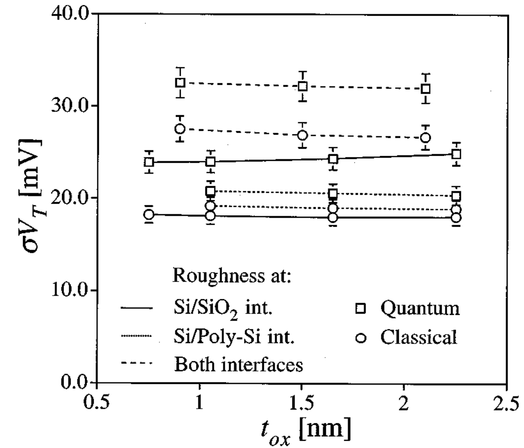

Fig. 8. Dependence of threshold voltage standard deviation σV_T on the average oxide thickness $\langle t_{\rm ox}\rangle$ for a 30×30 nm^2 MOSFET with roughness at the Si/SiO_2 interface, at the gate Si/SiO_2 interface, and at both interfaces $\Lambda = 10$ nm in all cases.

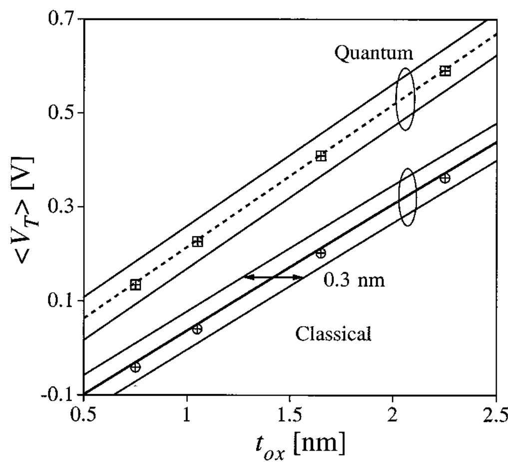

Fig. 7. Dependence of the average threshold voltage $\langle V_T\rangle$ on the average oxide thickness $\langle t_{\rm ox}\rangle$ for a 30×30 nm^2 MOSFET with random Si/SiO_2 interface (symbols) and of the threshold voltage V_T on the oxide thickness $t_{\rm ox}$ for a similar device with uniform oxide (lines).

one, $\Lambda = 2$ nm, is in the middle of the values used to fit mobility data. The second one, $\Lambda = 10$ nm, is at the lower end of correlation lengths extracted from AFM measurements, but for the 30×30 nm^2 MOSFETs gives a distribution which is not strongly peacked at the two bounding values of V_T.

B. Oxide Thickness (In)dependence

The dependence, or more accurately the virtual independence, of σV_T on the average oxide thickness $\langle t_{\rm ox}\rangle$ for a 30×30 nm^2 MOSFET is illustrated in Fig. 6. Again, roughness only at the Si/SiO_2 interface is considered in the simulations. This trend is related to the linear dependence between V_T and $t_{\rm ox}$ known from the textbook expression for the threshold voltage, which results in a constant variance in respect to oxide thickness. We also present in Fig. 7 the dependence of the average threshold voltage $\langle V_T\rangle$ on $\langle t_{\rm ox}\rangle$ calculated classically and quantum mechanically, this time only for $\Lambda =$ 10 nm (symbols). For comparison, the dependence of the threshold voltage V_T of devices with uniform oxide thickness $t_{\rm ox}$ is plotted in the same figure as a function of $t_{\rm ox}$ (lines). It is clear that the average threshold voltage $\langle V_T\rangle$ of the devices with random oxide thickness is very close to the corresponding threshold voltage of uniform oxide MOSFETs with $t_{\rm ox} = \langle t_{\rm ox}\rangle$. The slight lowering of $\langle V_T\rangle$ in the classical case is associated with the increase of the current density at the boundaries between the thinner and thicker oxide regions due to the field crowding effect discussed in Section II.B.

Although very little is known about the properties and the description of the gate/SiO_2 interface, we have designed simulation experiments in an attempt to understand its importance for the threshold voltage variation. The graphs presented in Fig. 8 summarize the results of these experiments in which only one correlation length $\Lambda = 10$ nm is considered. In the first experiment, roughness was introduced at the gate/SiO_2 and the Si/SiO_2 interface was flat. The parameters used to generate the random gate/SiO_2 interface were identical to the parameters used previously to generate the Si/SiO_2 interface. In the classical simulations, the amount of threshold voltage fluctuations introduced by roughness at the top and at the bottom interfaces is the same. In the DG simulations, the roughness at the top interface results in smaller σV_T compared to roughness at the bottom interface. This is consistent with the assumption made in Section III. A that the quantum enhancement in the threshold voltage fluctuations is related to lateral confinement effects. In this case, the lateral confinement is weaker resulting only from potential fluctuations introduced at the smooth Si/SiO_2 interface by the rough gate/SiO_2 interface. In the second simulation experiment, uncorrelated roughness was introduced at both interfaces. The analysis shows that the threshold voltage fluctuations introduced by each of the interfaces are statistically independent, and the total threshold voltage standard deviation in this case closely follows the relationship $\sigma V_T^{\rm tot} = \sqrt{(\sigma V_T^{\rm top})^2 + (\sigma V_T^{\rm bottom})^2}$. To the best of our knowledge, there are no conclusive measurements and agreement in the literature to what extend the roughness at the channel and the gate interfaces are uncorrelated. The question

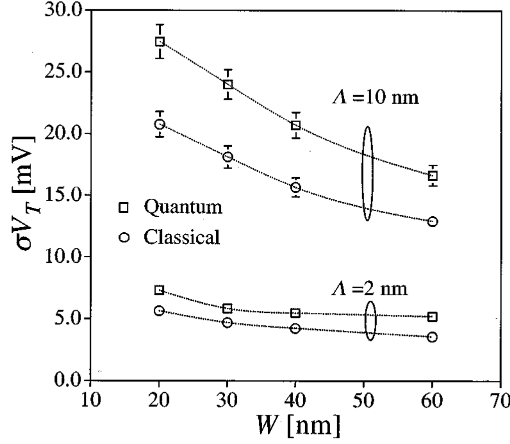

Fig. 9. Dependence of threshold voltage standard deviation σV_T on effective channel width $W_{\rm eff}$ for a 30×30 nm^2 MOSFET with random Si/SiO$_2$ interface.

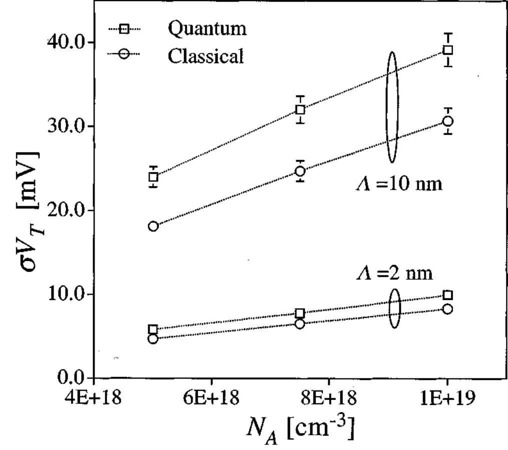

Fig. 11. Dependence of threshold voltage standard deviation σV_T on the channel doping concentration $L_{\rm eff}$ for a 30×30 nm^2 MOSFET with random Si/SiO$_2$ interface.

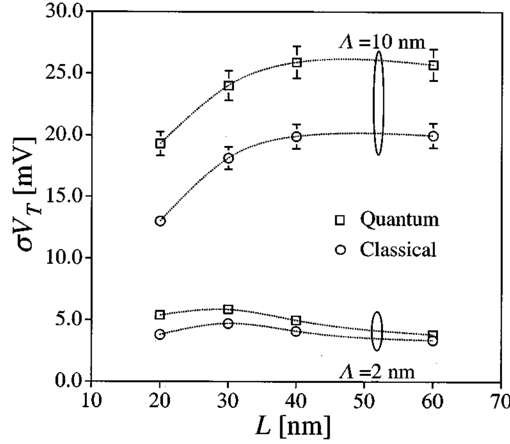

Fig. 10. Dependence of threshold voltage standard deviation σV_T on the effective channel length $L_{\rm eff}$ for a 30×30 nm^2 MOSFET with random Si/SiO$_2$ interface.

"What will happen if the roughness at the both interfaces is due to steps in the original silicon surface and therefore strongly correlated?" will be addressed in a follow-up paper.

C. Geometry Dependence

The dependence of σV_T on the effective channel width $W_{\rm eff}$ and the effective channel length $L_{\rm eff}$ are illustrated in Figs. 9 and 10, respectively. The variation of σV_T in respect to $W_{\rm eff}$ follows closely the expected $1/\sqrt{W_{\rm eff}}$ dependence from (1). The variation of σV_T in respect to $L_{\rm eff}$ follows the $1/\sqrt{L_{\rm eff}}$ dependence only for $\Lambda = 2$ nm and for values of $L_{\rm eff}$ larger than 30 nm. For $L_{\rm eff} < 30$ nm 2-D charge sharing effects significantly reduce the amount of the charge in the channel controlled by the gate and its contribution to the threshold voltage variation, which results in a departure from the $1/\sqrt{L_{\rm eff}}$ dependence. This effect is more pronounced at correlation length $\Lambda = 10$ nm where the departure from the $1/\sqrt{L_{\rm eff}}$ dependence of σV_T occurs at effective channel lengths below 40 nm.

D. Doping Concentration Dependence

Doping concentration N_A higher than 5×10^{18} cm^{-3} will be required to suppress short-channel effects and to adjust the threshold when the conventional MOSFET is scaled to channel lengths below 30 nm. As shown in Fig. 11, the standard deviation of the threshold voltage σV_T in the 30×30 nm^2 MOSFET increases sublinearly with the increase in the doping concentration following a dependence stronger than $\sqrt{N_A}$.

The results from Fig. 11 obtained with DG quantum corrections serve in Fig. 12 as a basis for comparing the standard deviation in the threshold voltage induced by OTV $\sigma V_T^{\rm OTV}$ and the standard deviation in the threshold voltage induced by dopant fluctuations $\sigma V_T^{\rm DF}$. In order to isolate the doping fluctuation (DF) effects, simulations were carried out first using random discrete dopants and uniform gate oxide. The corresponding $\sigma V_T^{\rm DF}$ is approximately two times larger than $\sigma V_T^{\rm OTV}$ for correlation length $\Lambda = 10$ nm, and more than five times larger for $\Lambda = 2$ nm. However, with the increase in the doping concentration, the gap between $\sigma V_T^{\rm DF}$ and $\sigma V_T^{\rm OTV}$ closes up. Referring back to Figs. 5 and 8, it is clear that for correlation lengths larger than 10 nm, taking into acount the roughness at both interfaces, the intrinsic parameter variations associated with OTV and dopant fluctuations become comparable.

Finally, simulations were carried out in which the OTV and the dopant fluctuations are taken into account simultaneously. The close inspection of the results reveals that the two sources of intrinsic parameter fluctuations act in a statistically independent manner resulting in a total standard deviation $\sigma V_T^{\rm tot}$ which closely follows the relationship $\sigma V_T^{\rm tot} = \sqrt{(\sigma V_T^{\rm OTV})^2 + (\sigma V_T^{\rm DF})^2}$.

IV. Conclusion

The interface roughness related oxide thickness fluctuations will introduce significant intrinsic fluctuation in the threshold voltage when the correlation length of the interface becomes comparable to the characteristic dimensions of aggressively

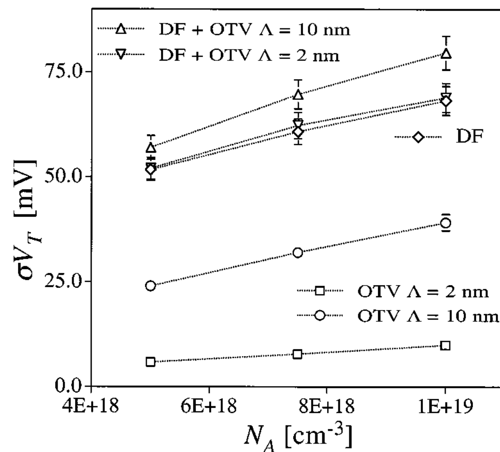

Fig. 12. Comparison of the standard deviation of the threshold voltage introduced by oxide thickness variation (OTV) and by doping fluctuations (DFs).

scaled MOSFETs near the end of the International Roadmap for Semiconductors. The introduction of quantum corrections in the simulations results in further increase of the fluctuations. In the oxide thickness range of 1–3 nm, the intrinsic threshold voltage fluctuations are practically independent of the oxide thickness. The fluctuations introduced by uncorrelated Si/SiO_2 and the gate/SiO_2 interfaces are statistically independent. A departure from the expected $1/\sqrt{\mathrm{Area}}$ dependence of the threshold voltage standard deviation is observed when the short-channel effects start to play a significant role. The doping concentration dependence of the threshold voltage standard deviation is sublinear but stronger than $\sqrt{N_A}$. For devices with characteristic dimensions below 30 nm, the oxide thickness induced threshold voltage fluctuations become comparable to the fluctuations induced by random discrete dopants, particularly when the contribution of both interfaces is taken into account and the larger correlation length suggested by AFM measurements are adopted.

Acknowledgment

The authors are grateful to A. R. Brown for a critical reading of the manuscript.

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Asen Asenov (M'96) received the M.Sc. degree in solid state physics from Sofia University, Sofia, Bulgaria, in 1979, and the Ph.D. degree in physics from The Bulgarian Academy of Science, Sofia, in 1989.

For ten years, he was Head of the Process and Device Modeling Group in IME, Sofia, developing one of the first integrated process and device CMOS simulators IMPEDANCE. From 1989 to 1991, he was a Visiting Professor at the Physics Department of the Technical University of Munich, Munich, Germany. He is currently Head of Department of Electronics and Electrical Engineering at the University of Glasgow, Glasgow, U.K. As a Leader of the Device Modeling Group and Academic Director of the Atomistic Device Simulation Center, he also coordinates the development of 2-D and 3-D device simulators and their application in the design of FETs, SiGe MOSFETs, and IGBTs. He has over 180 publications in process and device modeling and simulation, semiconductor device physics, "atomistic" effects in ultrasmall devices, and parallel computing.

Savas Kaya received the M.Phil. degree in 1994 from the University of Cambridge, Cambridge, U.K., and the Ph.D. degree in 1998 from Imperial College of Science, Technology & Medicine, London, U.K., for his work on strained Si quantum wells on vicinal substrates.

From 1998 to 2001, he was a Postdoctoral Researcher at the University of Glasgow, Glasgow, U.K., carrying out research in transport and scaling in Si/SiGe MOSFETs, and fluctuation phenomena in decanano MOSFETs. He is currently with the Russ College of Engineering, Ohio University, Athens. His other interests include TCAD, transport theory, nanostructures, and process integration.

John H. Davies received the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1982 for theoretical work on the electronic properties of amorphous semiconductors.

He was a Research Fellow at Cornell University, Ithaca, NY, before coming to Glasgow University, Glasgow, U.K., in 1986. He has since spent two periods of leave at The Ohio State University, Columbus, and the University of California at Santa Barbara. Most of his research is centered on the physics of transport in III–V heterostructures, which has included the modeling of surfaces and gates, including the effect of stress from patterned surfaces and gates. He has been interested in the effect of discrete, random donors for many years, and previous research showed their destructive effect on quantum transport in ballistic devices at low temperature. Other interests include the theory of resonant tunnelling, conduction in lateral superlattices, and the calculation of magnetic fields in permanent-magnet motors.