

Contents

1	Introduction	1
	References	5
 Part I Background		
2	Semiconductor Device Physics for TFTs	9
2.1	Introduction	9
2.2	Semiconductor Surface Physics	10
2.2.1	Ideal MIS Capacitor and Surface Band Bending	10
2.2.2	Gate Bias and Threshold Voltage	17
2.2.3	Real MIS Structures	17
2.2.3.1	Work Function Differences	18
2.2.3.2	Oxide Charges and Interface States	20
2.2.4	Evaluation of Surface Potential	25
2.3	Electron-Hole Pair Generation and Recombination	28
2.3.1	Thermal Equilibrium	29
2.3.2	Non-equilibrium, Steady State	31
2.3.3	Generation Currents	33
2.3.4	Recombination Processes	35
2.3.4.1	Low-Level Injection	36
2.3.4.2	High-Level Injection	37
2.4	Current Flow Equations	38
2.5	Summary	41
Appendix: Summary of Key Equations		42
A.1	Semiconductor Surface Band Bending	42
A.2	Carrier Recombination and Generation	43
	References	44

3 Insulated Gate Field Effect Transistors, IGFETs	45
3.1 Introduction	45
3.2 MOSFET Operation	46
3.3 Current-Voltage Equations.	49
3.3.1 Simplified Format.	49
3.3.1.1 Linear Regime	52
3.3.1.2 Saturation Regime	53
3.3.2 Full MOSFET Equation	54
3.3.2.1 Linear Regime	54
3.3.2.2 Saturation Regime	55
3.3.3 Non-ideal MOSFET Behaviour	57
3.4 Sub-Threshold Currents.	59
3.5 Thin Film Considerations	62
3.5.1 Threshold Voltage	63
3.5.2 Saturation Voltage, $V_{D(\text{sat})}$	64
3.6 Summary.	65
Appendix: Summary of Key Equations.	66
A.1 Simplified MOSFET On-State Analysis.	66
A.2 Simplified MOSFET Sub-Threshold Analysis	67
References	67
4 Active Matrix Flat Panel Displays.	69
4.1 Introduction	69
4.2 Liquid Crystal Cells	71
4.2.1 LC Material.	71
4.2.2 Twisted Nematic LC Cell Structure	73
4.3 Active Matrix Addressing	76
4.4 Pixel Layout Considerations.	83
4.4.1 General	83
4.4.2 Performance Artefacts.	85
4.4.2.1 Voltage Kick-Back	85
4.4.2.2 Vertical Cross-Talk	87
4.4.2.3 Row Resistance Effects	87
4.5 AMLCD Fabrication.	90
4.5.1 TFT Plate	90
4.5.2 Colour Filter, CF, Plate.	91
4.5.3 LC Cell.	92
4.5.4 Display Module	92
4.6 Other Display Technologies.	93
4.6.1 Active Matrix Electrophoretic Displays.	93
4.6.2 Active Matrix Organic Light Emitting Diode Displays	96
4.6.2.1 OLED Operation	96
4.6.2.2 AMOLED Pixels.	99

4.7 Summary	102
References	103

Part II TFTs

5 Hydrogenated Amorphous Silicon TFT Technology and Architecture	109
5.1 Introduction	109
5.2 a-Si:H Material	110
5.3 a-Si:H TFT Architecture	113
5.3.1 Back-Channel-Etched TFT Fabrication	114
5.3.2 Etch-Stop TFT Fabrication	115
5.4 TFT Layout Considerations	117
5.4.1 Photolithography Process	117
5.4.2 TFT Layout Issues	118
5.5 Plasma Enhanced Chemical Vapour Deposition, PECVD	119
5.5.1 Undoped a-Si:H	121
5.5.2 Doped a-Si:H	127
5.5.3 a-SiN _x :H Gate Insulator	130
5.6 Novel a-Si:H TFTs	131
5.6.1 Self-Aligned TFTs	131
5.6.2 Short Channel TFTs	133
5.6.3 Hydrogen-Diluted TFT Depositions	135
5.7 Summary	137
References	137
6 Hydrogenated Amorphous Silicon TFT Performance	141
6.1 Introduction	141
6.2 Defect Structure and a-Si:H Density of States	142
6.2.1 Basic Material Properties	142
6.2.2 a-Si:H Density of States, DOS	149
6.2.3 Band Bending and Surface Space Charge	150
6.2.4 Field Effect Mobility	155
6.2.5 Equilibration in Thin Films	158
6.2.5.1 Gate Dielectric	160
6.2.5.2 n- and p-channel TFTs	162
6.3 TFT Characteristics	163
6.3.1 On-State	163
6.3.2 Off-State	167
6.4 Bias-Stress Instability	169
6.4.1 Gate Bias	169
6.4.2 Pulsed Bias Stress	174
6.4.3 Gate and Drain Bias Stress Effects	176

6.5	Other Meta-Stability Effects	178
6.5.1	Staebler Wronski Effect	178
6.6	Summary	181
	References	182
7	Poly-Si TFT Technology and Architecture	185
7.1	Introduction	185
7.2	Poly-Si Preparation	187
7.2.1	Background	187
7.2.2	Excimer Laser Crystallisation	190
7.2.2.1	Introduction	190
7.2.2.2	Crystallisation Process	190
7.2.2.3	TFT Crystallisation	196
7.2.2.4	ELA Process Control Issues	200
7.2.3	Other Laser Techniques	203
7.2.4	Metal Induced Crystallisation	204
7.2.4.1	Ni Mediated Crystallisation of a-Si	204
7.2.4.2	SMC Poly-Si TFTs	208
7.3	Gate Dielectrics	212
7.3.1	Silicon Dioxide	212
7.3.2	Alternative Dielectrics	217
7.4	Poly-Si TFT Architecture and Fabrication	218
7.4.1	Architecture	218
7.4.1.1	Self Aligned Source and Drain Doping	219
7.4.1.2	Drain Field Relief	222
7.4.1.3	Other TFT Architectures	224
7.4.2	Fabrication Process	224
7.5	Advanced Processing	227
7.5.1	Large Grain Poly-Si	227
7.5.2	Modified Excimer Laser Crystallisation	227
7.5.2.1	Sequential Lateral Solidification	230
7.5.3	Green Laser Crystallisation	234
7.5.3.1	Pulsed Nd:YAG Lasers	234
7.5.3.2	CW Nd:YVO ₄ Lasers	237
7.5.4	Comparison of Large Grain Crystallisation Systems	240
7.6	Poly-Si Applications	242
7.7	Summary	244
	References	246
8	Poly-Si TFT Performance	253
8.1	Introduction	253
8.2	Electrical Conduction in Poly-Si	254
8.2.1	Analytical Bulk Conduction Model	254

8.2.2	Analytical Model of TFT Conduction	260
8.2.3	Limitations of Analytical Model	261
8.3	Poly-Si Density of States, DOS	262
8.4	TFT Off-State Currents	266
8.5	Performance Artefacts and Drain Field	272
8.5.1	Electrostatic Drain Field, F	273
8.5.2	Hot Carrier Damage and LDD	274
8.5.3	Field-Enhanced Leakage Currents	280
8.6	Other Bias-Stress Instabilities	282
8.6.1	Gate Bias Stress	283
8.6.1.1	Ionic Instability	283
8.6.1.2	Negative Bias-Temperature Instability	283
8.6.2	Combined Gate and Drain Bias Stress	285
8.7	Short Channel Effects	288
8.7.1	Parasitic Resistance Effects	290
8.7.2	Floating Body Effects	292
8.7.2.1	Kink Effect	292
8.7.2.2	Sub-Threshold and Threshold Voltage Effects	294
8.8	Summary	296
	References	297
9	Transparent Amorphous Oxide Semiconductor TFTs	301
9.1	Introduction	301
9.2	Material Properties	302
9.3	TFT Architecture and Fabrication	305
9.3.1	Architecture	306
9.3.2	Fabrication Processes	308
9.3.2.1	a-IGZO Layer	308
9.3.2.2	Gate Dielectric	308
9.3.2.3	Post Deposition Annealing	310
9.3.2.4	Metallisation	311
9.3.2.5	Process Flow	311
9.4	a-IGZO TFT Performance	312
9.4.1	n-Channel Characteristics	312
9.4.2	Conduction Process and Density of States Distribution, DOS	318
9.4.2.1	Conduction Process	318
9.4.2.2	Density of States Distribution, DOS	320
9.4.3	Bias Stress Instability	325
9.4.3.1	Gate Bias Instability	326
9.4.3.2	Negative Bias Illumination Stress (NBIS)	328
9.4.3.3	Stability Considerations for Active Matrix Addressing TFTs	330

9.5	AOS TFT Circuits	332
9.6	Summary	333
	References	334
10	Organic TFTs	339
10.1	Introduction	339
10.2	Background and Materials	342
10.2.1	Conjugated Molecular Systems.	342
10.2.2	Molecular Bonding	344
10.2.3	Molecular Organisation	344
10.2.4	Metal/Organic Contacts	347
10.2.5	Carrier Transport	350
10.3	OTFT Architecture	351
10.4	Materials and Fabrication Processes	354
10.4.1	Solution Processing Techniques	355
10.4.1.1	Spin-coating	355
10.4.1.2	Drop-casting	355
10.4.1.3	Zone-casting	356
10.4.1.4	Printing	357
10.4.2	Organic Semiconductor Layers for p-Channel TFTs	358
10.4.2.1	Vacuum Thermal Evaporation.	358
10.4.2.2	Solution Processing	360
10.4.3	Organic Semiconductor Layers for n-Channel TFTs	363
10.4.4	Gate Dielectric	368
10.4.4.1	Inorganic Dielectrics	369
10.4.4.2	Organic Dielectrics	370
10.4.4.3	Self-Assembled Monolayers	373
10.4.5	Metals	373
10.4.6	Process Flow	374
10.4.7	Novel Processing	376
10.5	OTFT Characteristics	378
10.5.1	General	378
10.5.2	Contact Effects.	381
10.5.3	Contact Architecture	386
10.6	Instability Effects	389
10.6.1	Air-Instability.	389
10.6.2	Gate Bias Stress Instability	390
10.7	Summary	395
	References	396

Part III Novel Substrates and Devices

11 TFTs on Flexible Substrates	407
11.1 Introduction	407
11.2 Substrate Handling	409
11.3 Substrate Bending	413
11.4 a-Si:H TFTs on Flexible Substrates	416
11.4.1 a-Si:H Fabrication Processes	416
11.4.1.1 Direct Processing on Plastic	417
11.4.1.2 Steel Foil Substrates	422
11.4.1.3 Carrier Plate Technology	423
11.4.1.4 Roll-to-Roll (R2R) Processing	426
11.4.2 Uniaxial Strain Effects on a-SiH TFTs	428
11.5 Poly-Si TFTs on Flexible Substrates	430
11.5.1 Fabrication Processes	430
11.5.1.1 Direct Fabrication on Plastic Substrates	431
11.5.1.2 Fabrication on Steel Foils	433
11.5.1.3 Transfer Processes	435
11.5.2 Uniaxial Strain Effects on Poly-Si TFTs	438
11.6 Organic TFTs on Flexible Substrates	440
11.6.1 Fabrication Processes	441
11.6.1.1 Direct Processing	441
11.6.1.2 Carrier Plate Processing	442
11.6.2 Uniaxial Strain Effects on Organic TFTs	442
11.7 Plastic Substrate Issues	444
11.8 Summary	446
References	447
12 Source-Gated Transistors	453
12.1 Introduction	453
12.2 Schottky Barrier Diodes	455
12.3 SGT Structure and Operation	459
12.3.1 Background	459
12.3.2 SGT1 Mode	460
12.3.3 SGT2 Mode	467
12.4 Fabrication Process	468
12.5 Comparison of SGT and FET Characteristics	470
12.6 Gate/Source-Barrier Interactions in OTFTs	473
12.7 Summary	478
References	479
Index	481