

Inverted Sine Carrier for Fundamental Fortification in PWM Inverters and FPGA Based Implementations

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Abstract: This paper deals with a novel natural sampled pulse width modulation (PWM) switching strategy for voltage source inverter through carrier modification. The proposed inverted sine carrier PWM (ISCPWM) method, which uses the conventional sinusoidal reference signal and an inverted sine carrier, has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping. The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges while keeping the total harmonic distortion (THD) lower without involving changes in device switching losses. The presented mathematical preliminaries for both SPWM and ISCPWM give a conceptual understanding and a comparison of the strategies. The detailed comparison of the harmonic content and fundamental component of the ISCPWM output for different values of modulation index with the results obtained for the SPWM is also presented. Finally, the proposed modulator has been implemented in field programmable gate array (FPGA- Xilinx Spartan 3) and tested with the proto-type inverter.

Keywords: Carrier modification, Inverted sine carrier pulse width modulation (ISCPWM), PWM inverter, THD.

1 Introduction

The harmonic content in the output of the inverter can be reduced by employing pulse-width modulation (PWM). The PWM techniques and strategies have been the subject of intensive research since 1970's were to fabricate a sinusoidal ac output voltage. Sinusoidal PWM (SPWM) is effective in reducing lower order harmonics while varying the output voltage and gone through many revisions and it has a history of three decades [1-5]. The SPWM technique, however, exhibits poor performance with regard to maximum attainable voltage and power. The fundamental amplitude in the SPWM output waveform is smaller than for the rectangular waveform. In three-phase case the ratio of the fundamental component of the utmost line-to-line voltage to the direct supply voltage is 0.866% and this value indicates poor exploitation of the dc supply.

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The reduced circuit complexity delta modulation suitable for half-bridge inverter was reported for smooth transition between the PWM and single pulse mode (V/f control) in 1981 [3]. The third harmonic injection PWM (THIPWM) method suitable for three-phase inverters was proposed in which a modulating wave is obtained by adding the third harmonic component to fundamental sine in right proportion while the carrier is conventional triangular [6]. The triplen harmonic injection PWM (TRIPWM) is a variation of the THIPWM, in which the modulation function is obtained by adding the harmonic components of integer multiples of three to the fundamental sine [7]. In the above mentioned harmonic injection PWM methods, it is possible to increase the fundamental about 15% and hence better utilization the dc power supply. Usage of staircase as modulating function with high frequency triangular carrier for three-phase application had demonstrated nearly 10% fundamental improvement in the work reported in 1988 [8]. A modified carrier PWM methods was proposed in which any two adjacent cycles of carrier triangular wave are grouped as either “W” shape or “M” shape and then suitably “W” and “M” cycle group conversions are made [9]. This type of carrier requires a digital platform for its implementation and gives about 4% and 19% improvements in fundamental component while working alone and amalgamated with THIPWM reference respectively. All the previous attempts to achieve the same objectives are either regular sampled or mode-changing methods. However, in regular sampled PWM (digitally based controller), the generation of harmonics is dominated by quantization effects even with frequency ratios as low as 8:1 [10] and hence they fail to emulate the properties of (natural) carrier and reference functions. The natural sampled solutions viz. THIPWM rely on mode changing.

The purpose of this paper is to propose a natural sampled single mode solution to fundamental restriction and distortion through the modification of carrier function. The proposed inverted sine carrier PWM (ISCPWM) control scheme for single-phase full-bridge inverter, which eliminates some of the limitations of the conventional SPWM viz. poor spectral quality of the output voltage, poor performance with regard to maximum output voltage possible etc. This paper also presents the theory and mathematical preliminaries of the novel scheme along with the SPWM in addition to computer simulation.

2 PWM Strategy

A Sinusoidal Pulse Width Modulation

The basic single-phase full-bridge PWM inverter is shown in Fig. 1 in which S_1 and S_2 will be given PWM pulses for first (positive) output half cycle and S_3 and S_4 are gated for the next (negative) half cycle. The unipolar PWM pulse generation with resulting pattern is represented in Fig. 2 in which a

triangular carrier wave is compared with sinusoidal reference waveform to generate PWM gating pulses. All PWM waveforms presented in this paper are assumed to be synchronous Unipolar PWM voltage switching.

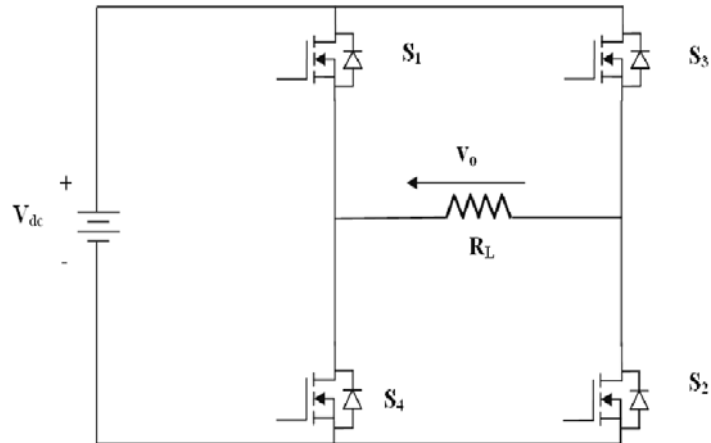


Fig. 1 – Basic single-phase inverter.

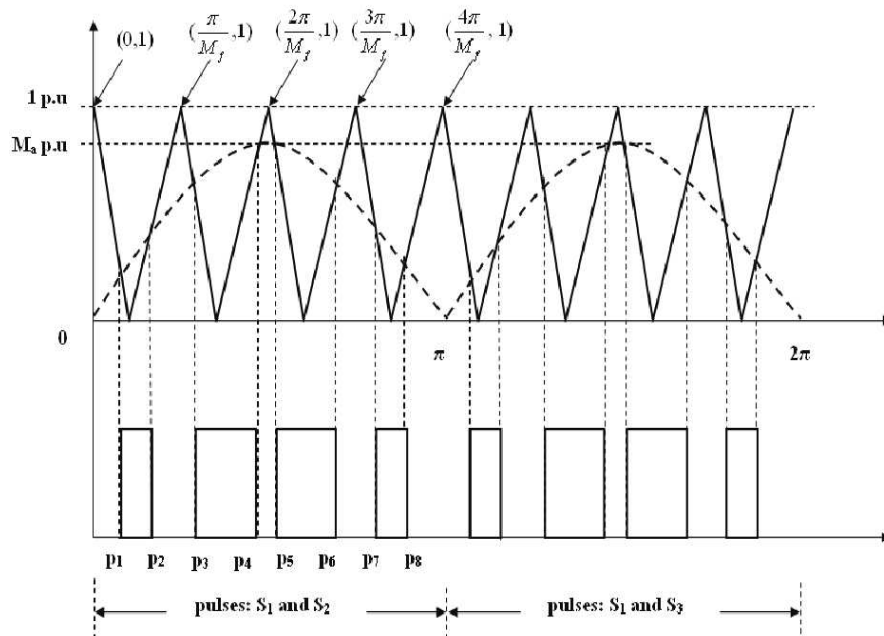


Fig. 2 – SPWM pulse generation and pattern.

B Mathematical Analysis

The harmonics present in the quasi-square wave and their relative amplitudes always remain the same. With PWM, however, the relative amplitudes of the harmonics change with the modulation index. The use of SPWM in inverters, for all its technical benefits, renders most complex calculations relating to inverter behavior. It is generally accepted that the performance of an inverter with any switching strategy can be related to the harmonic content of its output voltage [11].

A precise value of the switching angle and hence duty cycle can be obtained through the triangular (carrier) and the sinusoidal (reference) equations. The modulation pattern of the SPWM control (Fig. 2) indicates the switching angles/meeting points ($p_1, p_2, p_3 \dots p_i$). The PWM control signal is obtained by comparing a high frequency triangular carrier of frequency f_c and amplitude 1 (per unit) and a low frequency sine wave of frequency f_m and amplitude M_a (per unit). Equations for sinusoidal reference and triangular carrier are given by (1) and (2) respectively.

$$y = M_a \sin x, \quad (1)$$

$$x \pm \left(\frac{\pi}{2M_f} \right), \quad y = \frac{r\pi}{2M_f}, \quad (2)$$

where:

M_a - modulation index;

M_f - frequency ratio;

$r-1$ for first pair of triangular sections (straight lines), 3 for second pair, 5 for third pair and so on;

‘+’ - sign should be taken for odd number of line sections and

‘-’ - sign for should be taken for even number of line sections.

The equations describing the natural sampled switching angles are transcendental and have the general distinct solutions for odd and even meeting points. The condition for switching angles is given in (3) and (4) respectively for odd and even switching angles.

$$M_a \sin p_i + \frac{2M_f p_i}{\pi} = i, \quad i = 1, 3, 5, \dots, \quad (3)$$

$$M_a \sin p_i - \frac{2M_f p_i}{\pi} = 1 - i, \quad i = 2, 4, 6, \dots, \quad (4)$$

where i is number of points and p_i is i -th switching angle.

The pattern represented in Fig. 2 does have eight switching angles and four PWM pulses. The duty cycle can be calculated by simply adding the width of the individual pulses. The width of any pulse can be found from subtracting one odd meeting point from immediate even successor. Since the inverter output irrespective of control methods exhibits equal positive and negative half cycles, which results in zero dc component ($a_0 = 0$), and also does not possess any even harmonics due to half wave symmetry.

Equation (5) gives the generalized Fourier coefficients for the problem considered. In the equation p'_i represents switching angles corresponds to negative half cycle.

$$\begin{aligned}
 a_n &= \frac{V_{dc}}{n\pi\sqrt{2}} \sum_{k=1}^{i-1} \{(\sin np_{k+1} - \sin np_k) - (\sin np'_{k+1} - \sin np'_k)\}, \\
 b_n &= \frac{V_{dc}}{n\pi\sqrt{2}} \sum_{k=1}^{i-1} \{(\cos np_{k+1} - \cos np_k) - (\cos np'_{k+1} - \cos np'_k)\}, \\
 c_n &= \sqrt{a_n^2 + b_n^2}.
 \end{aligned} \tag{5}$$

3 Proposed ISCPWM

The control strategy uses the same reference (synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater pulse area. The difference in pulse widths (hence area) resulting from triangle wave and inverted sine wave with the low (output) frequency reference sine wave in different sections can be easily understood. In the gating pulse generation of the proposed ISCPWM scheme shown in Fig. 3, the triangular carrier waveform of SPWM is replaced by an inverter sine waveform.

For the ISCPWM pulse pattern, the switching angles may be computed as the same way as SPWM scheme. The equations of inverted sine wave is given by (6) and (7) for its odd and even cycles respectively.

The intersections ($q_1, q_2, q_3 \dots q_i$) between the inverted sine voltage waveform of amplitude 1 p.u and frequency f_c and the sinusoidal reference waveform of amplitude M_a p.u and frequency f_0 can be obtained by substituting (1) in both (6) and (7). The switching angles for ISCPWM scheme can be obtained from (8) and (9).

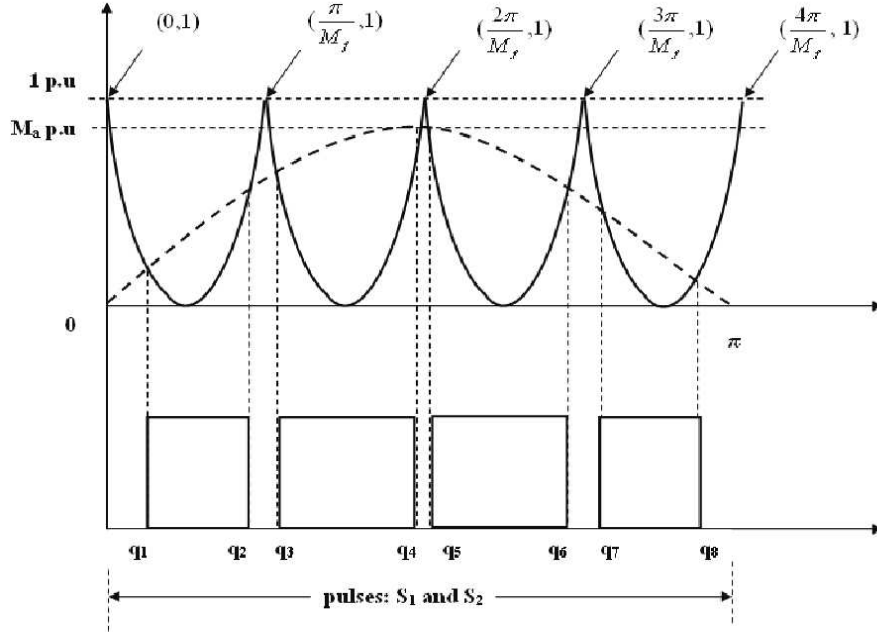


Fig. 3 – Inverter sine carrier PWM pulse pattern.

$$y = 1 - \sin\left(M_f x - \frac{\pi}{2}(i-1)\right) \quad (6)$$

$$y = 1 - \sin\left(M_f x - \frac{\pi}{2}(i-2)\right) \quad (7)$$

$$M_a \sin q_i + \sin\left(M_f q_i - \frac{\pi}{2}(i-1)\right) = 1, \quad i = 1, 3, 5, \dots \quad (8)$$

$$M_a \sin q_i + \sin\left(M_f q_i - \frac{\pi}{2}(i-2)\right) = 1, \quad i = 2, 4, 6, \dots \quad (9)$$

It is worth while to note that both in SPWM (considered) and ISCPWM schemes, the number of pulses will be equal to M_f and hence the constant switching loss is guaranteed. To have conceptual understanding of wider pulse area and hence the dexterous input dc utilization in the ISCPWM, location of switching angles, duty cycle and their dependence on M_a and M_f are discussed. Fig. 4 depicts the influence of M_a on different switching angles (four angles considered in both cases) at constant M_f of 6. From this figure, it is observed that the odd switching instants vary with negative slope and even

switching instants have positive slope. Variation of all the switching instants against M_a is a straight line and slope of each one is more than its previous one. All the odd switching angles of ISCPWM method happen earlier than similar angles of PWM method, while the situation is reverse in case of even switching angles and hence higher pulse area.

Fig. 5 gives the position of first switching angle, p_1/q_1 for various M_f at two M_a values 0.4 and 0.8. Influence of M_f over the switching angles for M_f value above 20 is negligible while for the range below 20 it largely depends on M_f . Both SPWM and ISCPWM upshots nonlinear relationship in the lower M_f range. Fig. 6 shows the variation of duty cycle for different M_a with constant M_f . The figure demonstrates that duty cycle is higher for ISCPWM throughout the entire range of M_a and the austere linear relationship of duty cycle in SPWM is violated in ISCPWM for lower values of M_a . In addition, in ISCPWM causes M_f dependency of duty. The ISCPWM gives higher duty cycle without any pulse dropping at given modulation index while makes the dependency a little non-linear. Fig. 7 shows that the dependence of duty cycle on M_f at any M_a value is a constant for even the lowest typical carrier frequency of application.

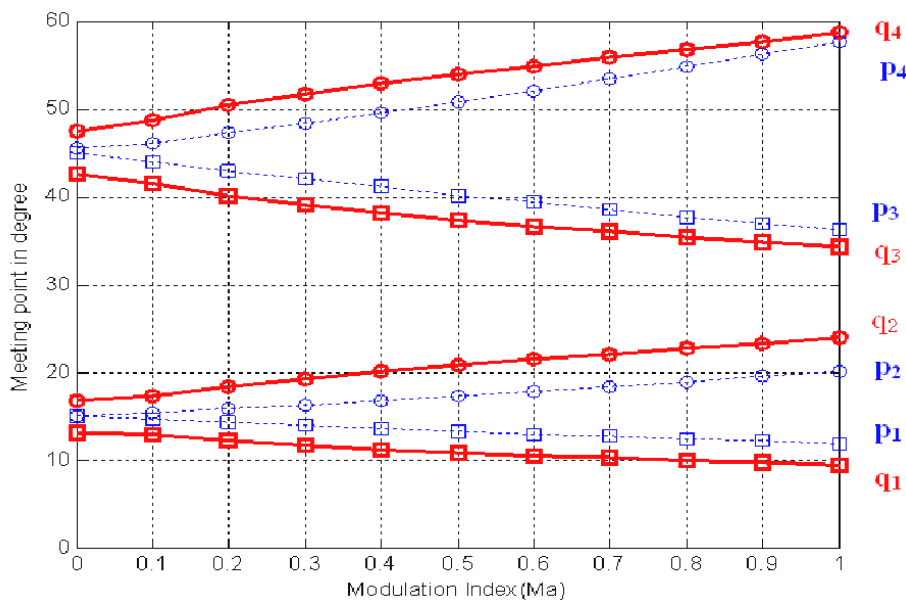


Fig. 4 – Influence of modulation index on switching angles.

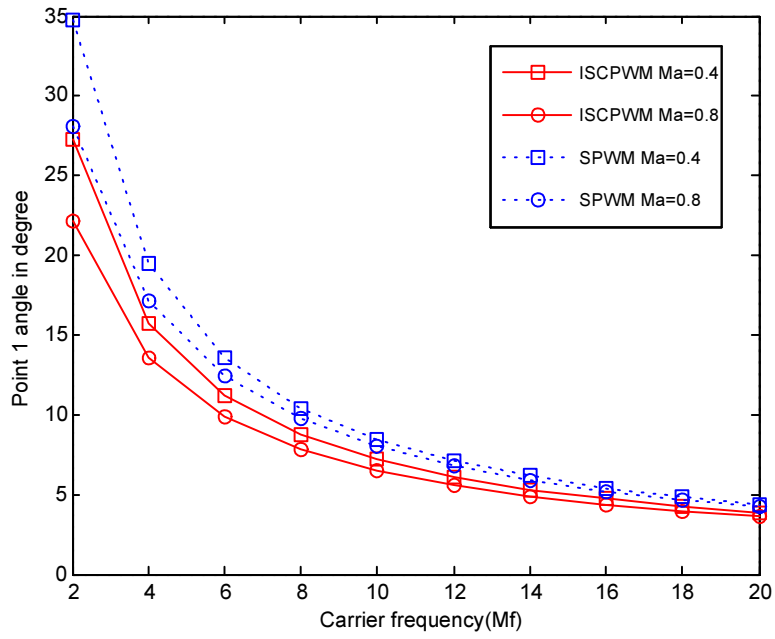


Fig. 5 – Influence of carrier frequency on switching instant.

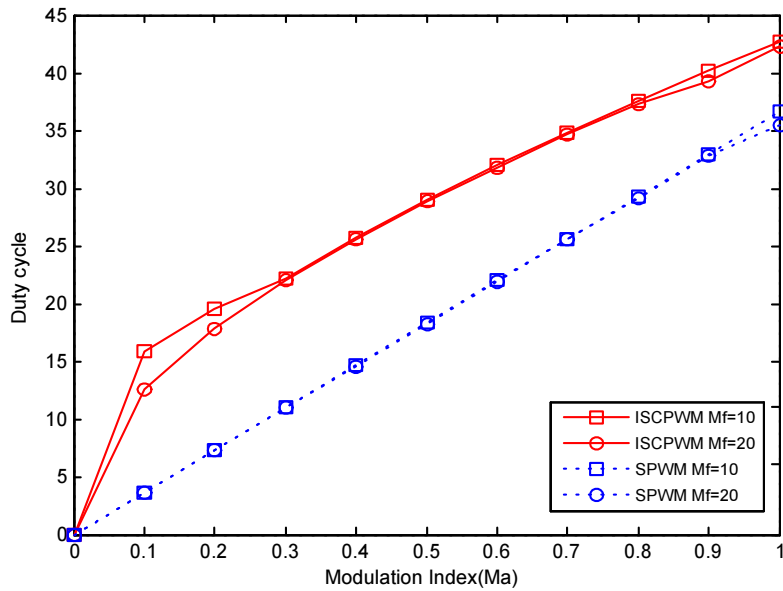


Fig. 6 – Modulation index vs duty cycle.

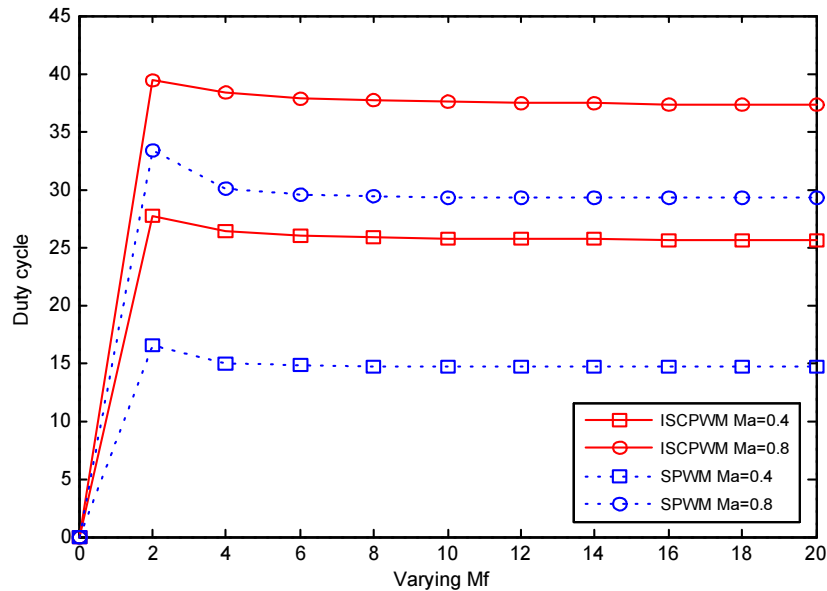
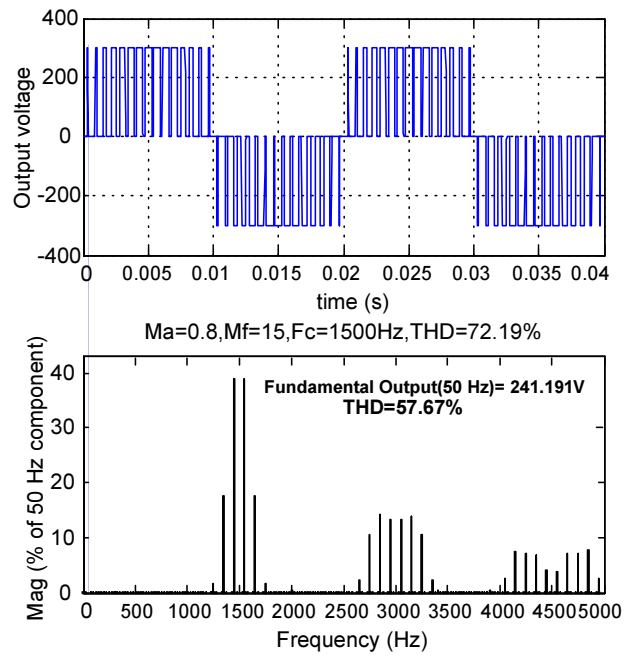


Fig. 7 – Frequency ratio vs duty cycle.

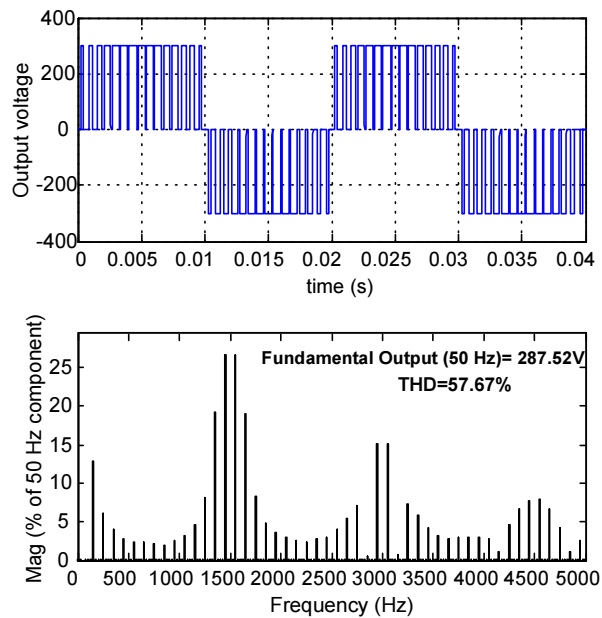
4 Simulation Results

To show the effectiveness of the proposed modulator simulation was performed for different modulation index and carrier frequency values.

The ISCPWM scheme achieves fundamental voltage values of range which can only be obtained by over modulation, if a conventional SPWM scheme is adopted. Fig. 8 shows the output voltage waveforms and harmonic spectrums of SPWM and ISCPWM while **Table 1** and **Table 2** compares the both methods for fundamental (h_1), lower order harmonics (h_2 - h_9), side band harmonics ($2M_f \pm 1$, $2M_f \pm 3$, etc) and THD for $M_a = 0.8$, $M_f = 15$ and $V_{dc} = 300V$. The improved fundamental and reduced THD are evident from the figure, which gives 19.21% fundamental fortification than SPWM. At $M_a = 1$ (verge on linearity), ISCPWM gives 9% higher fundamental than SPWM, while the fortification obtained from the harmonic injection methods with pulse dropping and mode changing is 15%. The additional advantage in the ISCPWM is, it does not require any mode changing like THIWPM. Regrettably, the ISCPWM causes marginal increase in the lower order harmonics, but except third harmonics all other harmonics are in acceptable level (less than 5%). It is worth noting that for three-phase applications, the heightened third harmonics need not be bothered.



(a) SPWM



(b) ISCPWM

Fig. 8 – Output voltage waveforms and their harmonic spectrum.

Table 1

Comparison of THD, fundamental and lower order harmonics.

Method	THD (%)	h_1 (V)	h_3 (V)	h_5 (V)	h_7 (V)	h_9 (V)
SPWM	68.02	241.2	0.42	0.28	0.07	0.31
ISCPWM	57.67	287.5	36.75	17.58	11.35	8.21

Table 2

Comparison of higher order harmonics.

Method	$2M_f - 3$ h_{27} (V)	$2M_f - 1$ h_{29} (V)	$2M_f + 1$ h_{31} (V)	$2M_f + 3$ h_{33} (V)
SPWM	42.34	93.72	93.72	42.33
ISCPWM	55.01	76.43	76.84	54.84
Method	$4M_f - 3$ h_{57} (V)	$4M_f - 1$ h_{59} (V)	$4M_f + 1$ h_{61} (V)	$4M_f + 3$ h_{63} (V)
SPWM	34.14	31.78	31.98	33.54
ISCPWM	1.32	43.69	43.72	2.16

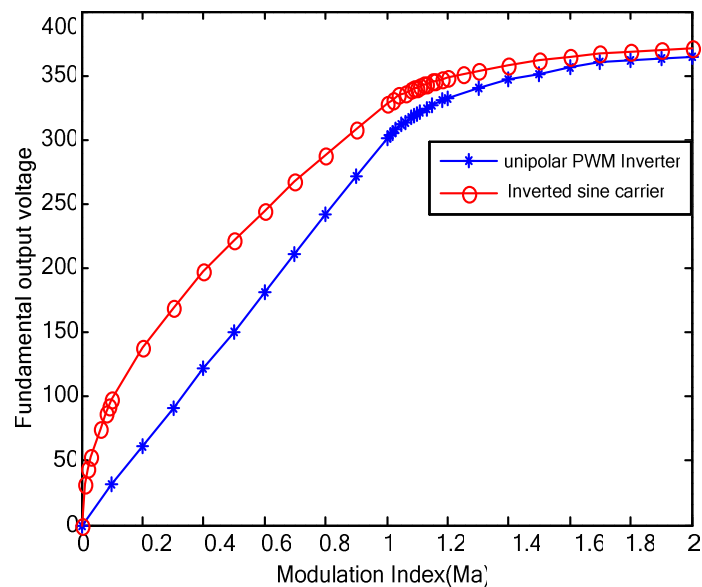


Fig. 9 – *Variation of fundamental with modulation index.*

Fig. 9 shows the complete fundamental component working range as function of M_a while the Fig. 10 presents the corresponding THD values. The

ISCPWM method gives higher fundamental throughout the inverter working range. Its performance is more appreciable in lower modulation index ranges. For instance, at $M_a = 0.1$, ISCPWM gives fundamental component value three times of SPWM at the same time the THD value 40% less. Fig. 11 shows the variation of fundamental component with the THD. Hence, the ISCPWM scheme is more favorable than the SPWM technique for use in the inverter.

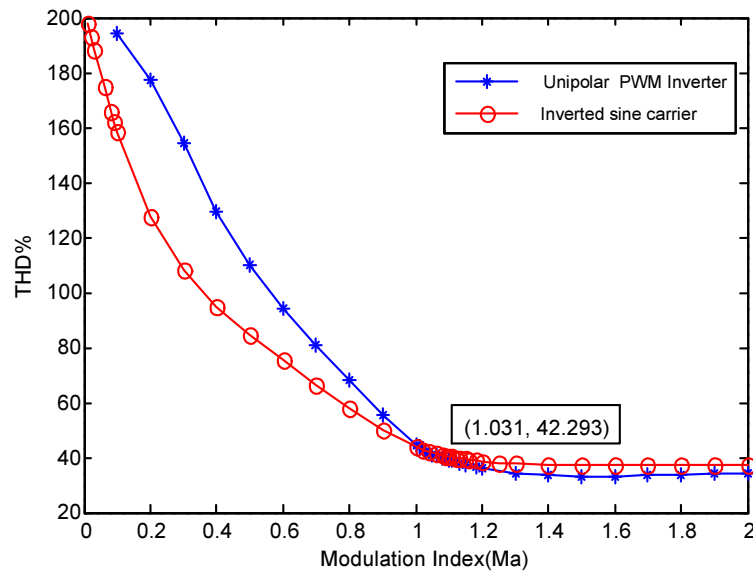


Fig. 10 – Variation of THD with modulation index.

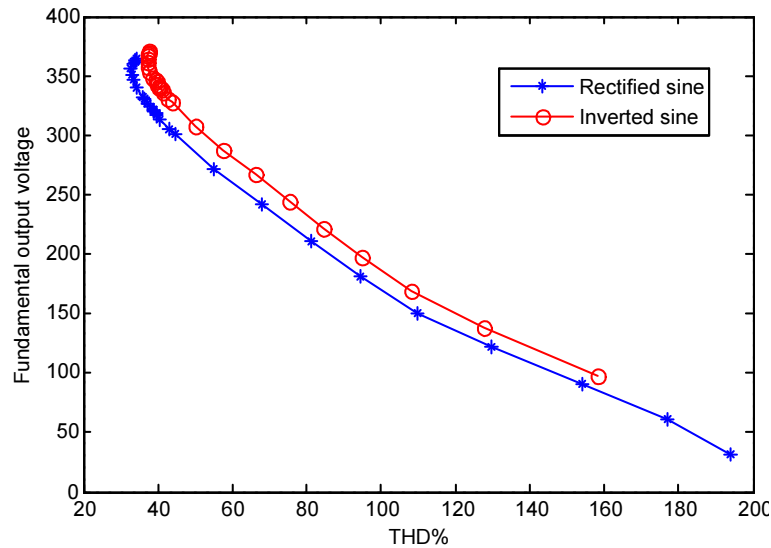


Fig. 11 – Values of THD for various output fundamental.

A Overmodulation

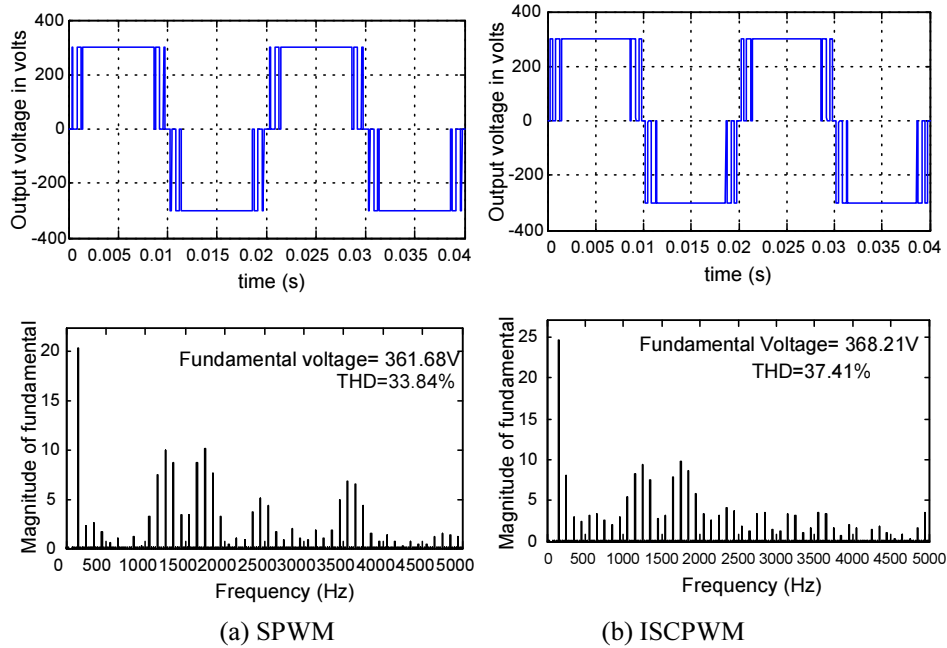


Fig. 12 – Output voltage and frequency spectrum-overmodulation.

To increase the fundamental amplitude further in the SPWM technique the only way is increasing the M_a beyond 1.0, which is called as an overmodulation. Overmodulation causes the output voltage to contain many more low order harmonics (3, 5, 7...etc.) and also the makes the fundamental component-modulation index relation non-linear linear. As M_a increases the on-time become proportionally larger and improves the value of the fundamental component in non-linear manner. As the proposed ISCPWM gives improved fundamental component, to some extend it replaces the overmodulation and avoids pulse dropping. For still higher values of fundamental, ISCPWM also has equally good opportunity to work in the overmodulated region. To understand the performance of the schemes in overmodulation range, the simulated spectral outputs are presented in Fig. 12 for $M_a = 1.8$. The result shows that though the ISCPWM works better than the traditional SPWM in overmodulation; its performance can not appreciated to the extent as in linear range.

B Amalgamation

The reference modification in harmonic injection PWM methods and carrier modification in the proposed ISCPWM aim at increasing the fundamental

through increase in the pulse area. As the aim of both the modifications is same, amalgamation of both reference and carrier modifications will improve the situation further. On the basis of this intuitive notion, it is logical to amalgamate the inverted sine carrier with third harmonic and triplen harmonic injected reference waveforms may be amalgamated in the three-phase system to improve the system further. Fig. 13 depicts such results obtained from amalgamated operation with third harmonic injection reference, which results in 19.73% enhancement in fundamental than SPWM, which is greater than the fortification obtained when triplen harmonic injected reference alone is used.

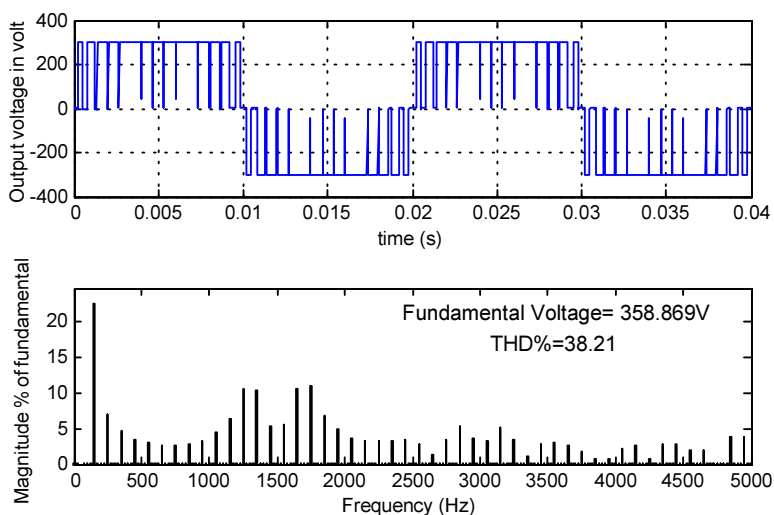


Fig. 13 – Output voltage and frequency spectrum-amalgamated operation.

5 Hardware Implementation

FPGA belongs to the wide family of programmable logic components [13]. Their densities are now exceeding 10 million gates [14]. The architecture is composed of a matrix of CLB, which is bordered by a ring of configurable input/output blocks (IOB). All these resources communicate among themselves through a programmable interconnection network and also fit to PWM signal, where it is subjected into certain hardware-oriented constraints. The algorithm uses the LUT for the sine reference and triangular/inverter sine carrier functions. The system (board) clock is divided and adjusted with the data count in LUT's. The carrier data is repeatedly called for M_f times recursively and compared with the sine reference data based on TRR algorithm [15]. When the reference is greater than the carrier data, a pulse will be produced.

The target technology uses one of the Xilinx series of FPGA. The circuit has been designed using VHDL, synthesized, placed and routed using the Xilinx

integrated service environment. The functionality of the final net list/design verification for the pulse generation has been completed using ModelSim SE-EE5.4e simulator in project navigator as evidenced in Fig. 14. After verifying the design by simulation, synthesis is carried out. Finally placement, routing and timing optimizations are performed. A proto-type inverter has been constructed using IRF840 MOSFET. Both SPWM and ISCPWM modulators have been tested with the help of a SRAM-FPGA based Xilinx family spartan-3 XC3S400-4-pq208. The XC3S400-4 pq208 has 400K logic gates, logic cells 8064, CLB is 896, distributed RAM bits 56K, and maximum user input/output is 264. The representative downloaded pulses are captured using fluke scope (199C series) and are shown in Fig. 15.

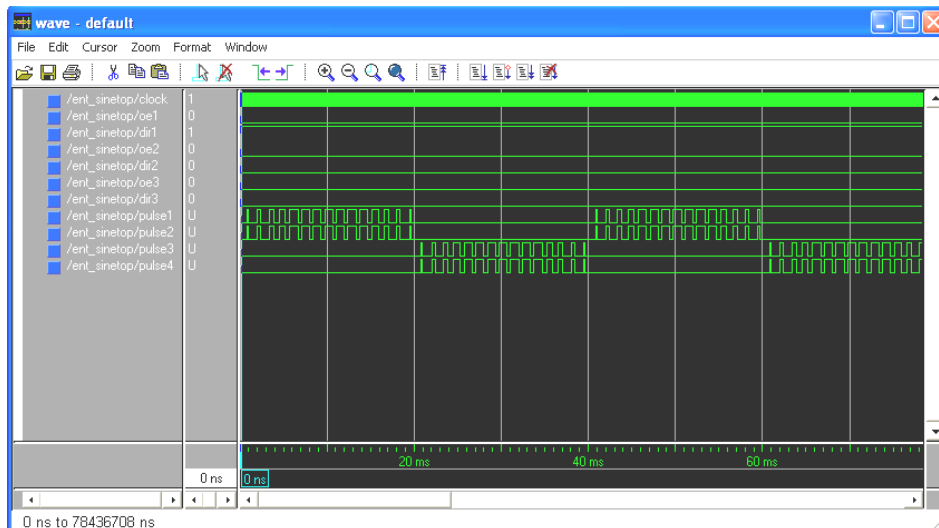


Fig. 14 – ModelSim Simulator Output Results.

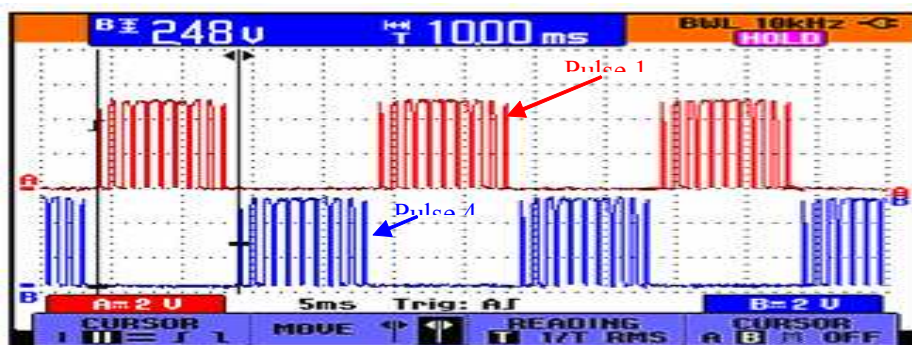


Fig. 15 – FPGA generated Switching Pulses 1 and 4.

6 Conclusion

The paper presents a novel PWM scheme for controlling the output of an inverter with improved fundamental component value. The main advantage of this approach is that it adopts a consistent strategy for the entire range of modulation index i.e. it does not require any mode change and also causes exactly same number of switching per cycle. The appreciable improvement in THD in the lower range of modulation depth attracts drive applications where low speed operation is required. The reduced distortions even at low modulation depth provide scope for proposed scheme not only when higher fundamental demanded and also obtaining low fundamental values. This paper also presents a systematic way to analytically characterize both SPWM and ISCPWM. The drawbacks of the proposed scheme are marginal boost in the lower harmonics and non-linear fundamental and M_a relation.

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