Research Square

Preprints are preliminary reports that have not undergone peer review. They should not be considered conclusive, used to inform clinical practice, or referenced by the media as validated information.

Investigating the Impact of Self-Heating Effects on Some Thermal and Electrical Characteristics of Dielectric Pocket Gate-All-Around (DPGAA) MOSFETs

Vaibhav Purwar (vaibhav193@gmail.com)
Rajasthan Technical University https://orcid.org/0000-0002-2462-5473
Rajeev Gupta
Rajasthan Technical University
Pramod Kumar Tiwari
IIT Patna: Indian Institute of Technology Patna
Sarvesh Dubey
Dr B R Ambedkar University

Research Article

Keywords: HCI, Electro-thermal (ET) Effects, Thermal contact resistance, Ambient Temperature, Phonons, Optical mode, Acoustic mode

Posted Date: September 16th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-876605/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

Abstract

The dielectric pocket gate-all-around (DPGAA) MOSFET is being considered the best suited candidate for ULSI electronic chips because of excellent electrostatic control over the channel. However, the phenomena of self-heating and hot carrier injection (HCI) severely affect the performance of the device, and make the behaviour of the DPGAA FET very unpredictable. In the present article, a comprehensive investigation under the influence of self-heating effects has been done for the variation in the lattice and carrier temperature against spacer length, ambient temperature, device length, and thermal contact resistance including *ON* and *Off* currents with gate bias voltage (V_{GS}). In order to analyse the *SHEs*, the hydrodynamic (HD) and thermodynamic (TD) transport models have been used for three-dimensional (3D) electrothermal (ET) simulation. The Lucky (hot carrier injection) model has been used to study the HCI degradation in DPGAA MOSFET using Sentaurus 3D TCAD simulator.

1. Introduction

Under the arena of nanoscale CMOS technology, the gate-all-around (GAA) MOSFET is one of the most promising devices. The published reports [1] claimed that the device could have excellent channel control, better subthreshold characteristics, large packing density, and short channel effects (SCEs) immunity [2]. Moreover, according to More Moore (IRDS), the CMOS structure has the feasibility to be downscaled below 22nm [3]. Reports say that the GAA CMOS Technology node shall reach 3nm by 2022, and one of the leading fabrication industries has proposed adopting the GAA structure for their upcoming CMOS Technology node [4]. For further improvement in the device performance, dielectric pockets (DPs) have been introduced in the channel region at the drain-channel and source-channel interface. The DP MOSFET is getting a lot of attention as a potential architecture due to restrained SCEs and minimized *Off*-current [5–6]. The *Off*-current (I_{off}) gets reduced as the DP acts as a diffusion stopper and impedes the path of punch through [7].

Although downscaling of the device increases the number of transistors per unit area on a chip, the chip suffers from high power dissipation and self-heating problem with the passage of time [8–9]. The shrinkage in device dimensions results in unbalanced scaling of dimensional parameters and supply voltage which causes a high electric field (~ 1MV/cm) near the channel-drain junction. This high electric field energizes the charge carriers to higher energy levels whence they become hot carriers. Accumulated hot carriers in the channel give rise to self-heating problem in the gadget [10–14]. The heating effect severely deteriorates the performance of the device owing to mobility reduction, increased gate leakage current, downfall in drain saturation current [15]. Moreover, the degradation in device performance also comes from electrothermal (ET) issues due to variation in ambient temperature, injection of hot-carrier, etc [16].

Some researchers have investigated self-heating effect (SHE) in silicon-based GAA MOSFETs [17–18]. *Park et al*. [17] studied the ET effects and degradation of drain current in GAA MOSFETs with vertically stacked multiple silicon-based nanowire channels. *Chin et al*. [18] developed an ultrafast high-resolution

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

thermo-reflectance (TR) imaging technique for investigating the increase in local surface temperature and high-resolution measurements by heating and cooling at constant time. Further, *Kompala et al.* [19] investigated the device performance degradation by the ET conductivity problem owing to the lower thermal conductivity of gate oxide, spacer region material, and higher thermal contact resistance (R_{th}). *Pala et al*. [20] studied the effect of self-heating with quantum confinement effects (QCEs) in the Nano-electronic device. *Asheghi et al*. [21] calculated the degradation in thermal conductivity due to the phonon-boundary scattering in terms of a simple mathematical model. It revealed the excessive drain current degradation due to SHEs in Silicon-based GAA MOSFETs. *A. Kumar et al*. [22] depicted that SHE and HCI severally degrade the performance of DGAA MOS due to high gate leakage current. *I. Myeong et al.* [24] reveal the effect of air gap/spacer for changing the thermal property of VFET. *S. Banchhor et al.* [25] analysed that SHE causes zero temperature coefficient (ZTC) bias-point instability in SOI-FINFETs. To date, the influence of ambient temperature (T_A), Drain voltage (V_{DS}), and device parameters such as spacer length, spacer conductivity, device length, and thermal contact resistance on carrier temperature, lattice temperature, along with hot carrier injection (HCI) induced degradation of DPGAA FET has not been investigated in detail.

The present work is dedicated to discuss the comprehensive study of variation in lattice temperature (T_L) and carrier temperature (T_C) against ambient temperature (T_A), drain-to-source voltage (V_{DS}), and different device geometries of the DPGAA MOSFET. The work also includes the study of hot carrier injection (HCI) in the device. All the mentioned works has been carried out using electrothermal (ET) simulation. The entire manuscript is organized as: Section II covers the device structure and methodology. Section III describes the results and discussion, and finally section IV sums-up the work.

2. Device Structure And Simulation Methodology

The 3D schematic diagram of DPGAA MOSFET for simulation on Sentaurus device simulator is shown in Fig. 1. In this structure, the silicon-based nanowire channel region is wrapped around by a thin oxide layer and contact metal (Tungsten Nitride) with a work function of 4.7eV [25]. Molybdenum (Mo) is used as a source/drain contact metal. All other physical parameters of the DPGAA MOSFET architecture for simulations are listed in Table I, and the thermal parameters used for electrothermal (ET) simulations are listed in Table II.

Table- I

Device parameters used for DPGAA MOSFET simulation.

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

Sl. No.	Parameter	Symbol	Value
1	Channel Length	L_C	20 nm
2	Source/Drain Doping	N_D	10^{20} cm^{-3}
3	Channel doping	N_A	10^{15} cm^{-3}
4	Oxide thickness	t_{ox}	2 nm
5	Channel thickness	t_{si}	10 nm
6	Metal Work-function	ϕ_M	4.7 eV
7	Dielectric pocket length	DP_L	4 nm
8	Dielectric pocket thickness	DP_D	4 nm
9	Spacer Length	L_{SP}	10-30 nm
10	Source/Drain Contact Length	L_{SC}/L_{DC}	5 nm
11	Thermal Contact Resistance	R_{th}	1×10^{-5}- 1×10^{-4} cm^2KW^{-1}
12	Gate-to-source voltage	V_{GS}	0-1V
13	Drain-to-source voltage	V_{DS}	0-1.2V

Table- II

Thermal conductivity parameters used for Device simulation using Ref [12].

Sl. No.	Material	Thermal conductivity (W/K-cm)
1	Channel Region (Si)	0.25
2	Source/Drain Region (Si)	0.62
3	SiO_2	0.014
4	Si_3N_4	0.185
5	Al_2O_3	0.02

The Hydrodynamic (HD) and Thermodynamic (TH) transport models have been coupled for the purpose of simulation. The HD model [26] acquires the electrothermal (ET) characteristics of carrier transport along with the carrier temperature (T_C) effect. The lattice temperature (T_L) variation has been obtained by

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

nsity gradient model is applied for solving the

quantum confinement effects (QCEs) of the charge carriers in the channel region. For the electrothermal (ET) simulation, the temperature-dependent thermal conductivity (TC) model [26] is applied for silicon TC dependence on channel film thickness. The Lombardi (CVT), Philips unified mobility, and high field saturation models have been used to simulate temperature, carrier concentration, and carrier-to-carrier scattering dependent carrier mobility. The constant thermal contact resistance value at an isothermal ambient temperature of 300K has been used for thermal boundary conditions of device terminals. Fig. 2a and Fig. 2b show the calibrated transfer characteristics for appropriate models and simulation data validation.

3. Results And Discussion

3.1 Effect on Lattice and Carrier temperature

The onset of self-heating occurs when the nearly free conduction band electrons in the channel region are accelerated by the electric field because of rise in the drain voltage (V_{DS}). The electrons (carriers) gain energy from the field and consequently, carrier temperature (T_C) increases. The carriers lose energy by inelastically scattering with the lattice phonons, where the carriers with energies below 50 meV scatter mainly with acoustic phonons, whereas, those with higher energy scatter strongly with the optical modes [27]. Such scattering events result in transfer of energies (heat) to the crystal lattice, and hence carrier temperature (T_C) is found much higher than the lattice temperature (T_L) (i.e., $T_C >> T_L$). In Fig. 3, the variations of the maximum lattice temperature (T_{Lmax}) and carrier temperature (T_{Cmax}) against V_{DS} for V_{GS} = 1 are shown. It be observed that T_{Cmax} and T_{Lmax} increase gradually up to 0.1V of V_{DS} owing to low-field transport (LFT) mechanism. On the other hand, for V_{DS} from 0.1V to 1V, T_{Lmax} and T_{Cmax} could be seen rising from 303K to 398K and 360K to 2664K because of high-field transport (HFT) mechanism. It may be noted that enhancement in carrier temperature results in phonon emission, where a significant portion of the generated phonons correspond to optical modes (low group velocity) or acoustic modes. Figure 4 deals with the changes in T_{Lmax} and T_{Cmax} against change in spacer lengths (L_{SP}) at V_{DS} = V_{GS} = 1V. The expansion in spacer length (L_{SP}) at fixed channel length extended the space between side contacts with the channel. It produced two effects (a) the induced electric field gets reduced along the channel length at the same value of V_{DS} and diminished the carrier energy, as a result of which T_{Cmax} got reduced. (b) The heat dissipation path extended for the channel from cooling sinks (metallic contacts of D/S) and caused the increase in T_{Lmax}. As per Fig. 4, against the variation of L_{SP} from 10nm to 30nm, the T_{Lmax} rises from 333K to 398K(~ 16% increase), and conversely T_{Cmax} falls from 3131K to 2664K(~ 15% decrease). Figure 5 displays the contour plots of (a) lattice temperature and (b) electron temperature in silicon nanowire along device length (nm) at V_{GS} = V_{DS} = 1V. Hot carriers (high energy carriers) moving from the source undergo heavy scattering near the drain side and give their energy in the form of phonons to the lattice. Consequently, there is increase in lattice temperature (T_L) near the drain region locally. Note that, the area of maximum lattice temperature (T_{Lmax}) is known as a '*Hotspot*', where the density of optical phonons is the maximum. The variations in T_L and T_C against the device length for the

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

fixed values of V_{DS} and V_{GS} at 1V are demonstrated in Fig. 6. It is already mentioned earlier that near the channel-drain interface, the energy of carriers gets sufficiently high owing to high electric field which make them hot. In Fig. 6, it can be easily observed that the electron temperature (T_C) near the channel-drain interface ($\approx 55\text{nm}$) reaches the peak value which is near 2500K. Note that, in the course of journey from source to drain, the carriers gain energy, and at the same time they also got scattered with lattice ions which results in generation of phonons. Therefore, an increase in lattice and carrier temperature may be observed in the plot. When the hot carriers enter the drain region, due to reduced mean free path length, there is a surge in electron-lattice scattering events resulting in a steep increment in lattice temperature as obvious from the Fig. 6. At the same time, it can be seen that the carriers lose their energy through scattering and their temperature starts decreasing from the channel-drain interface. Near the metallic contact, the lattice temperature again starts decreasing due to heat dissipation through the metallic contact.

3.2 Output and Transfer characteristics under SHE

Figure 7 shows the behaviour of output characteristics of the DPGAA MOSFET versus V_{DS} with *SHE* and without *SHE* for different V_{GS}. Self-heating causes the carrier mobility to degrade in the channel near the drain side due to populated hot carriers scattering, which result in the downfall of drain saturation current with the increase of V_{DS} at a particular value of V_{GS}. As per Fig. 7, the drain saturation current decreases due to *SHE* by approximately 8% in DPGAA MOSFET at V_{GS}=1V. The next figure (Fig. 8) depicts the transfer characteristics of DPGAA versus V_{GS} with *SHE* and without *SHE*.at V_{DS}=0.75V. It depicts that the *on*-state current of DPGAA degrades with SHE on increasing value of V_{GS}. The degradation of electron mobility and electron velocity along device length (nm) at V_{GS}=V_{DS}=1V is shown in Fig. 9. The electron mobility degrades by approximately 50% from source-channel to drain-channel interface. However, the electron velocity increases suddenly with a significant peak value (1.37×10^8 cm/s) in the channel region and tends to decrease near the drain and channel interface in the drain region.

3.3 SHE variations due to thermal contact resistances (R_{th})

Thermal contact resistance (R_{th}) plays a vital role in the heat transfer mechanism of the device. The low value of R_{th} provides a fast thermal conducting path for heat flow from the device through source and drain contacts. Figure 10 & Fig. 11 depict the increase in Lattice and carrier temperature for higher values of thermal contact resistances (R_{th}), respectively. According to Fig. 10, when R_{th} varies from $1\times10^{-5}cm^2KW^{-1}$ to $1\times10^{-4}cm^2KW^{-1}$, lattice temperature ($T_L$) increases from 332K to 472K (~ 42%increase). On the other hand, in Fig. 11, the electron temperature (T_C) can be seen increasing with an increase in R_{th} near the source and drain contacts, but the '*hotspot*' carrier temperature T_{Cmax} seems independent against the variation in R_{th}. The variation of maximum lattice temperature (T_{Lmax}) with thermal conductivity of spacers for various values of R_{th} is plotted in Fig. 12. It has been observed that if the thermal conductivity of spacers increases from 0.14W/K-cm to 0.185W/K-cm, the T_{Lmax} gets reduced by

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

around ~ 5.1% for R_{th} = 5×10^{-5}cm^{2}KW^{-1}. Obviously, the thermal conductivity of spacers may play important role in fighting with self-heating effects. Figure 13 shows the variation of the drain current versus R_{th} for various types of gate insulators. The drain current decreases from 39.8μA to 25.3μA (~ 36.4% decrease) for Al_2O_3, 38.9μA to 24.6μA (~ 36.8% decrease) for Si_3N_4 and 35.5μA to 22.3μA (~ 37.2% decrease) for SiO_2, respectively, which claims the scope of high K-dielectric (Al_2O_3) material to get the high drain current.

3.4 Gate Leakage current under HCI degradation

This section is dedicated to discuss the gate leakage current (I_G) under hot carrier injection with *SHE* for the DPGAA MOSFET. The hot carrier injection model (LUCKY) [28] is used in the ET simulation of the device. It is used to extract the significant values of the carriers injected into the gate oxide near the '*hotspot*' region. Because of the presence of a strong vertical electric field in the channel region, the significant tunnelling current occurs through the gate oxide near the '*hotspot*' region. These injected carriers break the ionic bonds of the gate oxide and create a tunnel, as a result of which gate leakage current (I_G) enhances and the drain saturation current (*ON*-current) degrades in the device [29]. In Fig. 14, the variation of the gate leakage current versus spacer length (L_{SP}) is plotted. Against the variation of spacer length from 10nm to 30nm, the gate leakage current (I_G) decreases from 13.5nA to 4.8nA (~ 64.5% decrease). It is explained earlier that the considerable spacer length reduces the carrier temperature (T_C) and hence causes a reduction in leakage current.

3.5 *Effect of Ambient temperature (T_A) variations*

The ambient temperature (T_A) is one of the crucial factors of *SHE* degradation [14]. Here, ET simulation has been used to investigate the *SHE* in DPGAA MOSFETs to analyse the impact of T_A. Figure 15 demonstrates the variation of the maximum lattice temperature (*hotspot* temperature) (T_{Lmax}) versus ambient temperature (T_A) for the various values of R_{th}. The T_{Lmax} increases from 398K to 494K (~ 24.1% increase) with the rise in T_A from 300K to 400K for R_{th} = 5×10^{-5}cm^{2}KW^{-1}. The variation of the drain current (I_D) against ambient temperature (T_A) for the various values of R_{th} is plotted in Fig. 16. Increasing T_A from 300K to 400K, the I_D decreases from 37.8μA to 35μA (~ 7.5% decrease) because the lateral electric field degrades the carrier mobility at R_{th} = 5×10^{-5}cm^{2}KW^{-1}. Figure 17 demonstrates the cutline plot of the variation in lattice temperature (T_L) versus device length (nm) for increasing T_A values (300K to 400K in a step of 20K). The drain lattice temperature (T_L) is higher than the channel and source regions because the high electric field enhances the scattering in the drain region. However, the T_L increases with an increase in T_A.

4. Conclusion

The *SHEs* and HCI degradation in dielectric pocket gate-all-around (DPGAA) MOSFET has been discussed using ET simulation. Under the *SHE* it is observed that the drain saturation current of DPGAA degrades by

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

8%, whereas, when compared with GAA MOSFET, the drain saturation current under SHE is found to be reduced by 1%. The *Off*-state current (I_{OFF}) of DPGAA being reduced by 57% as compared with GAA. Hence the I_{ON}/I_{OFF} ratio of DPGAA is found to be improved significantly. However, *SHE* may be ameliorated when the carrier temperature gets reduced by 15% and lattice temperature increases by 16% against the increase in spacer length (L_{SP}) from 10nm to 30nm. It is further noted that the HCI gets diminished for a similar increment in spacer length as the gate leakage current is reduced by 64.5%. The self-heating effect gets intensified because of rise in lattice and carrier temperature by 42% with the rise of thermal contact resistance (R_{th}) from $1\times10^{-5}cm^2KW^{-1}$ to $1\times10^{-4}cm^2KW^{-1}$. Therefore, the significant spacer length (L_{SP}) with appropriate thermal contact resistance may be utilized to design a less prone device from self-heating and HCI degradation.

Declarations

Acknowledgment

Not applicable.

Funding Statement

This work did not receive a financial support.

Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

Author Contribution

All authors have made substantial contributions to the conception and design, or acquisition of data, or analysis and interpretation of data; have been involved in drafting the manuscript or revising it critically for important intellectual content; and have given final approval of the version to be published. Each author has participated sufficiently in the work to take public responsibility for appropriate portions of the content. All authors read and approved the final manuscript.

Availability of data and material

The data and material are available within the manuscript.

Compliance with ethical standards

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

The authors declare that all procedures followed were in accordance with the ethical standards.

Consent to participate

All the authors declare their consent to participate in this research article.

Consent for Publication

All the authors declare their consent for publication of the article on acceptance.

References

1. GAA FET Technology Market – Forecast (2021–2026) [Online] available: https://www.industryarc.com/Report/19199/GAA-FET-technology market.html Accessed 15 August 2021
2. Lu W, Xie P, Lieber CM (2008) Nanowire transistor performance limits and application. IEEE Trans Electron Devices 55:2859–2876
3. International Roadmap for Devices and Systems (IRDS) More Moore. [Online] Available:https://irds.ieee.org/images/files/pdf/2017/2017IRDS_ES.pdf, Accessed 15 August 2021
4. Nancy Cohen Samsung at foundry event talks about 3nm, MBCFET developments [Online] Available:https://techxplore.com/news/2019-05-samsung-foundry-event-3nm mbcfet.html, Accessed 15 August 2021
5. Jurczak M, Skotnicki T, Gwoziecki R, Paoli M, Tormen B, Ribot P, Dutartre D, Monfiray S, Galvier J (2001) Dielectric pocket- A new concept of the junctions for deca-nanometric CMOS devices. IEEE Trans Electron Devices 48:1770–1774
6. Awasthi H, Kumar N, Purwar V, Dubey S (2020) Impact of Temperature on Analog/RF Performance of Dielectric Pocket Gate-all-around (DPGAA) MOSFETs. Silicon https://doi.org/10.1007/s12633-020-00610-2
7. Purwar V, Gupta R, Kumar N, Awasthi H, Dixit VK, Singh K, Dubey S, Tiwari PK (2020) Investigating linearity and effect of temperature variation on analog/RF performance of dielectric pocket high-k double gate-all-around (DP-DGAA) MOSFETs. Appl Phys A. https://doi.org/10.1007/s00339-020-03929-0
8. Pop E, Sinha S, Goodson K (2006) Heat generation and transport in nanometer-scale transistors. Proceedings of the IEEE 94:1601, 2006
9. Pop E (2010) Energy dissipation and transport in nanoscale devices. Nano Research 3:147–196
10. Rhyner R, Luiser M (2016) Minimizing self-heating and heat dissipation in ultrascaled nanowire transistors. Nano Lett 16:1022–1026

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

11. Jiang H, Shin S, Liu X, Zhang X, Alam MA (2016) Characterization of self-heating leads to universal scaling of HCI degradation of multi-fin SOI FinFETs. *Proceedings of International Reliability Physics Electronics Symposium* 2A.3.1-2A.3.7
12. Shrivastava M, Agrawal M, Mahajan S, Gossner H, Schulz T, Sharma DK, Rao VR (2012) Physical insight toward heat transport and an improved electrothermal modeling framework for FinFET architectures. IEEE Trans Electron Devices 59:1353–1363
13. Nakagome Y, Takeda Y, Kume H, Asai S (1982) New observation of hot-carrier injection phenomena. Jpn J Appl Phys 22:99
14. Venkateswarlu S, Sudarsanan A, Singh SG, Nayak K (2018) Ambient Temperature-Induced Device Self-Heating Effects on Multi-Fin Si n-FinFET performance. IEEE Trans Electron Devices 65:2721–2728
15. Braccioli M, Curatola G, Yang Y, Sangiorgi E, Fiegna C (2009) Simulation of self-heating effects in different SOI MOS architectures. Solid-State Electron 53:445–451
16. Srinivas PS, T N, Kumar A, Jit S, Tiwari PK (2020) Self-heating effects and hot carrier degradation in $In_{0.53}Ga_{0.47}As$ gate-all-around MOSFETs. Semicond Sci Technol. https://doi.org/10.1088/1361-6641/ab7f9b
17. Park JY, Lee BH, Chang KS, Kim DU, Jeong C, Kim CK, Bae H, Choi YK (2017) Investigation of Self-heating effects in gate-all-around MOSFETs with vertically stacked multiple silicon nanowire channels. IEEE Trans on Electron Devices 64:4393–4399
18. Shin SH, Wahab MA, Masuduzzaman M, Maize K, Gu J, Si M, Shakouri A, Ye PD, Alam M A (2015) Direct observation of self-heating in III-V Gate-all-around Nanowire MOSFETs. IEEE Trans on Electron Devices 62:3516–3523
19. Kompala BK, Kushwaha P, Agarwal H, Khandelwal S, Duarte J-P, Hu C, Chauhan YS (2016) Modeling of nonlinear thermal resistance in FinFET. Jpn J Appl Phys 55:04ED11
20. Pala MG, Cresti A (2015) Increase of self-heating in nanodevice induced by surface roughness: A full quantum study. Journal of Appl Phys 117:084313–084311
21. Asheghi M, Behkam B, Yazdani K, Joshi R, Goodson KE (2002)Thermal conductivity model for thin silicon-on-insulator layers at high temperatures.*Proc. IEEE Int. SOI Conf.*, pp. 51–52
22. Kumar A, Srinivas P S T N, Tiwari PK (2019) An insight into self-heating effects and its implications on hot carrier degradation for silicon-nanotube-based double gate-all-around (DGAA) MOSFETs. IEEE Journal of Elect Device Society. https://doi.org/10.1109/JEDS.2019.2947604
23. Banchhor S, Chauhan N,Anand B (2021) A new physical insight into the zero-temperature coefficient with self-heating in silicon-on-insulator fin field-effect transistor. Semicond Sci Technol. https://doi.org/10.1088/1361-6641/abd220
24. Myeong I, Shin H (2021) Study on self-heating effect and lifetime in vertical-channel field effect transistor. Microelectron Reliab. https://doi.org/10.1016/j.microrel.2021.114093

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

25. Jiang PC, Lai YS, Chen JS (2006) Dependence of crystal structure and work function of WN_X films on the nitrogen content. Appl Phys Letters 89:1–3
26. Synopsys (2016) *Sentaurus Device User Guide. Version N-2017.09*, Mountain View, CA, USA
27. Ferry D K (2013) Semiconductors bonds and bands," IOP Publishing, Bristol, UK, Sep. 2013. https://doi.org/10.1088/978-0-750-31044-4
28. Hu C (1979) Lucky-electron model of channel hot-electron emission. IEDM Tech. Dig, p 22
29. Shin S, Wahab MA, Masuduzzman M, Si M, Gu J, Ye PD, Alam MA (2014) Origin and implications of hot carrier degradation of gate-all-around nanowire III-V MOSFETs. Proc. IEEE Int. Rel. Phys. Symp.4A.3.1-4A.3.6

Figures

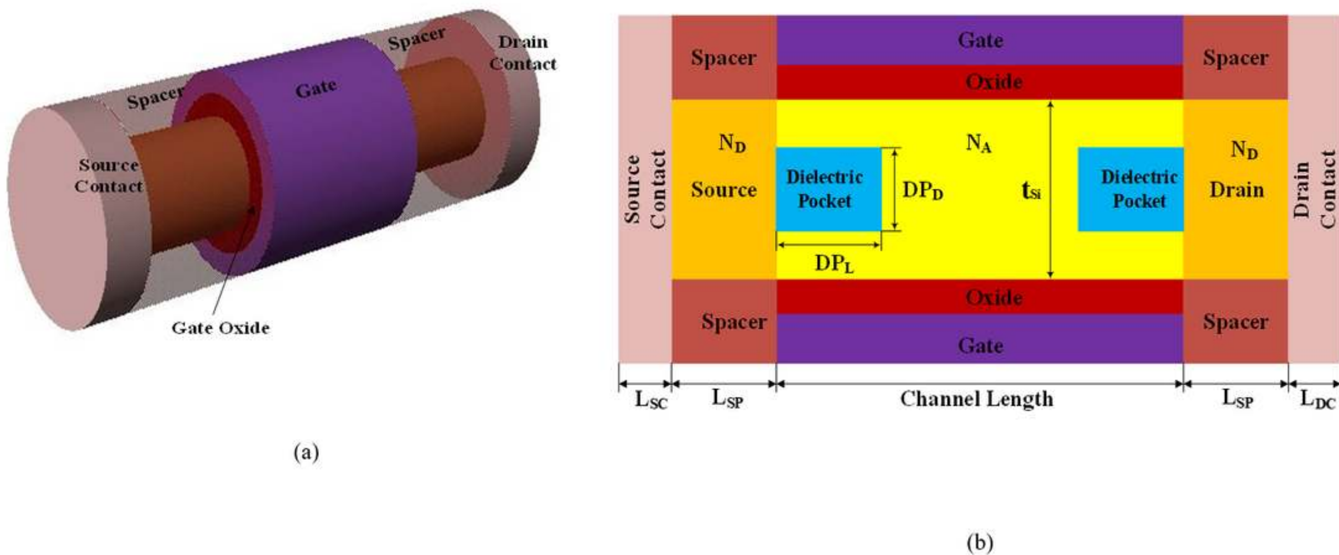
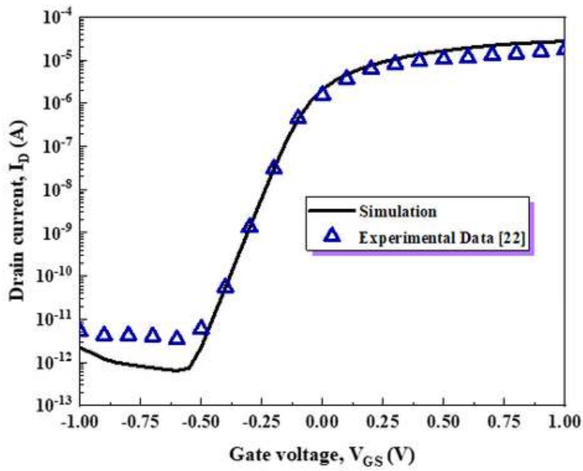
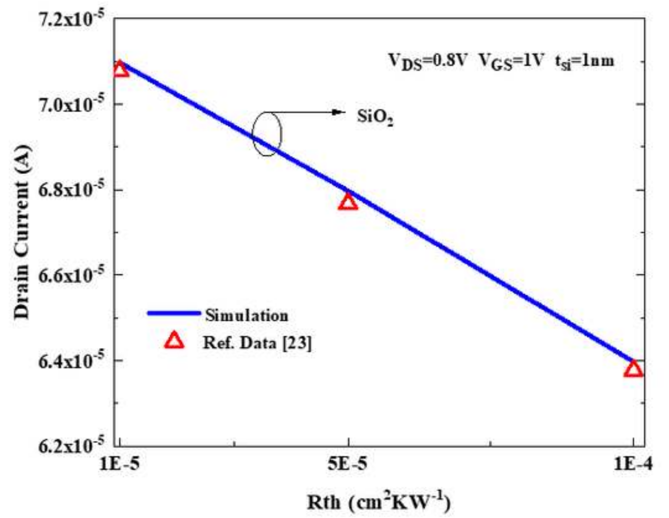


Figure 1

(a) The 3D schematic architecture of DPGAA MOSFET (b) The 2D schematic cut-plane of DPGAA MOSFET

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js



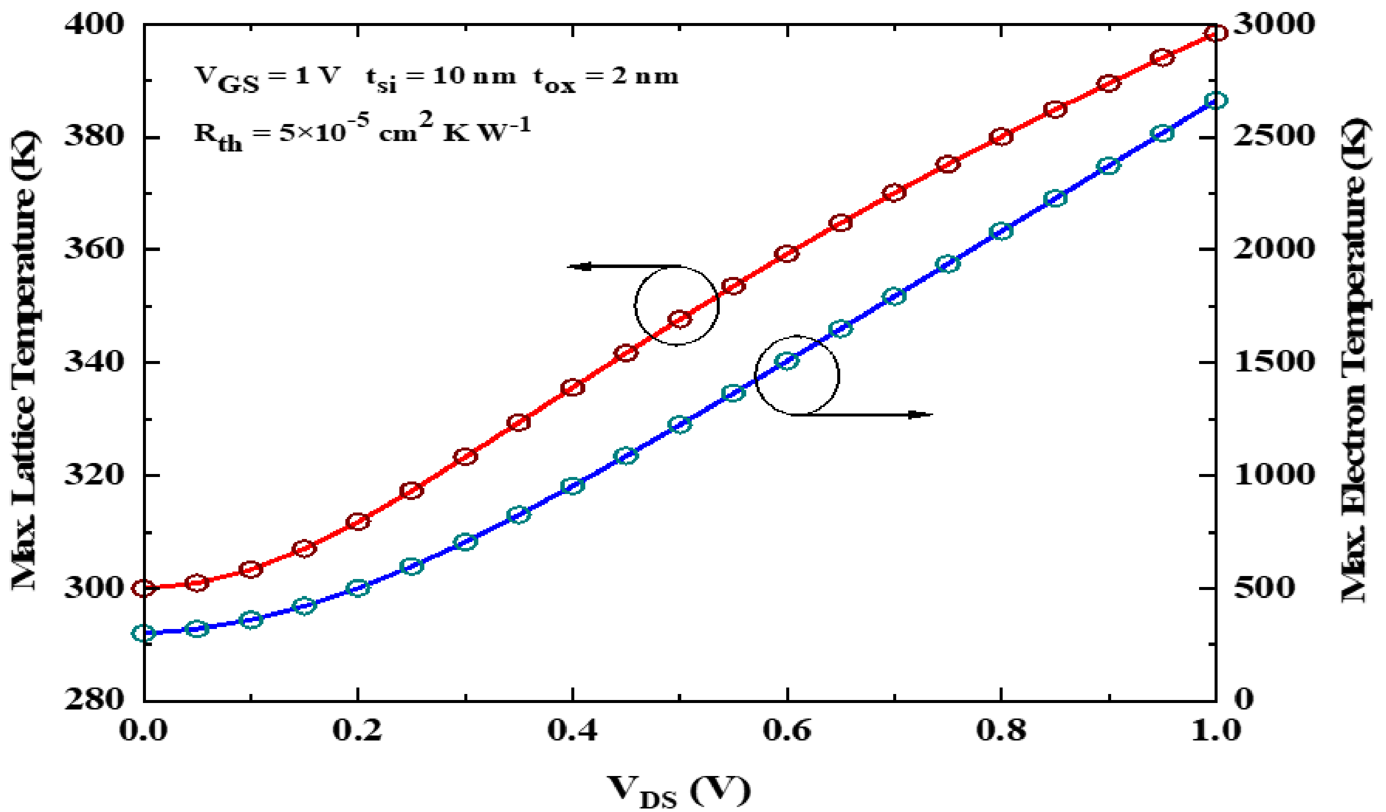


(a)

(b)

Figure 2

Comparison of transfer characteristics TCAD simulation with measured data of (a) Ref. [22] and (b) Ref. [23]



Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

Figure 3

Variation of maximum lattice temperature (TLmax) and maximum electron temperature (TCmax) versus drain-to-source voltage (VDS)

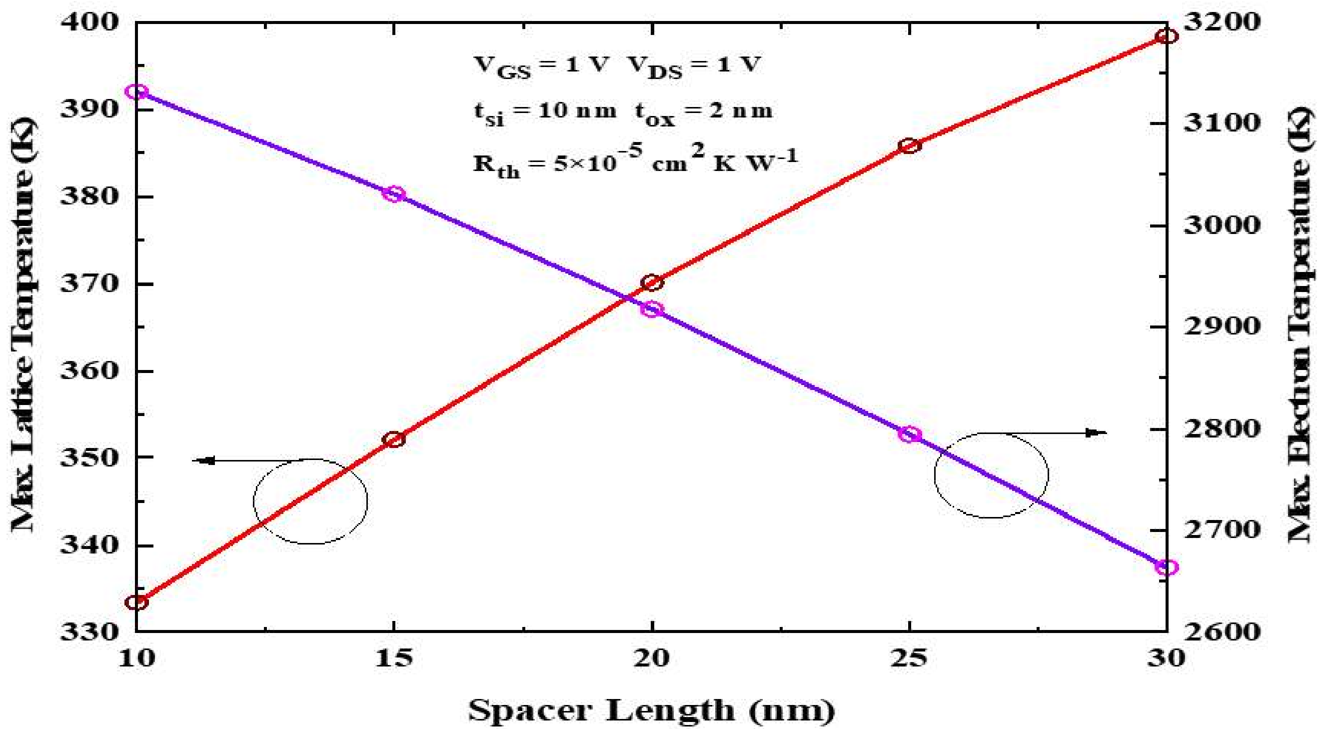


Figure 4

Variation of maximum lattice temperature (TLmax) and maximum electron temperature (TCmax) versus spacer length (LSP)

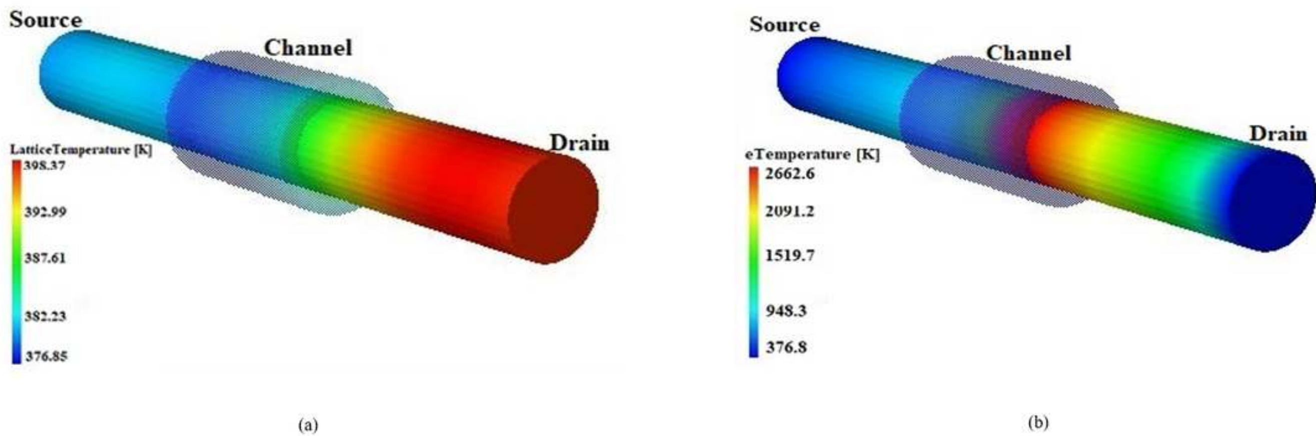


Figure 5

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

Contour plot of (a) Lattice temperature and (b) Electron temperature effects in Nanowire along device length (nm)

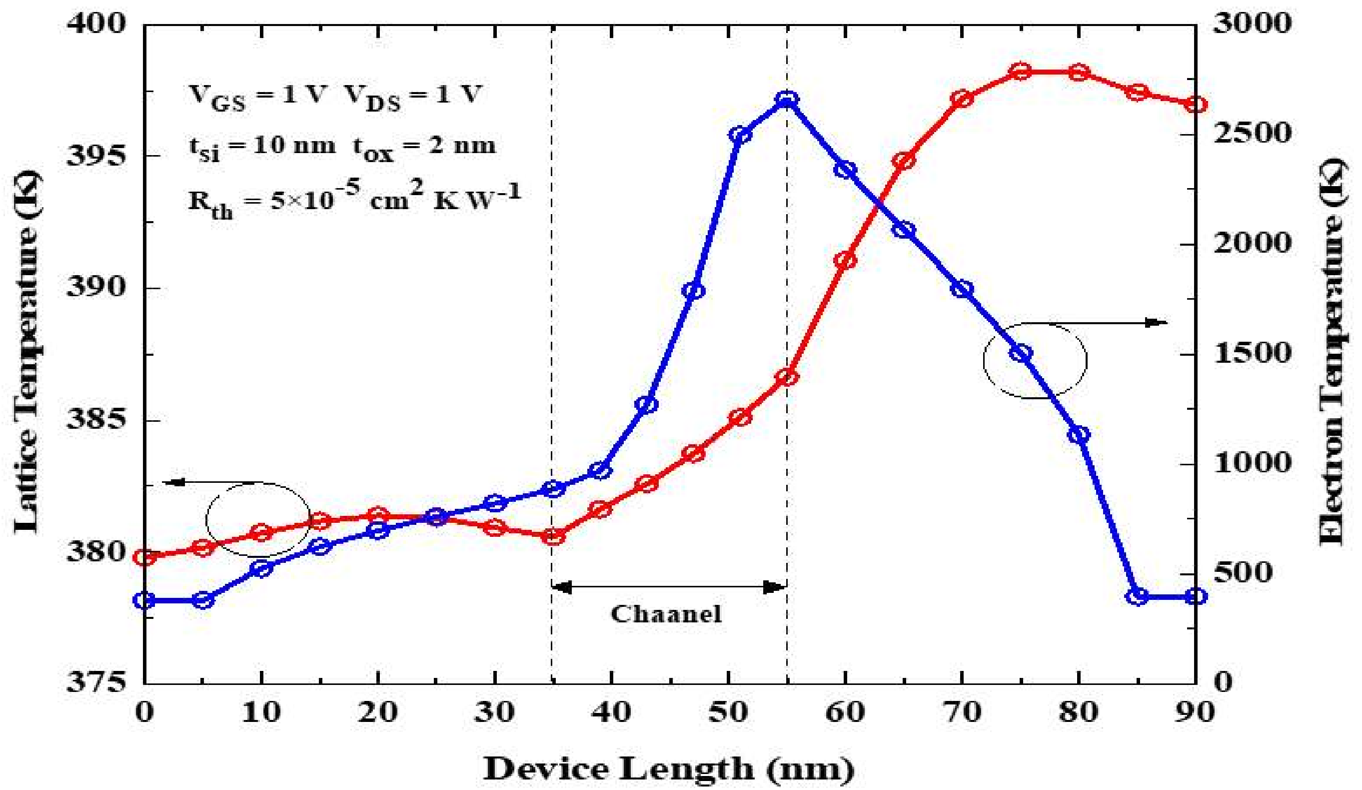


Figure 6

Cutline plot of the variation of lattice and electron temperature versus device length (nm)

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

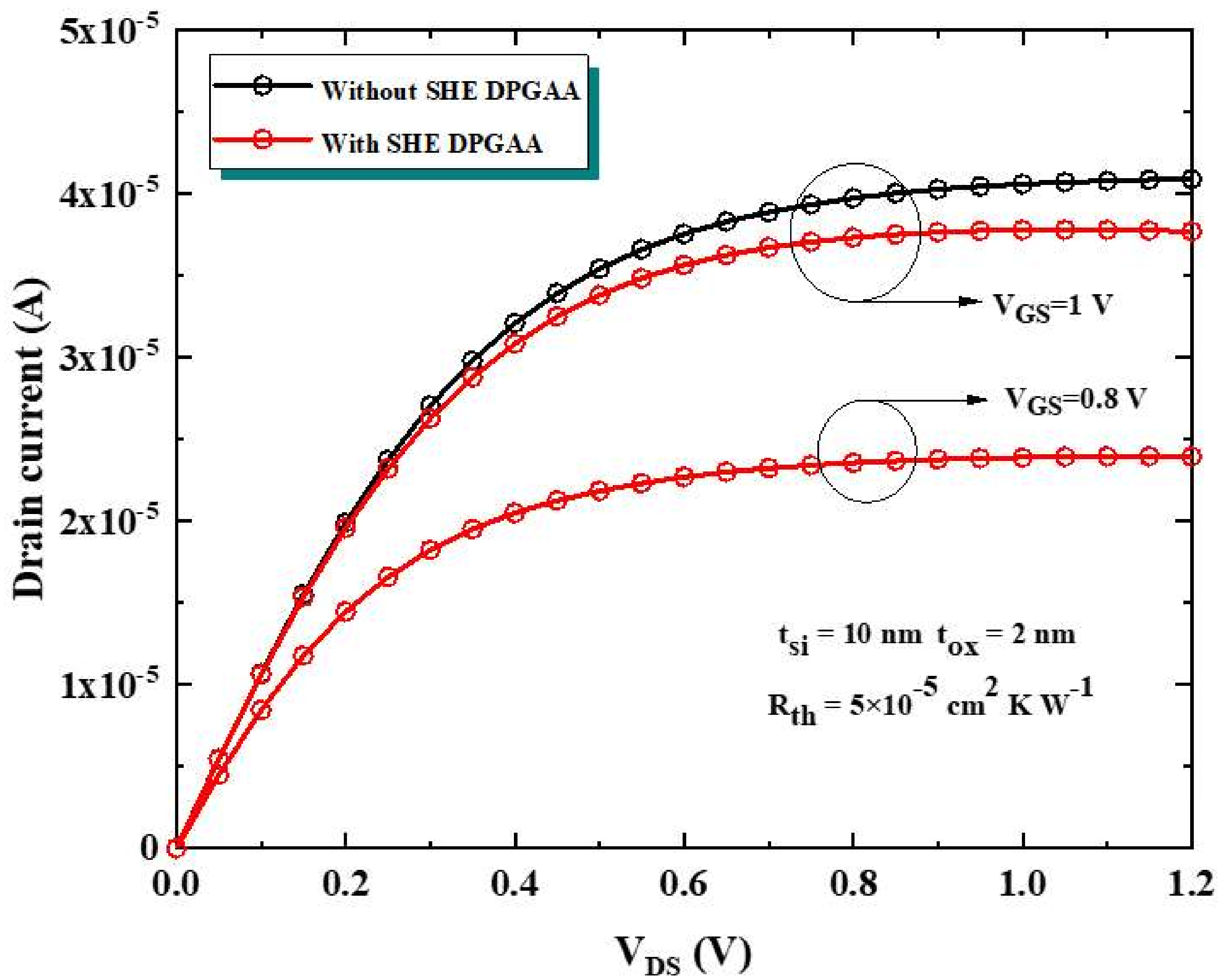


Figure 7

Comparison of output characteristics of DPGAA versus VDS with SHE and without SHE for different VGS

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

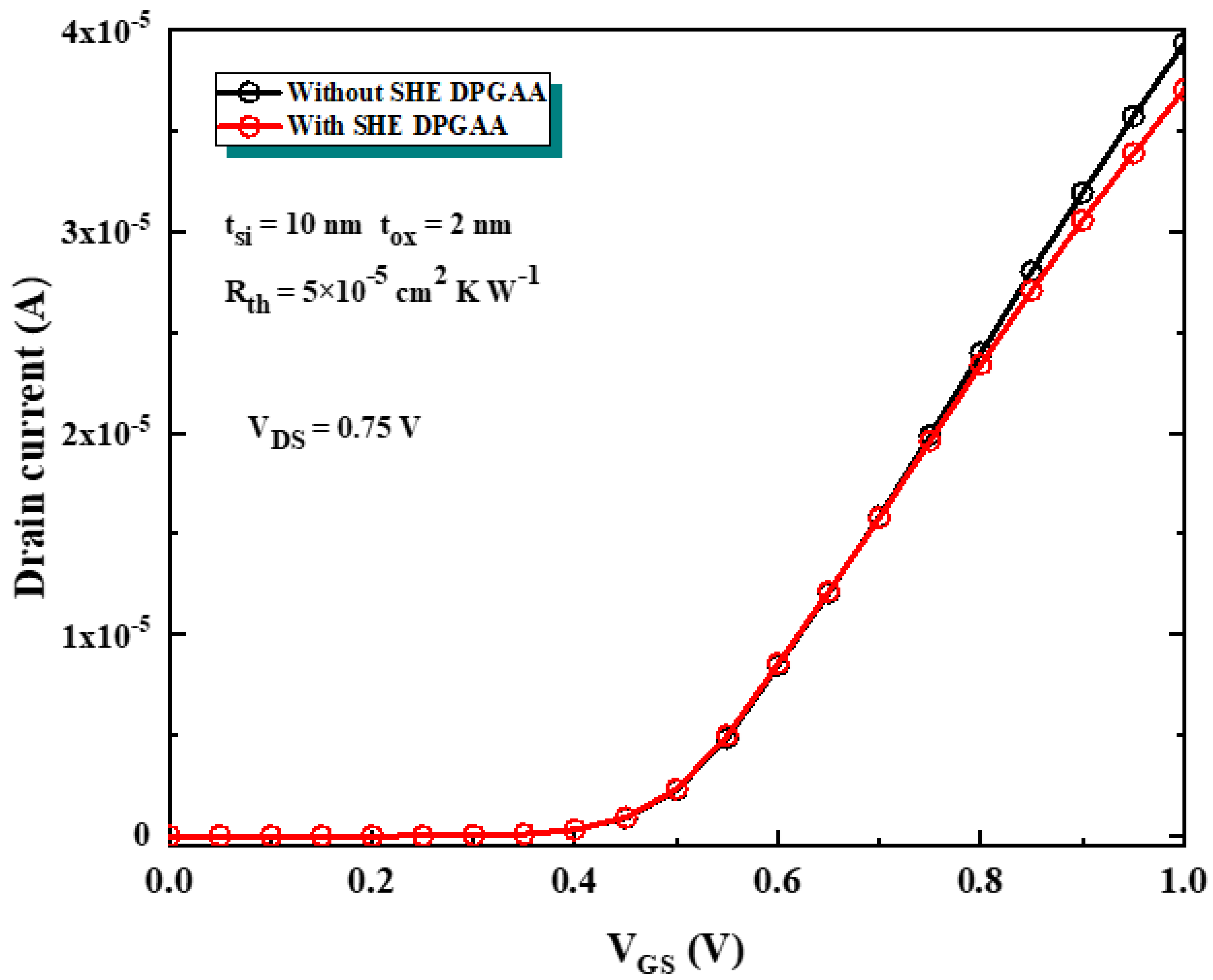


Figure 8

Comparison of transfer characteristics of DPGAA versus VGS with SHE and without SHE

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

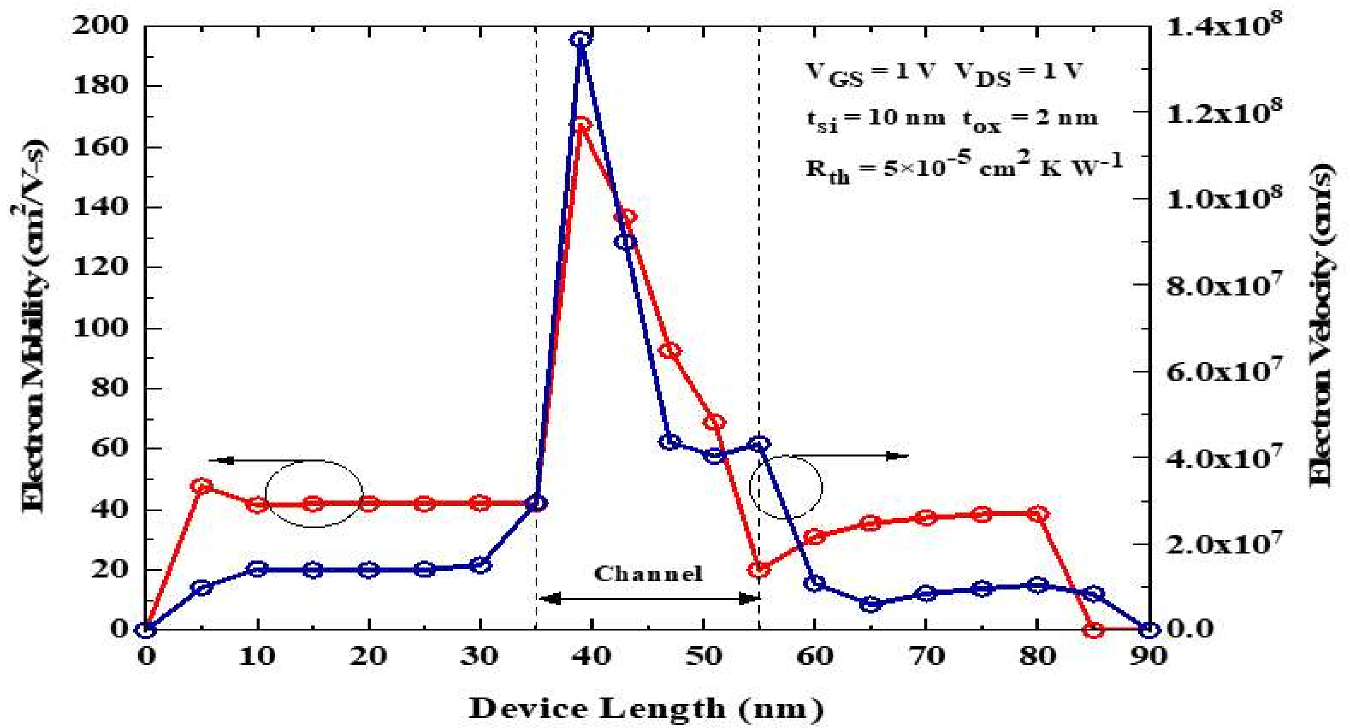


Figure 9

Cutline plot of variation of electron mobility and electron velocity versus device length (nm)

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

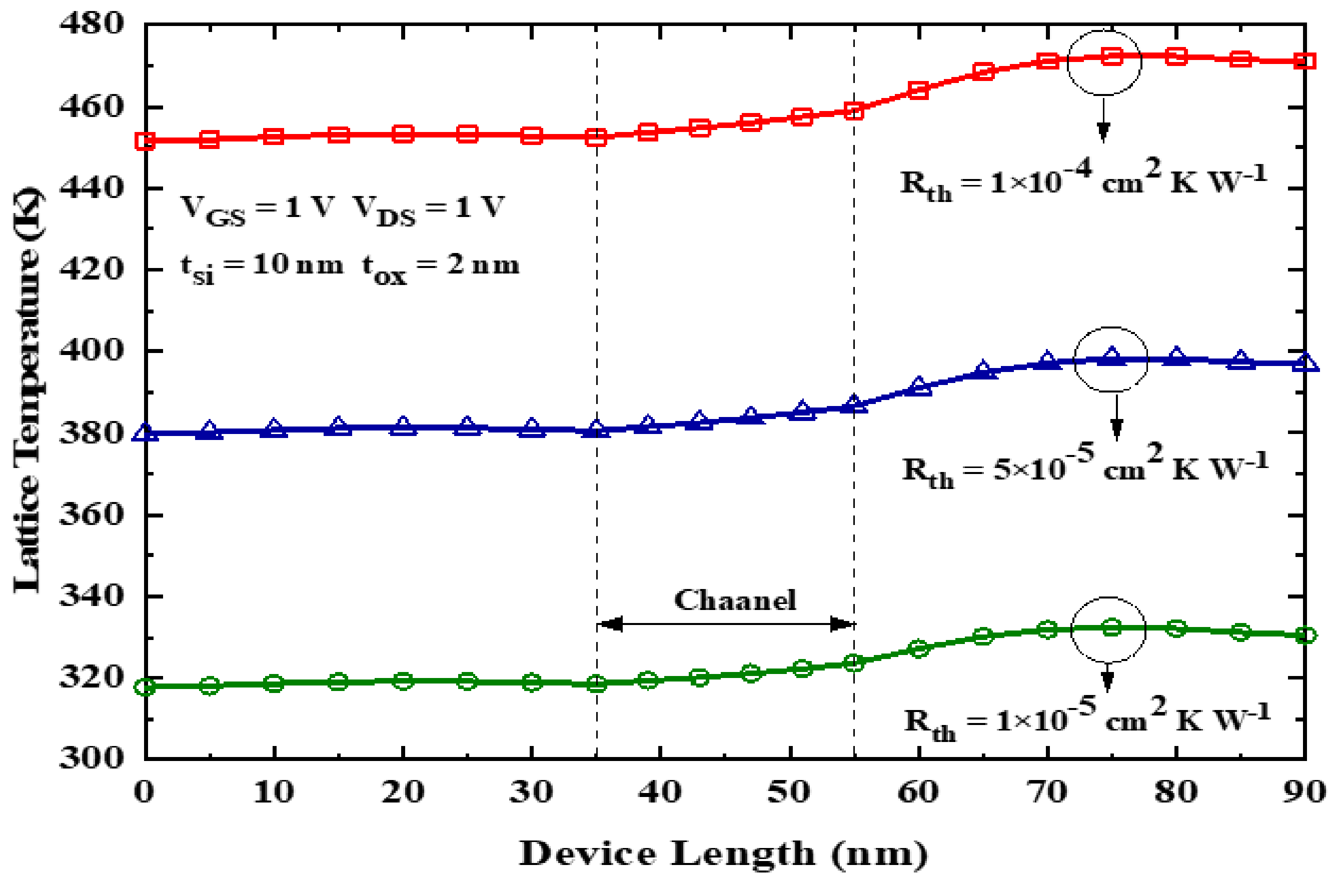


Figure 10

Cutline plot of the variation of lattice temperature (TL) versus device length (nm) for various value of Rth

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

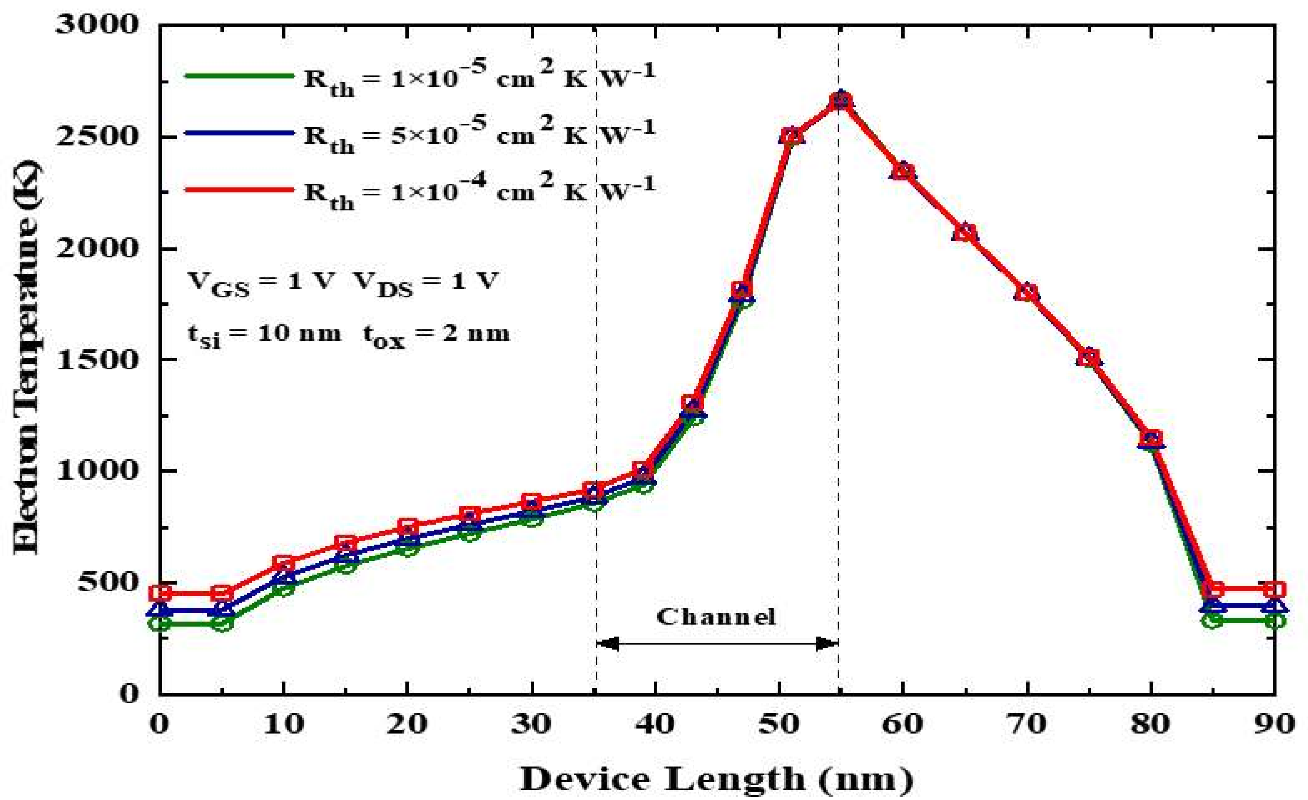


Figure 11

Cutline plot of the variation of electron temperature (Tc) versus device length (nm) for various value of Rth

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

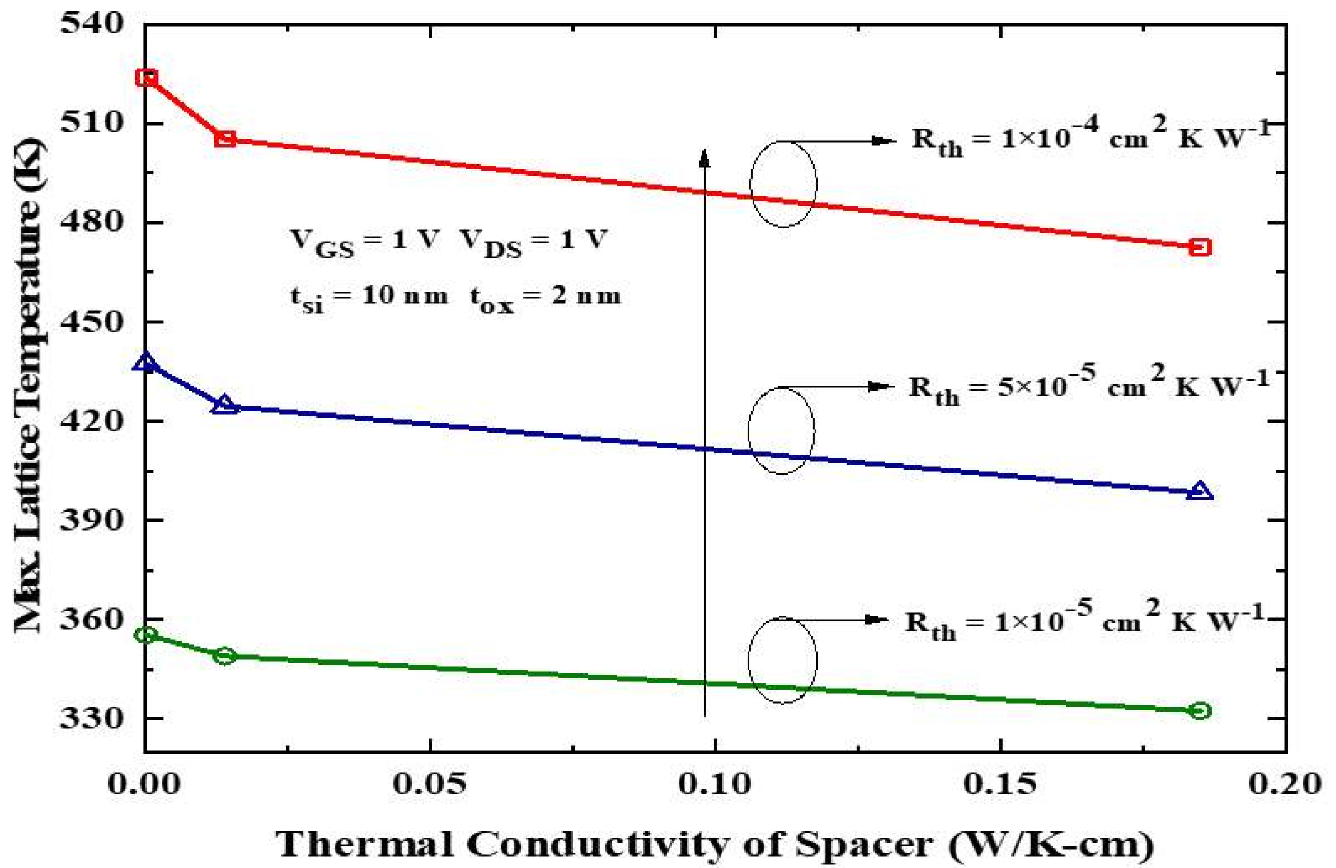


Figure 12

Variation of maximum lattice temperature (TLmax) versus changing thermal conductivity of spacer for various value of Rth

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

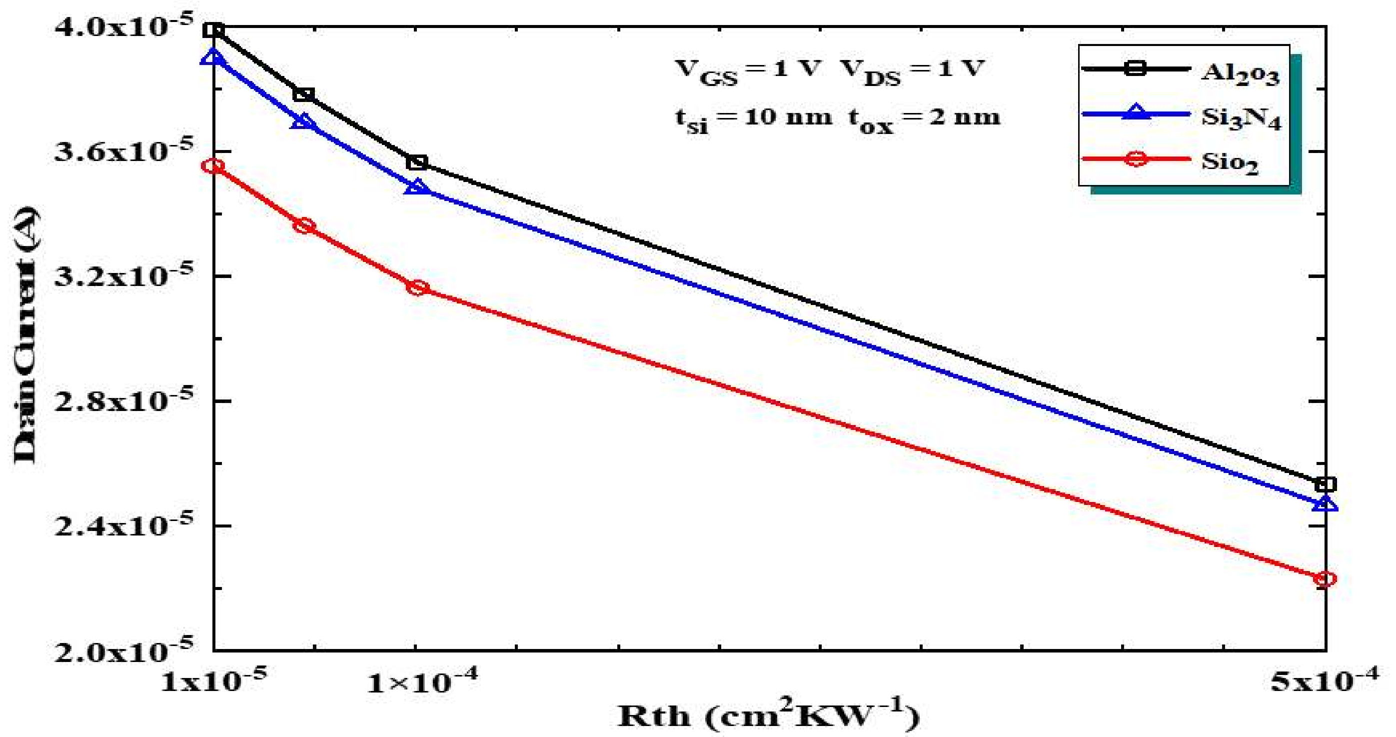


Figure 13

Variation of the drain current versus increasing in Rth for various types of gate oxide

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

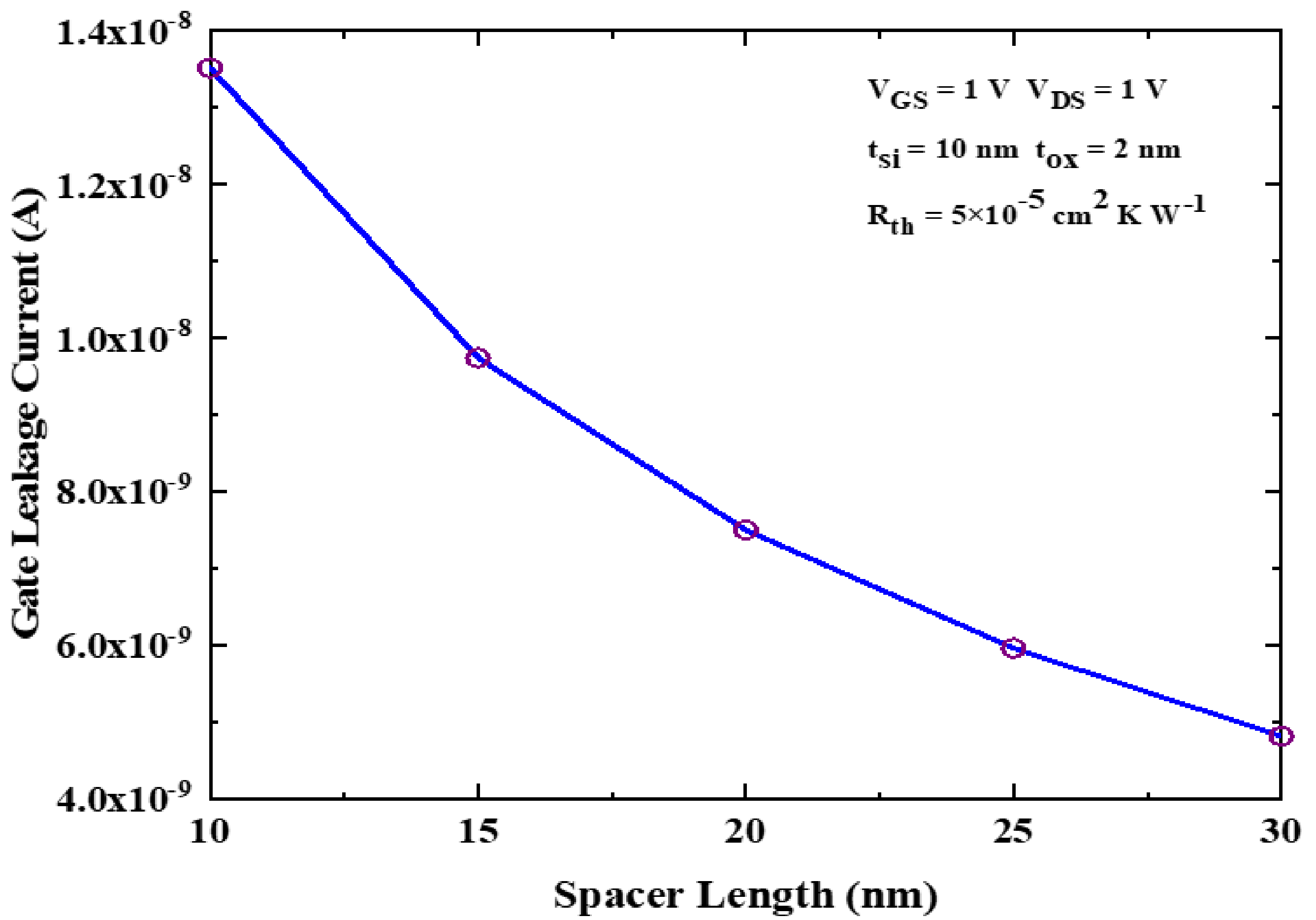


Figure 14

Variation of the gate leakage current versus increasing spacer length (LSP)

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

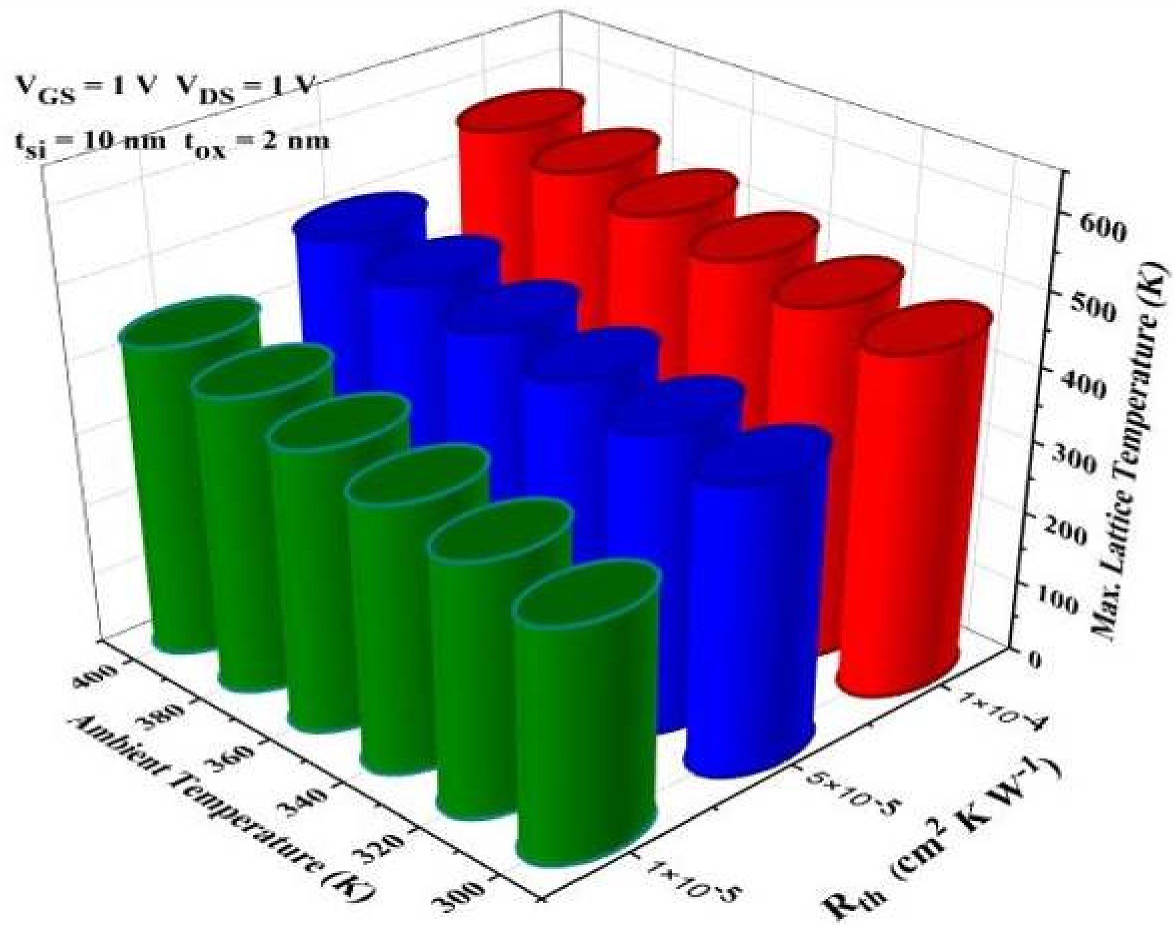


Figure 15

Variation of the maximum lattice temperature (peak of 'Hot Spot') (TLmax) versus increasing ambient temperature (TA) for the various value of Rth

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

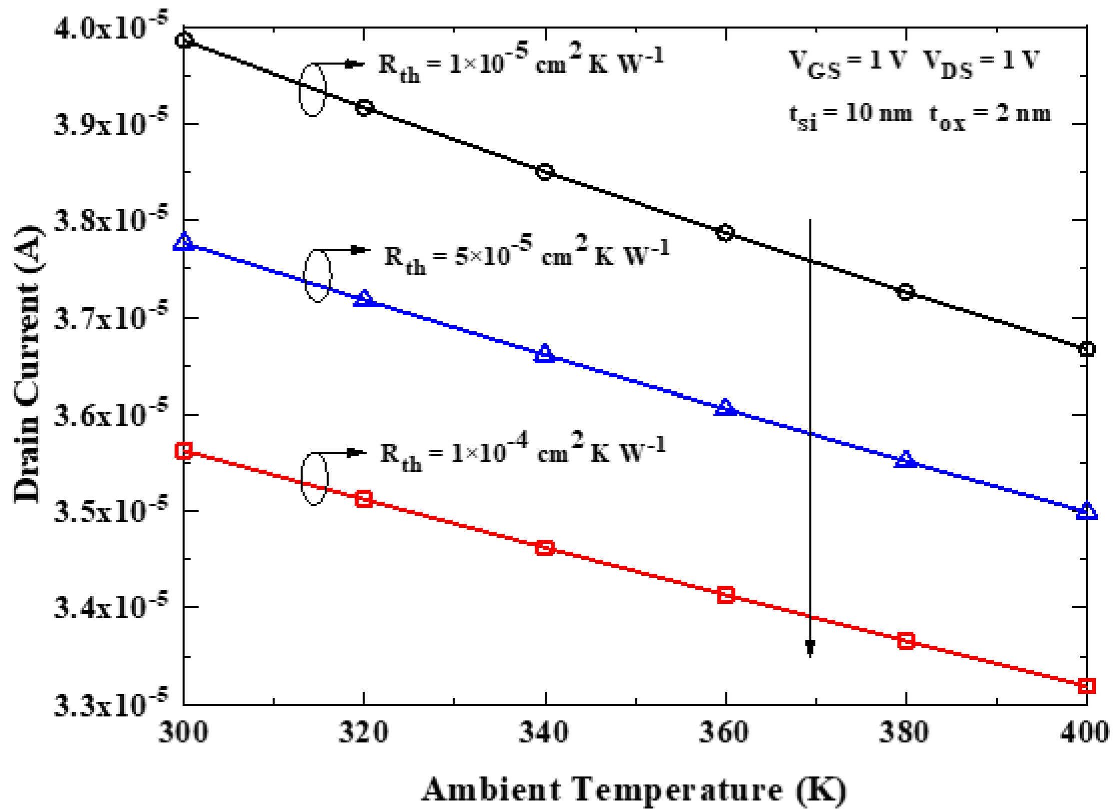


Figure 16

Variation of the drain current versus increasing ambient temperature (TA) for the various value of Rth

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js

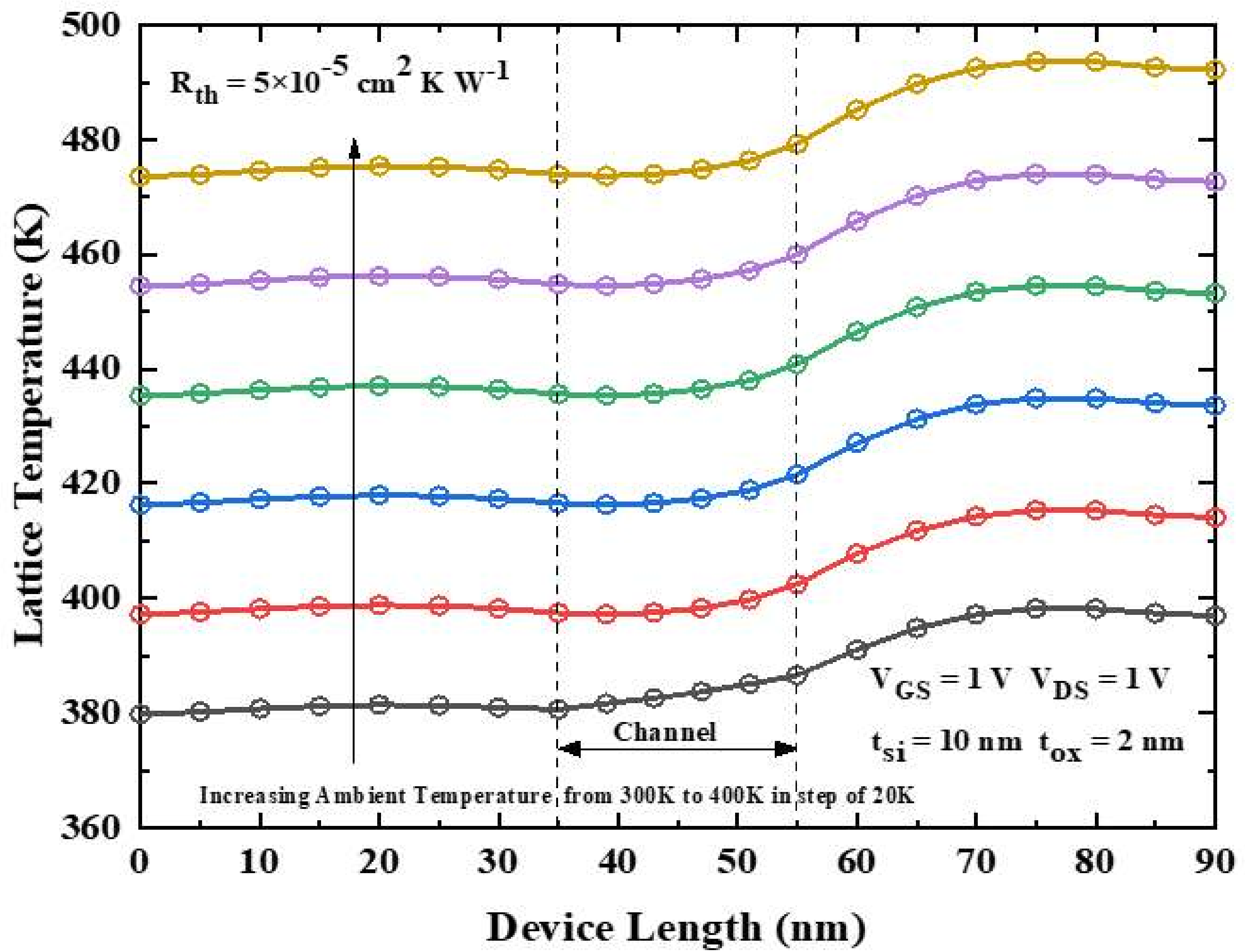


Figure 17

Cutline plot of the variation of lattice temperature (TL) versus device length (nm) for increasing ambient temperature (TA) values

Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js