Investigation and Design of On-Chip Power-Rail ESD Clamp Circuits Without Suffering Latchup-Like Failure During System-Level ESD Test

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***Abstract*—On-chip power-rail electrostatic discharge (ESD) protection circuit designed with active ESD detection function is the key role to significantly improve ESD robustness of CMOS integrated circuits (ICs). Four power-rail ESD clamp circuits with different ESD-transient detection circuits were fabricated in a 0.18-μm CMOS process and tested to compare their system-level ESD susceptibility, which are named as power-rail ESD clamp circuits with typical *RC*-based detection, PMOS feedback, NMOS+PMOS feedback, and cascaded PMOS feedback in this work. During the system-level ESD test, where the ICs in a system have been powered up, the feedback loop used in the power-rail ESD clamp circuits provides the lock function to keep the ESD-clamping NMOS in a "latch-on" state. The latch-on ESD-clamping NMOS, which is often drawn with a larger device dimension to sustain high ESD level, conducts a huge current between the power lines to perform a latchup-like failure after the system-level ESD test. A modified power-rail ESD clamp circuit is proposed to solve this problem. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness, and without suffering the latchup-like failure during the system-level ESD test.**

***Index Terms*—Electromagnetic compatibility (EMC), electrostatic discharge (ESD), ESD protection circuit, latchup, system-level ESD test.**

I. Introduction

ELECTROSTATIC discharge (ESD) protection has been one of the most important reliability issues in CMOS integrated circuit (IC) products. ESD failures caused by thermal breakdown due to high current transient, or dielectric breakdown in gate oxide due to high voltage overstress, often result in immediate malfunction of IC chips. In order to obtain high ESD robustness, CMOS ICs must be designed with on-chip ESD protection circuits at the input/output (I/O) pins and across the power lines [1]. With the reduced breakdown voltage of the thinner gate oxide in advanced deep-submicron CMOS processes, turn-on-efficient ESD protection circuit is required to clamp the overstress across the gate oxide of internal circuits. Since the stored electrostatic charges could be either positive or negative, there are four different ESD-testing modes at input-output (I/O) pins with respect to the grounded $V_{\rm DD}$ or $V_{\rm SS}$ pins [2]. Besides, for a comprehensive ESD verification, two additional pin combinations under ESD test, which are the pin-to-pin ESD stress and the $V_{\rm DD}$-to-$V_{\rm SS}$ ESD stress, are performed to verify the ESD reliability of IC chip [2]. These two additional ESD testing modes often lead to some unexpected ESD current through I/O pins and power lines into the internal circuits and result in ESD damage in the internal circuits [3]. Therefore, effective power-rail ESD clamp circuit between $V_{\rm DD}$ and $V_{\rm SS}$ power lines is necessary for whole-chip ESD protection. The typical on-chip ESD protection design with active power-rail ESD clamp circuit in CMOS ICs is shown in Fig. 1[4]. When the input (or output) pin is zapped under the positive-to-$V_{\rm SS}$ (PS-mode) or negative-to-$V_{\rm DD}$ (ND-mode) ESD stresses, the power-rail ESD clamp circuit can provide a low impedance path between $V_{\rm DD}$ and $V_{\rm SS}$ power lines to efficiently discharge ESD current. To avoid unexpected ESD damages in the internal circuits under pin-to-pin and $V_{\rm DD}$-to-$V_{\rm SS}$ ESD stresses, the power-rail ESD clamp circuit must be designed with high turn-on efficiency and fast turn-on speed.

In the active power-rail ESD clamp circuit, the ESD-transient detection circuit is designed to detect ESD event and sends a control voltage to the gate of ESD-clamping NMOS. Since the ESD-clamping NMOS is turned on by a positive gate voltage rather than by snapback breakdown, the ESD-clamping NMOS can be turned on quickly to discharge ESD current before the internal circuits are damaged. Thus, the effective power-rail ESD clamp circuit is necessary for protecting the internal circuits against ESD damage. Some modified designs on the ESD-transient detection circuits had been reported to enhance the performance of power-rail ESD clamp circuits [5]–[9].

Recently, system-level ESD reliability has attracted more attentions than before in microelectronics products. This tendency results from not only the integration of more functional circuits in a single chip, but also the strict requirement of reliability regulation, such as the system-level ESD test for electromagnetic compatibility (EMC) [10]. During the system-level ESD test, the microelectronics products must sustain the ESD stress of $\pm$8 kV ($\pm$15 kV) under the contact-discharge (air-discharge) test mode to meet the immunity requirement of "level 4." During such a high-energy ESD event, some of ESD-induced overshooting/undershooting pulses may be coupled into the microelectronics products to cause damage or malfunction on the CMOS ICs inside the device under test (DUT) [11], [12].

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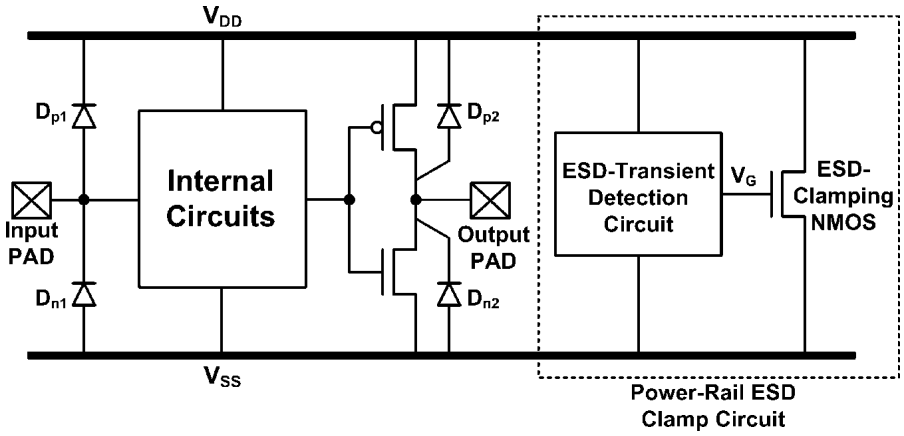


Fig. 1. Typical on-chip ESD protection design with active power-rail ESD clamp circuit.

Some CMOS ICs are very susceptible to system-level ESD stresses, even though they have passed the component-level ESD specifications of human-body model (HBM) of ± 2 kV, machine-model (MM) of ± 200 V, and charged-device model (CDM) of ± 1 kV [13].

In this work, the malfunction or wrong triggering behavior among different on-chip power-rail ESD clamp circuits under system-level ESD test are investigated [14]. Some ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits continually keep the ESD-clamping NMOS in the latch-on state after the system-level ESD test. The latch-on ESD-clamping NMOS between $V_{\rm DD}$ and $V_{\rm SS}$ power lines in the powered-up microelectronic system causes a serious latchup-like failure in CMOS ICs. The system-level ESD gun [15] and the transient-induced latchup (TLU) measurement method [16] are used to evaluate the susceptibility among four different power-rail ESD clamp circuits to system-level ESD test. Furthermore, a modified power-rail ESD clamp circuit is proposed to avoid such latchup-like failure. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD robustness without suffering the latchup-like failure during the system-level ESD test.

II. Power-Rail ESD Clamp Circuits

To provide effective on-chip ESD protection, four different power-rail ESD clamp circuits had been reported [5]–[9], which are redrawn in Fig. 2(a)–(d) with the names of 1) power-rail ESD clamp circuit with typical *RC*-based detection, 2) power-rail ESD clamp circuit with PMOS feedback, 3) power-rail ESD clamp circuit with NMOS+PMOS feedback, and 4) power-rail ESD clamp circuit with cascaded PMOS feedback, in this work. Those power-rail ESD clamp circuits have been designed and fabricated in a 0.18-μm CMOS process to investigate their susceptibility to system-level ESD test.

A. Power-Rail ESD Clamp Circuit With Typical RC-Based Detection

The typical *RC*-based power-rail ESD clamp circuit is illustrated in Fig. 2(a) with a three-stage buffer between the *RC* circuit and the ESD-clamping NMOS [5]. The ESD-clamping NMOS is used to provide a low impedance path between $V_{\rm DD}$ and $V_{\rm SS}$ to discharge ESD current. The ESD-transient detection circuit detects ESD pulses with the rise time of $\sim$10 ns and sends a control voltage to the gate of ESD-clamping NMOS. Under the ESD stress condition, the voltage level at the $V_{\rm Filter}$ node is increased much slower than that on $V_{\rm DD}$ power line, because the *RC* circuit has a time constant in the order of microsecond (μs). Due to the delay of the voltage increase at the $V_{\rm Filter}$ node, the three-stage buffer is powered by the ESD energy and conduct a voltage to the $V_{\rm G}$ node to turn on the ESD-clamping NMOS. The turned-on ESD-clamping NMOS, which provides a low-impedance path between $V_{\rm DD}$ and $V_{\rm SS}$ power lines, clamps the overstress ESD voltage to effectively protect the internal circuits against ESD damage.

The turn-on time of ESD-clamping NMOS during ESD transition can be adjusted by designing the *RC* time constant in the ESD transient detection circuit. The turn-on time is usually designed around $\sim$100 ns to meet the half-energy discharging time of HBM ESD current. Under normal circuit operating conditions, the power-rail ESD clamp circuit must be kept off to avoid power loss from $V_{\rm DD}$ to $V_{\rm SS}$. The rise time of $V_{\rm DD}$ powered up is around $\sim$1 ms or even longer in the most of microelectronics systems. To meet such a timing requirement, the *RC* time constant in the *RC*-based ESD-transient detection circuit is typically designed with 0.1–1 μs to achieve the design constraints.

B. Power-Rail ESD Clamp Circuit With PMOS Feedback

Another design consideration for power-rail ESD clamp circuit is the circuit immunity to false triggering during power-up condition. The power-rail ESD clamp circuit should be turned on when the ESD voltage appears across $V_{\rm DD}$ and $V_{\rm SS}$ power lines, but kept off when the IC is under normal power-on condition. To meet these requirements, the *RC* time constant was usually designed with 0.1–1 μs to achieve the design constraints. However, the large *RC* time constant used in the power-rail ESD clamp circuit may cause false triggering during a fast power-up condition with a rise time of less than 10 μs. The modified power-rail ESD clamp circuit incorporated with PMOS feedback, as shown in Fig. 2(b), was used to mitigate such a mistrigger problem [6]. The transistor MPFB can help to keep the gate voltage of ESD-clamping NMOS below its threshold voltage and further reduce the current drawn during the power-up condition.

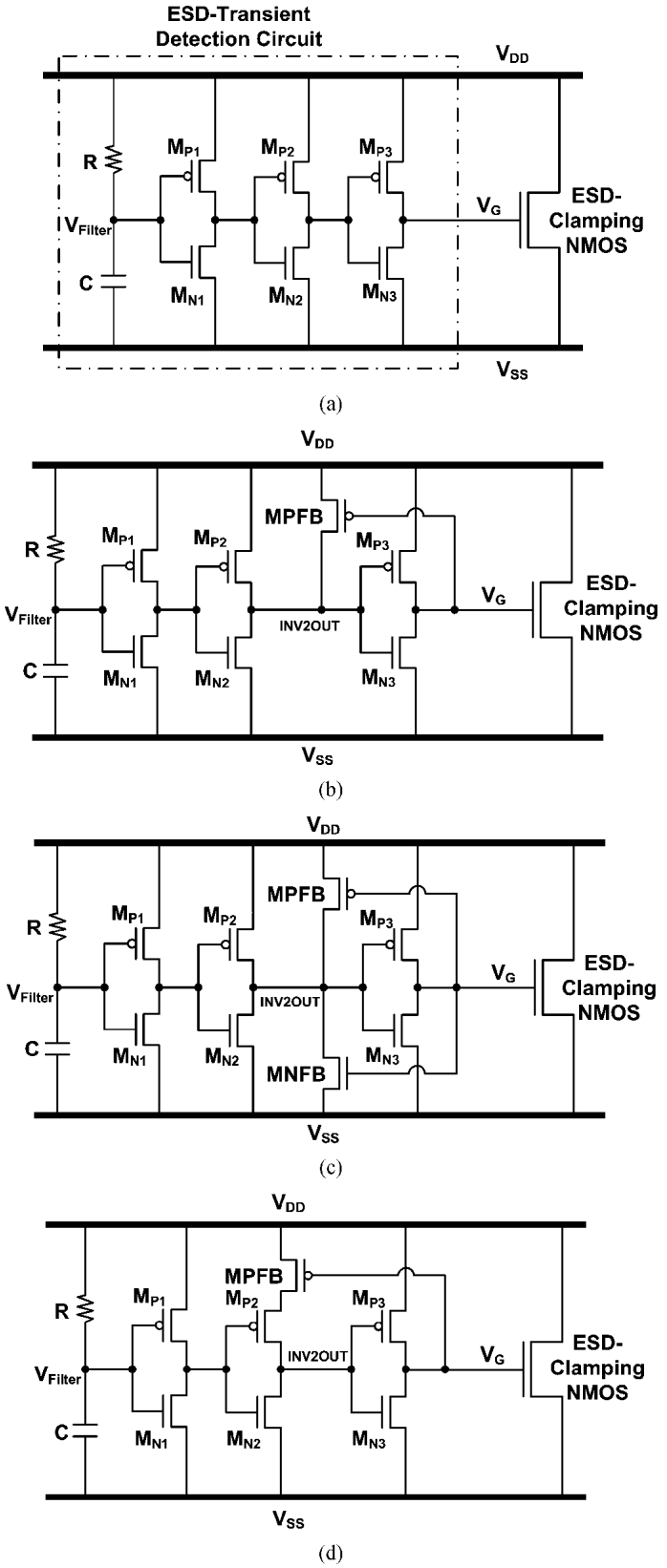


Fig. 2. Four different power-rail ESD clamp circuits designed with (a) typical *RC*-based detection, (b) PMOS feedback, (c) NMOS+PMOS feedback, and (d) cascaded PMOS feedback.

C. Power-Rail ESD Clamp Circuit With NMOS+PMOS Feedback

In the advanced CMOS technology with thinner gate oxide, the power-rail ESD clamp circuit with a large MOS capacitance in the *RC* timer was reported to cause significant standby power consumption due to gate oxide leakage current [7]. Thus, the modified power-rail ESD clamp circuits with small MOS capacitance are desired to combat the gate leakage. It was reported that the power-rail ESD clamp circuit incorporated with a regenerative feedback network can be used to significantly reduce the *RC* time constant, as illustrated in Fig. 2(c) [8].

The transistors MPFB and MNFB provide a feedback loop, which can latch the ESD-clamping NMOS in the conductive state during ESD-stress condition. When a fast positive going ESD transient across the power rails, the MNFB can further pull the potential of INV2OUT node towards ground to latch the ESD-clamping NMOS in the conductive state until the voltage on $V_{\rm DD}$ drops below the threshold voltage of ESD-clamping NMOS. With this feedback loop in the power-rail ESD clamp circuit, the dynamic currents of $\rm M_{P2}$, $\rm M_{N2}$, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. After the timing out of the *RC* time constant in ESD transient detection circuit, the transistor $\rm M_{P2}$ begins to conduct and increase the potential of INVOUT2 node. The settling potential of INVOUT2 node is set by the current balance between $\rm M_{P2}$ and MNFB. Thus, the device ratios of $\rm M_{P2}$ and MNFB in the power-rail ESD clamp circuit with NMOS+PMOS feedback should be appropriately selected.

D. Power-Rail ESD Clamp Circuit With Cascaded PMOS Feedback

Another *RC*-based power-rail ESD clamp circuit with cascaded PMOS feedback has been proposed to reduce the *RC* time constant and to solve false trigger issue during fast power-up constraints, as shown in Fig. 2(d) [9]. The PMOS transistor MPFB is connected to form the cascaded feedback loop, which is a dynamic feedback design.

During the ESD-stress condition, the transistor MPFB was turned off and the voltage on the INV2OUT node can be remained in a low state. Thus, the turn-on time of the ESD-clamping NMOS can be longer than that of the typical *RC*-based power-rail ESD clamp circuit. If the ESD-clamping NMOS is mistriggered during fast power-up condition or by an overvoltage under normal operating conditions, the voltage on the INV2OUT node can be charged up toward $V_{\rm DD}$ by the subthreshold current of MPFB. Therefore, the ESD-clamping NMOS will not stay at latch-on state and turn itself off after the fast power-up condition. Compared with the feedback designs with direct PMOS feedback in Fig. 2(b), the power-rail ESD clamp circuit with cascaded PMOS feedback has the advantage of capacitance reduction.

E. Realization in Silicon Chip

For the four power-rail ESD clamp circuits in this work, the ESD-clamping NMOS is designed to turn on under the ESD-stress condition to efficiently discharge the ESD current between $V_{\rm DD}$ and $V_{\rm SS}$ power lines. The turn-on time of the ESD-clamping NMOS is designed to meet the half-energy discharging time of HBM ESD event. In the normal operating condition and $V_{\rm DD}$ power-up condition, the ESD-clamping NMOS is designed to keep off to avoid power loss or false triggering. The four power-rail ESD clamp circuits in this

TABLE I
DEVICE DIMENSIONS (W/L IN μm) OF THE POWER-RAIL ESD CLAMP CIRCUIT WITH TYPICAL *RC*-BASED DETECTION

R	50kΩ
C	2pF
M_{P1}	12/0.18
M_{N1}	4/0.18
M_{P2}	24/0.18
M_{N2}	8/0.18
M_{P3}	60/0.18
M_{N3}	16/0.18
ESD-Clamping NMOS	2000/0.18

TABLE II
DEVICE DIMENSIONS (W/L IN μm) OF THE POWER-RAIL ESD CLAMP CIRCUIT WITH PMOS FEEDBACK

R	50kΩ
C	2pF
M_{P1}	12/0.18
M_{N1}	4/0.18
M_{P2}	24/0.18
M_{N2}	8/0.18
M_{P3}	60/0.18
M_{N3}	16/0.18
MPFB	24/0.18
ESD-Clamping NMOS	2000/0.18

TABLE III
DEVICE DIMENSIONS (W/L IN μm) OF THE POWER-RAIL ESD CLAMP CIRCUIT WITH NMOS+PMOS FEEDBACK

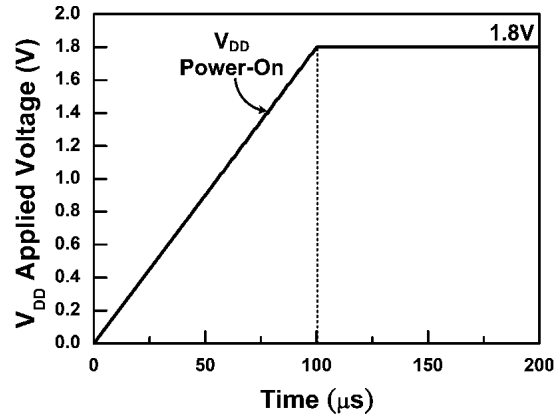
R	50kΩ
C	2pF
M_{P1}	12/0.18
M_{N1}	4/0.18
M_{P2}	24/0.18
M_{N2}	8/0.18
M_{P3}	90/0.18
M_{N3}	16/0.18
MPFB	36/0.18
MNFB	12/0.18
ESD-Clamping NMOS	2000/0.18

work are designed with such design concepts to evaluate their susceptibility to system-level ESD tests. The device dimensions of four different power-rail ESD clamp circuits realized in a given 0.18-μm CMOS process are summarized in Tables I–IV.

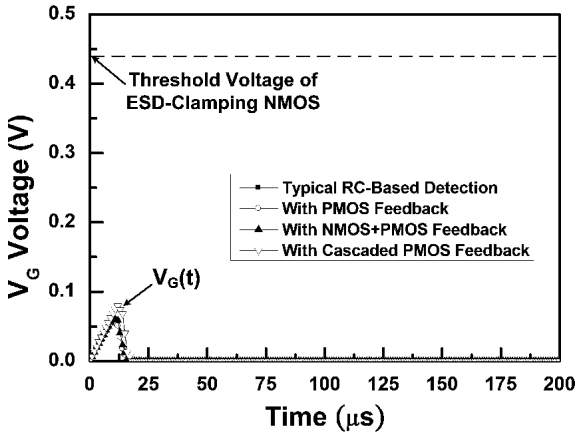
To verify such design, some simulations are provided in the following. In Fig. 3(a), a $V_{\rm DD}$ power-on voltage waveform with a rise time of 0.1 ms and a voltage height of 1.8 V is applied to the $V_{\rm DD}$ line of the power-rail ESD clamp circuits. During such a $V_{\rm DD}$ power-on condition, among the four different power-rail ESD clamp circuits, the voltage waveforms on the node $V_{\rm G}$ are shown in Fig. 3(b), where the $V_{\rm G}$ peak voltage during the power-on transition are all below the threshold voltage ($\sim$0.44 V) of the ESD-clamping NMOS. With a very small

TABLE IV
DEVICE DIMENSIONS (W/L IN μm) OF THE POWER-RAIL ESD CLAMP CIRCUIT WITH CASCADED PMOS FEEDBACK

R	50kΩ
C	2pF
M_{P1}	12/0.18
M_{N1}	4/0.18
M_{P2}	4/0.18
M_{N2}	8/0.18
M_{P3}	60/0.18
M_{N3}	16/0.18
MPFB	200/0.18
ESD-Clamping NMOS	2000/0.18



(a)



(b)

Fig. 3. HSPICE simulated voltage waveforms among the four different power-rail ESD clamp circuits under the $V_{\rm DD}$ power-on condition. (a) A slow ramp voltage waveform with rise time of 0.1 ms is used to simulate the rising edge of the $V_{\rm DD}$ power-on voltage. (b) The simulated voltage waveforms on the node $V_{\rm G}$ when the $V_{\rm DD}$ power-on voltage is applied to $V_{\rm DD}$.

$V_{\rm G}$ voltage in Fig. 3(b), the ESD-clamping NMOS in the four different power-rail ESD clamp circuits was expected to be always kept off when the IC is in normal operating conditions.

In Fig. 4(a), a fast ramp voltage with a rise time of 10 ns is used to simulate the rising edge of HBM ESD pulse. The pulse height of the fast ramp voltage set as 5 V is used to monitor the voltage on the node $V_{\rm G}$ before the drain breakdown of ESD-clamping NMOS. As shown in Fig. 4(b), among the four different power-rail ESD clamp circuits, the voltage waveforms on the node $V_{\rm G}$ are simultaneously increased when the fast ramp

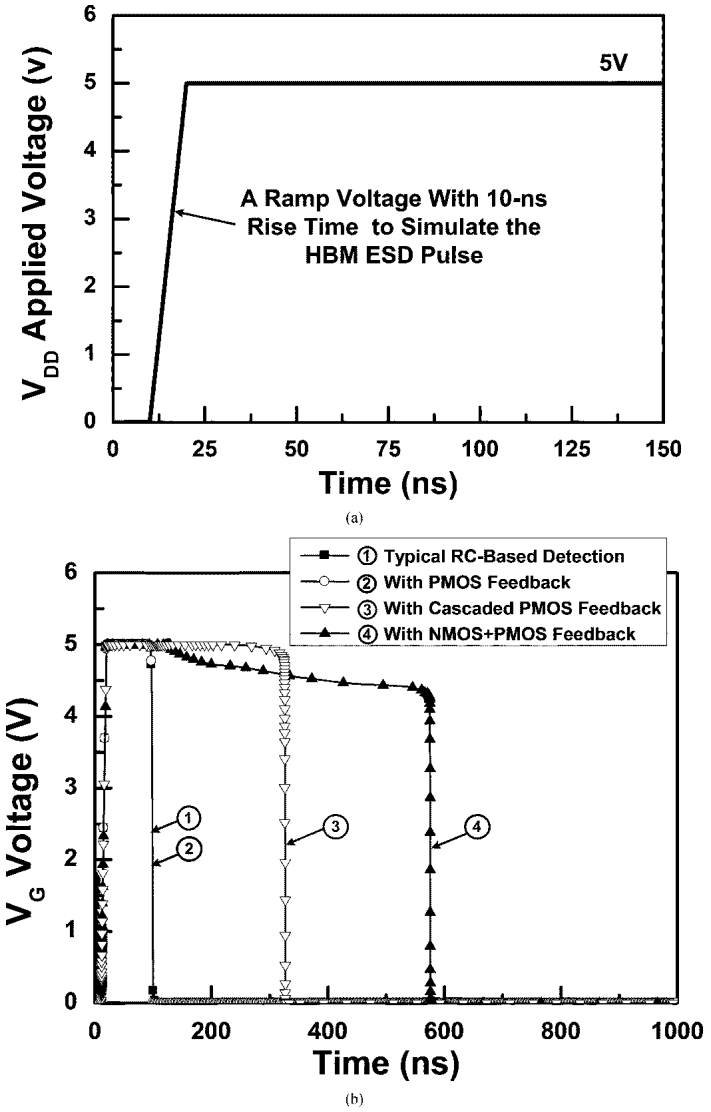


Fig. 4. HSPICE simulated voltage waveforms among the four different power-rail ESD clamp circuits under HBM ESD stress condition. (a) A fast ramp voltage waveform with rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse. (b) The simulated voltage waveforms on the node $V_{\rm G}$ when the fast ramp voltage is applied to $V_{\rm DD}$.

voltage is applied to $V_{\rm DD}$, whereas the $V_{\rm SS}$ is grounded. The four power-rail ESD clamp circuits are designed to provide a low impedance path between $V_{\rm DD}$ and $V_{\rm SS}$ power lines to efficiently discharge ESD current under ESD stress conditions. Combing with feedback circuit structure in the ESD-transient detection circuits, the turn-on time of the ESD-clamping NMOS can be increased by static or dynamic latches [8], [9]. For the power-rail ESD clamp circuits with NMOS+PMOS feedback and cascaded PMOS feedback, the turn-on time of the ESD-clamping NMOS can be longer than that of power-rail ESD clamp circuits with typical *RC*-based detection and PMOS feedback. The turn-on time of power-rail ESD clamp circuits with NMOS+PMOS feedback or cascaded PMOS feedback can be designed around 100 ns, if the *RC* time constant in the corresponding ESD-transient detection circuit is further reduced. To simply the comparison for transient-induced latchup-like failure in this work, the *RC* values in the ESD-transient detection circuits among four power-rail ESD clamp circuits are set the same of $R = 50$ kΩ and $C = 2$ pF in silicon fabrication.

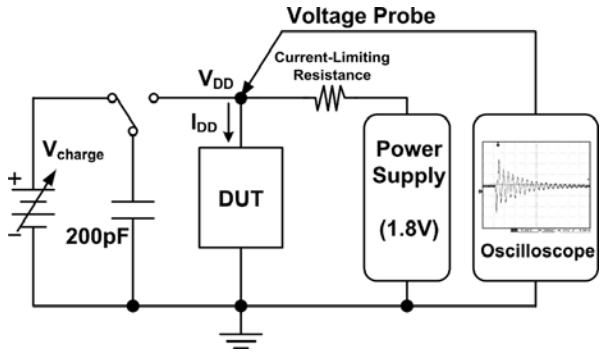


Fig. 5. Measurement setup for transient-induced latchup (TLU) [16].

III. Transient-Induced Latchup (TLU) Test

A. Measurement Setup

Transient-induced latchup (TLU) test has been used to investigate the susceptibility of DUT to the noise transient or glitch on the power lines under normal circuit operating condition. The component-level TLU measurement setup with bipolar trigger voltage can accurately simulate the ESD-induced noises on the power lines of CMOS ICs under system-level ESD test [16]. The measurement setup for TLU test is shown in Fig. 5. The charging voltage $V_{\rm Charge}$ has two different polarities, which are positive ($V_{\rm Charge} > 0$) or negative ($V_{\rm Charge} < 0$). The positive (negative) $V_{\rm Charge}$ can generate the positive-going (negative-going) bipolar trigger noises on the power pins of DUT. A 200-pF capacitor used in the machine model (MM) ESD test [17] is employed as the charging capacitor. The power-rail ESD clamp circuits shown in Fig. 2(a)–(d) are placed as DUT. The supply voltage of 1.8 V is used as $V_{\rm DD}$ and the noise trigger source is directly connected to DUT through the relay in the measurement setup. The $I_{\rm DD}$ current waveform is measured by a separated current probe. The current-limiting resistance is used to avoid electrical-over-stress (EOS) damage in DUT under a high-current latch-up state. The voltage and current waveforms on DUT (at $V_{\rm DD}$ node) after TLU test are monitored by the oscilloscope.

B. Measurement Results

With the TLU measurement setup in Fig. 5, the $V_{\rm DD}$ and $I_{\rm DD}$ transient responses can be recorded by the oscilloscope, which can clearly indicate whether TLU occurs ($I_{\rm DD}$ significantly increases) or not. Fig. 6(a) and (b) show the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under the stresses with $V_{\rm Charge}$ of -4 V and $+12$ V, respectively. After the TLU test with an initial $V_{\rm Charge}$ of -4 V, the latchup-like failure occurs in this power-rail ESD clamp circuit, because $I_{\rm DD}$ significantly increases and $V_{\rm DD}$ is pulled down, as shown in Fig. 6(a). After the TLU test with an initial $V_{\rm Charge}$ of $+12$ V, latchup-like failure occurs in Fig. 6(b). All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this part [18]. This implies that the feedback loop in the ESD-transient detection circuit is locked after TLU test and continually keeps the ESD-clamping

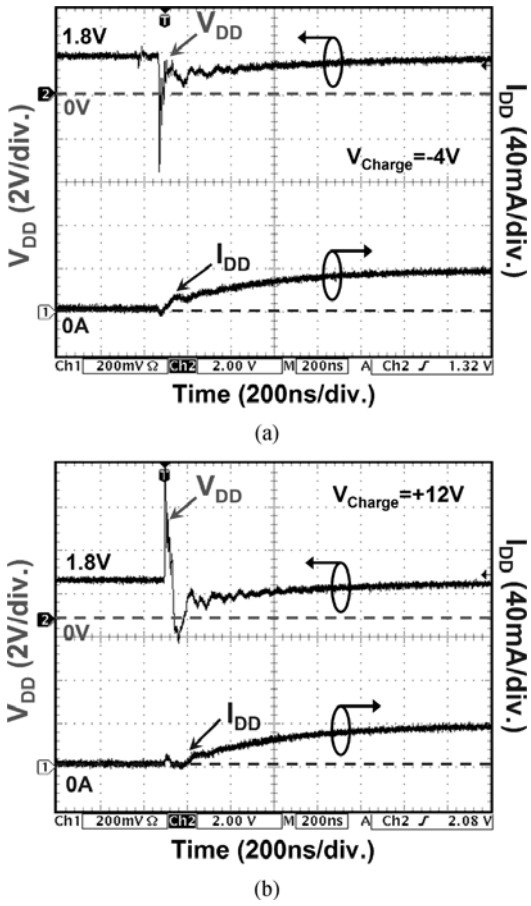


Fig. 6. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under TLU test with $V_{\rm Charge}$ of (a) -4 V and (b) $+12$ V.

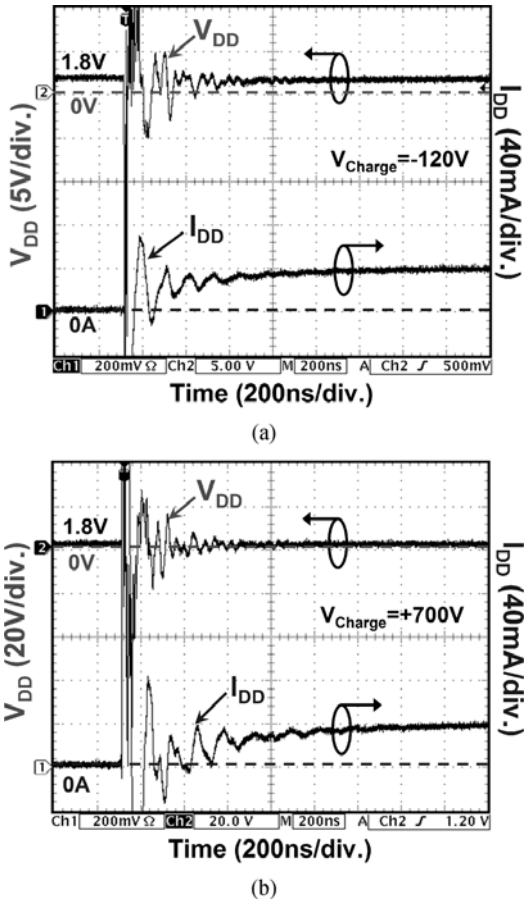


Fig. 7. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback under TLU test with $V_{\rm Charge}$ of (a) -120 V and (b) $+700$ V.

NMOS in the latch-on state. From the observed voltage and current waveforms, large $I_{\rm DD}$ current is caused by the latch-on state of ESD-clamping NMOS after TLU test.

For the power-rail ESD clamp circuit with cascaded PMOS feedback, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses are shown in Fig. 7(a) and (b) under the TLU test with the initial $V_{\rm Charge}$ of -120 V and $+700$ V, respectively. The similar latchup-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of ESD-clamping NMOS after TLU test. The TLU levels (the minimum voltage of $V_{\rm Charge}$ to induce the latchup-like failure on $V_{\rm DD}$) among the aforementioned four different power-rail ESD clamp circuits are listed in Table V.

TABLE V
COMPARISON ON TLU LEVELS AMONG FOUR DIFFERENT POWER-RAIL ESD CLAMP CIRCUITS UNDER TLU TEST

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
Typical RC-Based Detection	Over +1kV	Over -1kV
With PMOS Feedback	Over +1kV	Over -1kV
With NMOS+PMOS Feedback	+12V	-4V
With Cascaded PMOS Feedback	+700V	-120V

IV. SYSTEM-LEVEL ESD TEST

A. Measurement Setup

In the standard of IEC 61000–4-2 [10], two test modes have been specified, which are air-discharge test mode and contact-discharge test mode. Fig. 8 shows the standard measurement setup of the system-level ESD test with indirect contact-discharge test mode [10]. The measurement setup of system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the equipment under test (EUT) from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from the ESD will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by such high ESD-coupled energy.

With such a standard measurement setup, the susceptibility of different power-rail ESD clamp circuits against the system-level ESD stresses can be evaluated. The stand alone power-rail ESD clamp circuit in IC package is powered up with power supply of 1.8 V. Before any ESD zapping, the initial $V_{\rm DD}$ voltage level

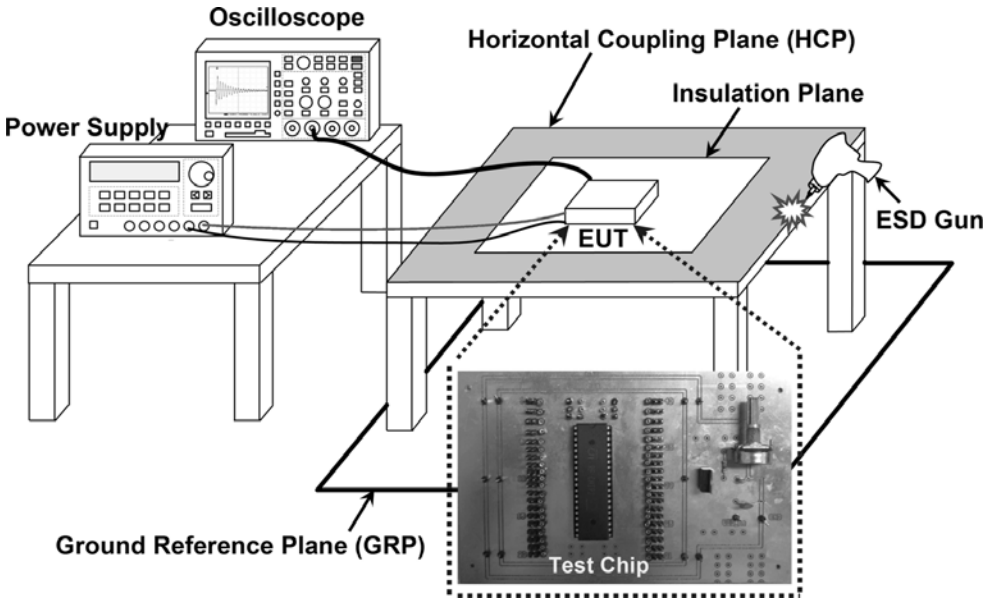


Fig. 8. Measurement setup for system-level ESD test with indirect contact-discharge test mode [10] to evaluate the susceptibility of power-rail ESD clamp circuits.

on the IC is measured to make sure the correct bias of 1.8 V. After every ESD zapping, the voltage level on $V_{\rm DD}$ node of IC is measured again to watch whether latchup-like failure occurs after the system-level ESD test, or not. If the latchup-like failure occurs, the potential on $V_{\rm DD}$ node will be pulled down to a much lower level due to the latch-on state of ESD-clamping NMOS in the power-rail ESD clamp circuits, and $I_{\rm DD}$ will be significantly increased.

B. Measurement Results

With the system-level ESD measurement setup in Fig. 8, the $V_{\rm DD}$ and $I_{\rm DD}$ transient responses can be recorded by the oscilloscope, which can clearly indicate whether the latchup-like failure occurs or not. Fig. 9(a) and (b) show the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses on the power-rail ESD clamp circuit with typical *RC*-based detection when ESD gun with ESD voltage of -10 kV and $+10$ kV zapping on the HCP, respectively. After the system-level ESD test with an ESD voltage of -10 kV, latchup-like failure is not initiated in this power-rail ESD clamp circuit, because $I_{\rm DD}$ is still kept at zero, as shown in Fig. 9(a). After the system-level ESD test with an ESD voltage of $+10$ kV, latchup-like failure is not observed in Fig. 9(b). Under system-level ESD test with ESD voltage of -10 kV and $+10$ kV, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms on the power-rail ESD clamp circuit with PMOS feedback are shown in Fig. 10(a) and (b), respectively. Under system-level ESD test with an ESD voltage of -10 kV ($+10$ kV), $V_{\rm DD}$ acts with the intended bipolar trigger. Meanwhile, latchup-like failure does not occur because $I_{\rm DD}$ is not increased, as shown in Fig. 10(a) (Fig. 10(b)). For the power-rail ESD clamp circuits with typical *RC*-based detection or PMOS feedback, latchup-like failure does not occur even though the ESD voltage is as high as -10 kV or $+10$ kV in the system-level ESD test.

Fig. 11(a) and (b) show the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses on the power-rail ESD clamp circuit with NMOS+PMOS feedback under the system-level ESD test with

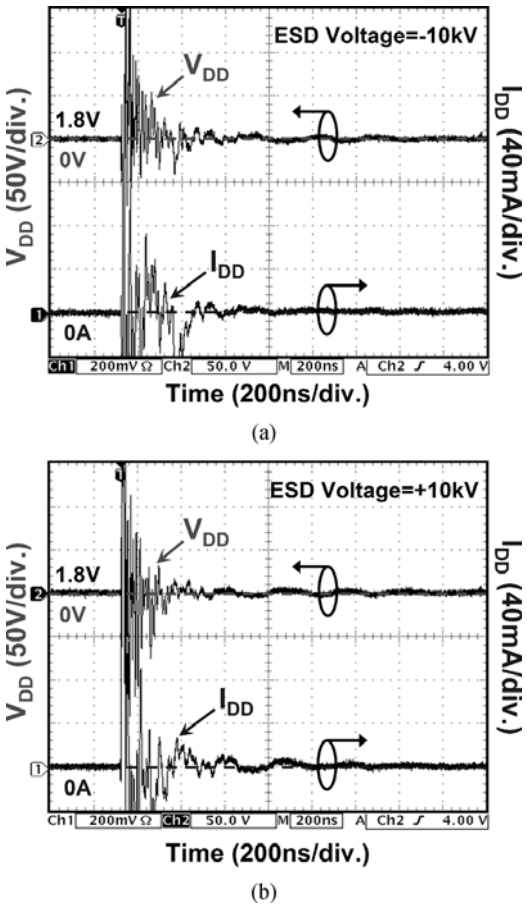


Fig. 9. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the power-rail ESD clamp circuit with typical *RC*-based detection under system-level ESD test with ESD voltage of (a) -10 kV and (b) $+10$ kV.

ESD voltages of -0.2 kV and $+2.5$ kV, respectively. After the system-level ESD test with an ESD voltage of -0.2 kV, latchup-like failure can be initiated in this power-rail ESD clamp circuit, because $I_{\rm DD}$ is significantly increased and $V_{\rm DD}$ is pulled down as shown in Fig. 11(a). After the system-level

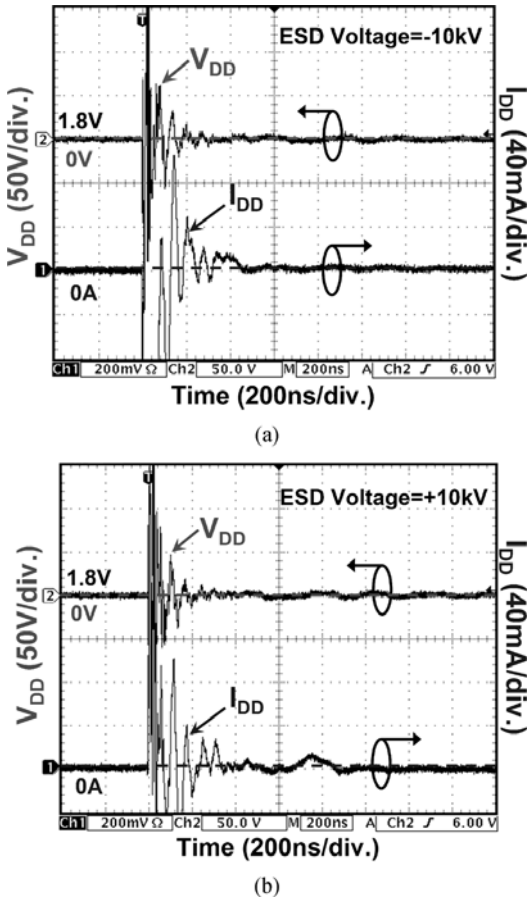


Fig. 10. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the power-rail ESD clamp circuit with PMOS feedback under system-level ESD test with ESD voltage of (a) -10 kV and (b) $+10$ kV.

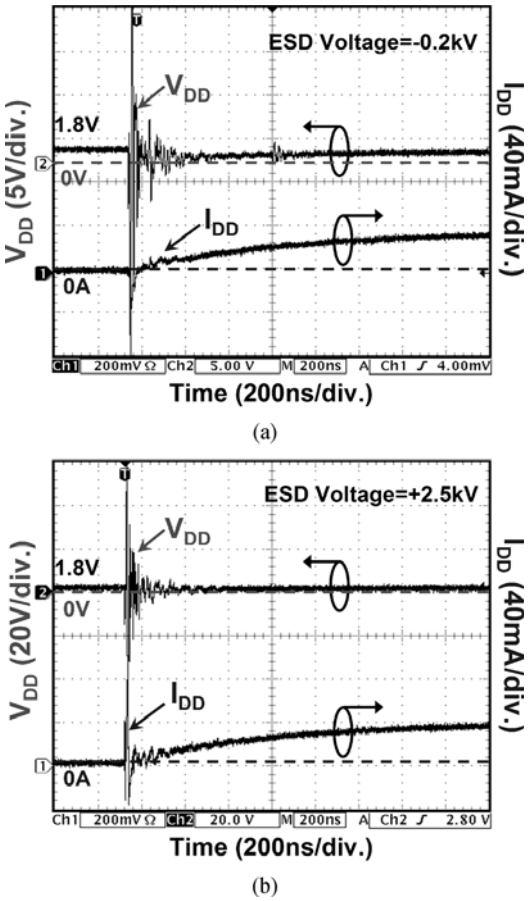


Fig. 11. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under system-level ESD test with ESD voltage of (a) -0.2 kV and (b) $+2.5$ kV.

ESD test with an ESD voltage of $+2.5$ kV, the latchup-like failure can be also found in Fig. 11(b).

For the power-rail ESD clamp circuit with cascaded PMOS feedback, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient responses are shown in Fig. 12(a) and (b) under the system-level ESD test with ESD voltages of -1 kV and $+10$ kV, respectively. The similar latchup-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of ESD-clamping NMOS under the system-level ESD test with an ESD voltage of -1 kV, as shown in Fig. 12(a).

The susceptibility among the aforementioned four different power-rail ESD clamp circuits against system-level ESD test are listed in Table VI. The power-rail ESD clamp circuits with NMOS+PMOS feedback or with cascaded PMOS feedback have lower ESD voltages to cause latchup-like failure after system-level ESD test. Such measured results by ESD gun test are consistent with those of TLU shown in Table V. From the experimental results, the power-rail ESD clamp circuit designed with NMOS+PMOS feedback is highly sensitive to transient-induced latchup-like failure. The typical power-rail ESD clamp circuits with *RC*-based detection and with PMOS feedback are free to such a latchup-like failure.

The failure location after system-level ESD test has been inspected, as shown in Fig. 13. The failure location is located at the $V_{\rm DD}$ metal line from the $V_{\rm DD}$ pad to the power-rail ESD clamp circuit, which was drawn with a metal width of 30 μm in the test chip.

V. Modified Power-Rail ESD Clamp Circuit

From the above measurement results, some ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits continually keep the ESD-clamping NMOS in the latch-on state after the system-level ESD test. The latch-on ESD-clamping NMOS between $V_{\rm DD}$ and $V_{\rm SS}$ power lines in the powered-up microelectronic system causes a serious latchup-like failure in CMOS ICs. In order to meet electromagnetic compatibility regulation under system-level ESD test, modified power-rail ESD clamp circuits without suffering the latchup-like failure are highly desirable. It has been reported that the power-rail ESD clamp circuit with conventional rise time detector and a separated on-time control circuit can reduce the *RC* area and improve the immunity to false triggering [19]. The separated on-time control circuit can keep the ESD-clamping NMOS turned on for the expected maximum duration of an ESD event. From the measured results under the system-level ESD test, two ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits had been found suffering latchup-like failure. In order to avoid such a latchup-like failure, it could be useful to reduce the latch strength of the feedback loop in the ESD-transient detection circuit by suitable device dimension sizing. In this work, another modified power-rail ESD clamp circuit is proposed to avoid such latchup-like failure. The proposed power-rail ESD clamp circuit can provide high enough chip-level ESD

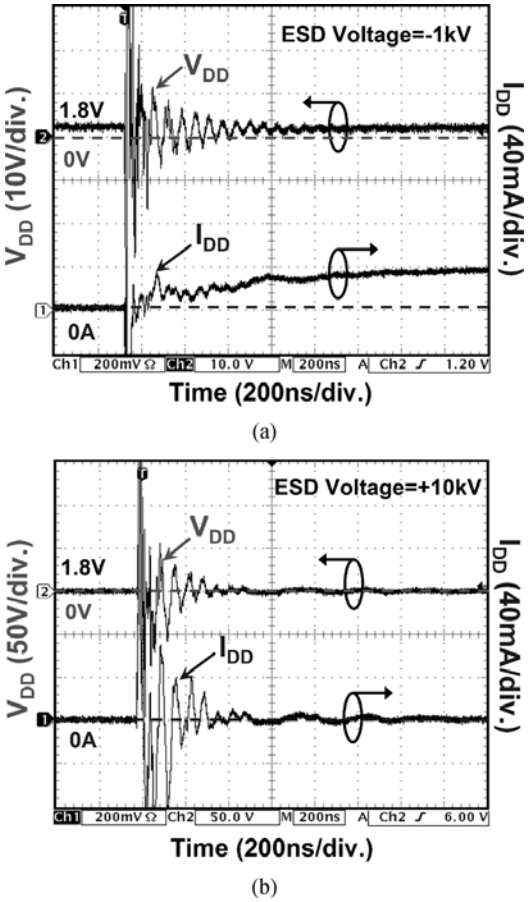


Fig. 12. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback under system-level ESD test with ESD voltage of (a) -1 kV and (b) $+10$ kV.

TABLE VI
COMPARISON ON THE SUSCEPTIBILITY AMONG FOUR DIFFERENT POWER-RAIL ESD CLAMP CIRCUITS UNDER SYSTEM-LEVEL ESD TEST

Power-Rail ESD Clamp Circuits	Positive ESD Stress	Negative ESD Stress
Typical RC-Based Detection	Over +10kV	Over -10kV
With PMOS Feedback	Over +10kV	Over -10kV
With NMOS+PMOS Feedback	+2.5kV	-0.2kV
With Cascaded PMOS Feedback	Over +10kV	-1kV

robustness without suffering the latchup-like failure during the system-level ESD test.

A. Power-Rail ESD Clamp Circuit With NMOS Reset Function

Fig. 14 shows the proposed power-rail ESD clamp circuit with NMOS reset function to overcome the latchup-like failure, which is realized with NMOS+PMOS feedback and an additional NMOS device ($\rm M_{NR1}$) to provide the reset function after system-level ESD stresses. When the ESD-clamping NMOS is latched-on, the NMOS device ($\rm M_{NR1}$) will be turned on after

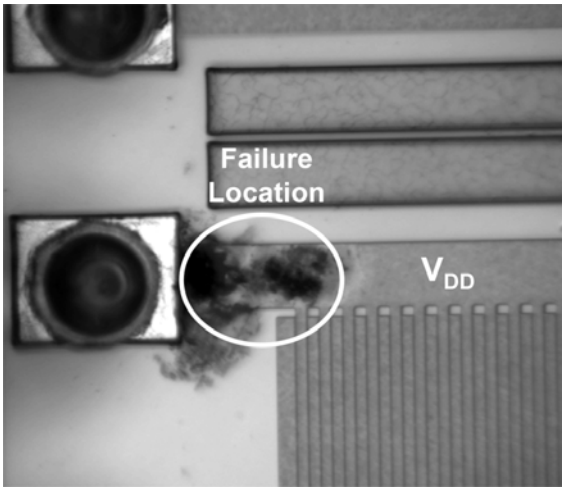


Fig. 13. Failure location of power-rail ESD clamp circuit after system-level ESD stress.

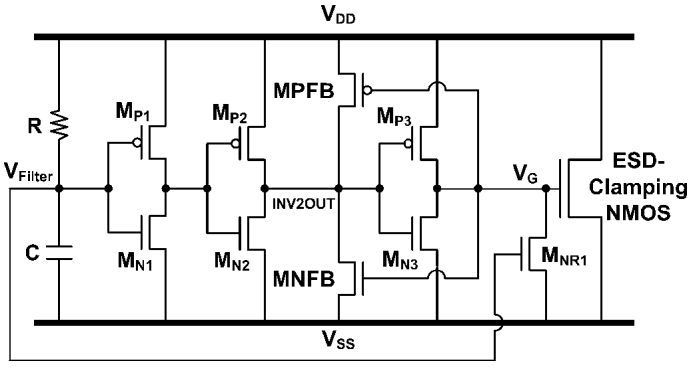


Fig. 14. Proposed power-rail ESD clamp circuit with NMOS reset function to overcome latchup-like failure.

the time out of *RC* time constant. Thus, the gate potential of the ESD-clamping NMOS will be pulled down toward 0 V to release the "latch-on" state.

B. Simulation Results

The NMOS device $\rm M_{NR1}$ is used to release the "latch-on" state of the ESD-clamping NMOS. After system-level ESD tests, the potential on the $V_{\rm Filter}$ node is charged toward the voltage potential on $V_{\rm DD}$. When the potential at the $V_{\rm Filter}$ node is greater than the threshold voltage of $\rm M_{NR1}$, $\rm M_{NR1}$ can be turned on to pull down any potential at $V_{\rm G}$. Thus, the "latch-on" state of the ESD-clamping NMOS caused by system-level ESD test can be released. With the NMOS+PMOS feedback in the power-rail ESD clamp circuit, the dynamic currents of $\rm M_{P2}$, $\rm M_{N2}$, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. The dimensions of $\rm M_{NR1}$ and $\rm M_{P3}$ should be appropriately designed with consideration of the NMOS+PMOS feedback loop.

Fig. 15 shows the simulated transient responses on $V_{\rm G}$ voltages of the proposed power-rail ESD clamp circuit and the original power-rail ESD clamp circuit with NMOS+PMOS feedback, respectively. The voltage on $V_{\rm DD}$ is 1.8 V and the initial voltage on $V_{\rm G}$ is set to 1.8 V to simulate the "latch-on" state of the ESD-clamping NMOS after system-level ESD tests. With an initial voltage of 1.8 V, the $V_{\rm G}$ voltage of the power-rail

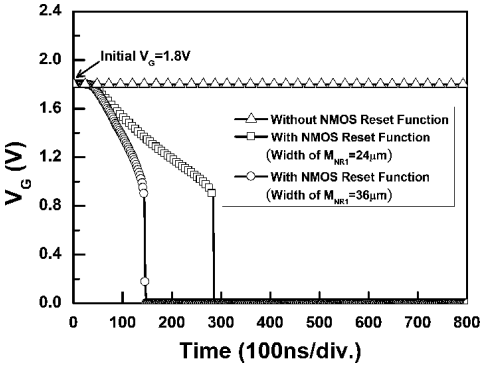


Fig. 15. Simulated $V_{\rm G}$ voltage waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function and power-rail ESD clamp circuit with NMOS+PMOS feedback with an initial $V_{\rm G}$ voltage of 1.8 V.

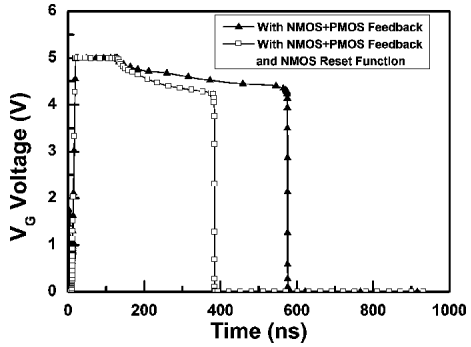


Fig. 16. Simulated $V_{\rm G}$ voltage waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function and power-rail ESD clamp circuit with NMOS+PMOS feedback under the ESD-like rising edge of HBM ESD stress.

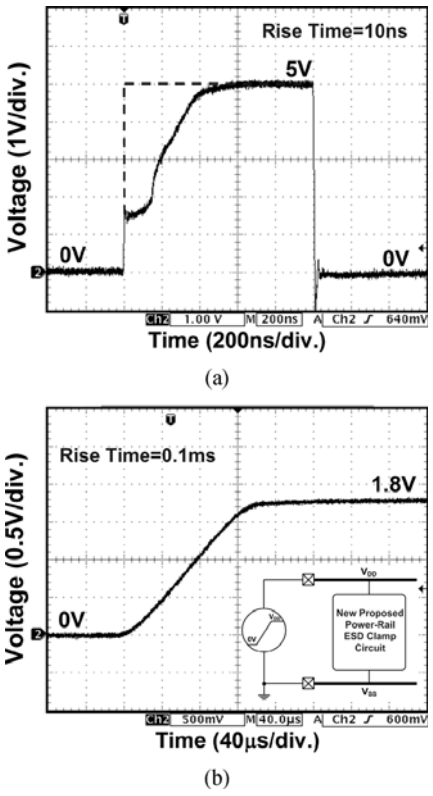


Fig. 17. Measured voltage waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function in (a) ESD-stress condition and (b) power-on condition.

ESD clamp circuit with NMOS+PMOS feedback continues to keep at 1.8 V. As shown in Fig. 15, the $V_{\rm G}$ voltage of the proposed power-rail ESD clamp circuit can be pulled down to 0 V to release the "latch-on" state of ESD-clamping NMOS. By increasing the device size of $\rm M_{NR1}$, the latch-on time of ESD-clamping NMOS can be reduced, as shown in Fig. 15. Therefore, the proposed power-rail ESD clamp circuit with NMOS reset function can avoid the latchup-like failure after system-level ESD tests.

For HBM ESD stress simulation, a fast ramp voltage with a rise time of 10 ns shown in Fig. 4(a) is applied to $V_{\rm DD}$ of the proposed power-rail ESD clamp circuit with NMOS reset function and the power-rail ESD clamp circuit with NMOS+PMOS feedback, whereas the $V_{\rm SS}$ is grounded. The pulse height of the fast ramp voltage set as 5 V, before drain breakdown of ESD-clamping NMOS, is used to monitor the voltage on the node $V_{\rm G}$ and the turn-on time of ESD-clamping NMOS. As shown in Fig. 16, compared with power-rail ESD clamp circuits with NMOS+PMOS feedback, the proposed power-rail ESD clamp circuit with NMOS reset function has a shorter turn-on time of around 380 ns.

C. Experimental Results

The proposed power-rail ESD clamp circuit with NMOS reset function has been designed and fabricated in a 0.18-μm CMOS process. Measurements were performed to compare the system-level ESD robustness between this proposed and the original power-rail ESD clamp circuits.

1) Turn-On Verification: To verify the ESD-transient detection function of the proposed power-rail ESD clamp circuit with NMOS reset function, a voltage pulse generated from a pulse generator is used to simulate the rising edge of HBM ESD pulse, which has a square-type voltage waveform with a rise time about 10 ns. When the voltage pulse is applied to $V_{\rm DD}$ power line with $V_{\rm SS}$ grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD-clamping NMOS to provide a low-impedance path between $V_{\rm DD}$ and $V_{\rm SS}$ power lines. Due to the limited driving current of the pulse generator, the voltage on $V_{\rm DD}$ power line will be degraded by the turned-on ESD-clamping NMOS. The voltage waveform on $V_{\rm DD}$ power line of the proposed power-rail ESD clamp circuit with NMOS reset function is shown in Fig. 17(a), where a voltage pulse with a pulse height of 5 V and a pulse width of 1000 ns is applied to $V_{\rm DD}$ power line. The voltage waveform is degraded at the rising edge because the ESD-clamping NMOS is simultaneously turned-on when the ESD-like voltage pulse is applied to $V_{\rm DD}$ power line. The voltage degradation is dependent on the turned-on resistance of the ESD-clamping NMOS and the output resistance (typically, 50 Ω) of the pulse generator. A larger device dimension of the ESD-clamping NMOS leads to a more serious degradation on the voltage waveform. When the $V_{\rm Filter}$ node is charged up to the threshold voltage of the inverter1 (formed by $\rm M_{P1}$ and $\rm M_{N1}$ in Fig. 14), the ESD-clamping NMOS will be turned off and the voltage waveform will be restored to the original voltage level. In Fig. 17(a), the applied 5-V voltage pulse has a recovery time of about 400 ns, which is corresponding to the turn-on time of the ESD-clamping NMOS.

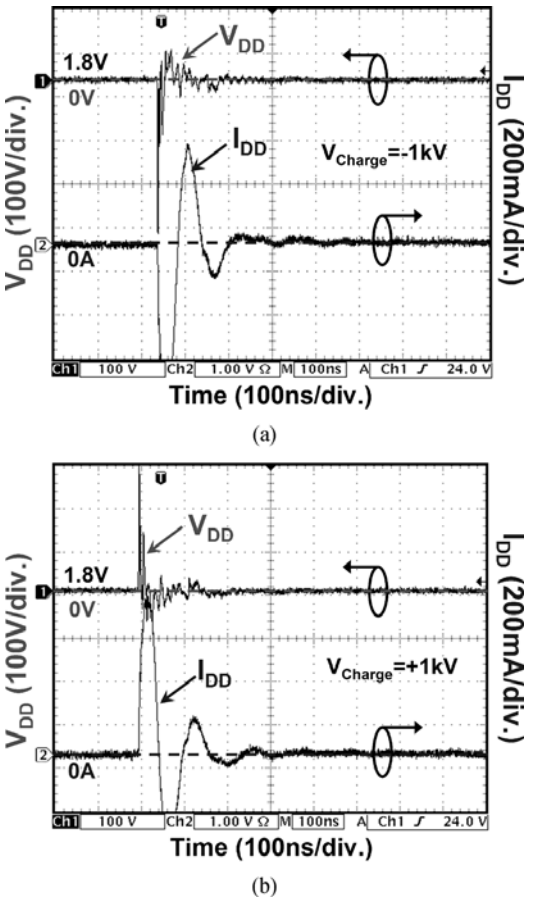


Fig. 18. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function under TLU test with $V_{\rm Charge}$ of (a) -1 kV and (b) $+1$ kV. No latchup-like failure occurs in this TLU test.

To verify the action of the proposed power-rail ESD clamp circuit with NMOS reset function under normal power-on conditions, an experimental setup is shown in the inset figure of Fig. 17(b). A ramp voltage with a rise time of 0.1 ms and a magnitude of 1.8 V is applied to $V_{\rm DD}$ power line with $V_{\rm SS}$ power line grounded to simulate the power-on condition. The measured voltage waveform on $V_{\rm DD}$ power line is shown in Fig. 17(b), where the voltage waveform is still remained as a ramp voltage without degradation. Thus, the ESD-clamping NMOS in the proposed power-rail ESD clamp circuit with NMOS reset function has been verified to keep off while the IC is in the power-on condition.

2) TLU Immunity: With the TLU measurement setup in Fig. 5, the measured $V_{\rm DD}$ and $I_{\rm DD}$ responses on the proposed power-rail ESD clamp circuit with $V_{\rm charge}$ of -1 kV and $+1$ kV are shown in Fig. 18(a) and (b), respectively. With a negative (positive) $V_{\rm charge}$ of -1 kV ($+1$ kV), latchup-like failure does not occur in Fig. 18(a) (Fig. 18(b)) because $I_{\rm DD}$ is not significantly increased and $V_{\rm DD}$ is not pulled down.

The TLU level of the proposed power-rail ESD clamp circuit with NMOS reset function and the original power-rail ESD clamp circuit with NMOS+PMOS feedback against system-level ESD test are listed in Table VII. Moreover, latchup-like failure does not occur in the proposed power-rail ESD clamp circuit after TLU tests with ESD voltage of up to -1 kV and $+1$ kV.

TABLE VII
COMPARISON ON TLU LEVELS BETWEEN PROPOSED POWER-RAIL ESD CLAMP CIRCUIT WITH NMOS RESET FUNCTION AND THE ORIGINAL POWER-RAIL ESD CLAMP CIRCUIT WITHNMOS+PMOS FEEDBACK UNDER TLU TEST

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
With NMOS+PMOS Feedback and NMOS Reset Function	Over +1kV	Over -1kV
With NMOS+PMOS Feedback	+12V	-4V

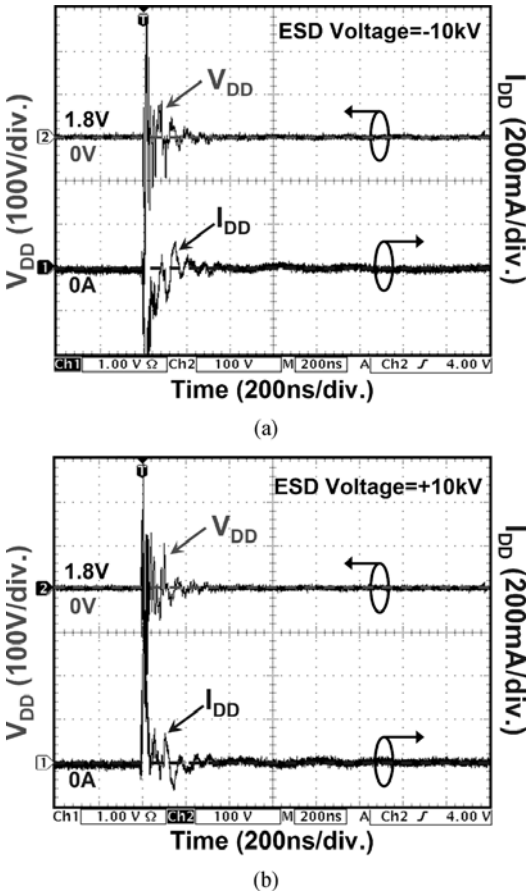


Fig. 19. Measured $V_{\rm DD}$ and $I_{\rm DD}$ waveforms on the proposed power-rail ESD clamp circuit with NMOS reset function under system-level ESD test with ESD voltage of (a) -10 kV and (b) $+10$ kV. No latchup-like failure occurs in this system-level ESD test.

3) System-Level ESD Susceptibility: The measured $V_{\rm DD}$ and $I_{\rm DD}$ responses on the proposed power-rail ESD clamp circuit under system-level ESD tests with ESD voltages of -10 kV and $+10$ kV are shown in Fig. 19(a) and (b), respectively. With a negative (positive) ESD voltage of -10 kV ($+10$ kV), the latchup-like failure does not occur in Fig. 19(a) (Fig. 19(b)) because the $I_{\rm DD}$ is not significantly increased and $V_{\rm DD}$ is not pulled down.

The susceptibility of the proposed power-rail ESD clamp circuit with NMOS reset function and the original power-rail ESD clamp circuit with NMOS+PMOS feedback against

TABLE VIII
COMPARISON ON THE SUSCEPTIBILITY BETWEEN PROPOSED POWER-RAIL ESD CLAMP CIRCUIT WITH NMOS RESET FUNCTION AND THE ORIGINAL POWER-RAIL ESD CLAMP CIRCUIT WITH NMOS+PMOS FEEDBACK UNDER SYSTEM-LEVEL ESD TEST

Power-Rail ESD Clamp Circuits	Positive ESD Stress	Negative ESD Stress
With NMOS+PMOS Feedback and NMOS Reset Function	Over +10kV	Over -10kV
With NMOS+PMOS Feedback	+2.5kV	-0.2kV

TABLE IX
COMPARISON OF HBM LEVEL, CDM LEVEL, AND LAYOUT AREA AMONG FIVE DIFFERENT POWER-RAIL ESD CLAMP CIRCUITS IN A 0.18-μm CMOS PROCESS

Power-Rail ESD Clamp Circuits	HBM ESD Level	CDM ESD Level	Layout Area	
			ESD-Clamping NMOS	ESD-Transient Detection Circuit
Typical RC-Based Detection	Over ±8kV	Over ±1kV	95μm x 80μm	35μm x 80μm
With PMOS Feedback	Over ±8kV	Over ±1kV	95μm x 80μm	40μm x 80μm
With NMOS+PMOS Feedback	Over ±8kV	Over ±1kV	95μm x 80μm	40μm x 80μm
With Cascaded PMOS Feedback	Over ±8kV	Over ±1kV	95μm x 80μm	40μm x 80μm
With NMOS+PMOS Feedback and NMOS Reset Function	Over ±8kV	Over ±1kV	95μm x 80μm	40μm x 80μm

system-level ESD test are compared in Table VIII. For the proposed power-rail ESD clamp circuit, latchup-like failure does not occur.

4) Chip-Level ESD Robustness: The chip-level ESD robustness (HBM and CDM) and layout area of the five different power-rail ESD clamp circuits integrated in this work are listed in Table IX. In order to provide a low impedance path between $V_{\rm DD}$ and $V_{\rm SS}$ power lines to efficiently discharge ESD current under chip-level ESD stresses conditions, the ESD-clamping NMOS has been drawn with a large device dimension ($\rm W/L = 2000\ \mu m/0.18\ \mu m$). Therefore, the layout area of five different power-rail ESD clamp circuits is dominated by the ESD-clamping NMOS. ESD-transient detection circuits only occupy smaller part in the whole layout area, as compared with the layout area of ESD-clamping NMOS. The proposed power-rail ESD clamp circuit with NMOS reset function and the aforementioned four different power-rail ESD clamp circuits can pass HBM ESD stress of over ± 8 kV and CDM ESD stress of over ± 1 kV.

CDM test in this work was carried out according to ESDA CDM test standard [20] and the package type of test chip is 40-pin side braze package. Five different power-rail ESD clamp circuits are all included in a test chip with separated $V_{\rm DD}$ and $V_{\rm SS}$ pins, where the die size of test chip is $1500 \times 1500\ \mu\rm m^2$. During CDM ESD test on the test chip with different power-rail ESD clamp circuits, the direct charging method in the ESDA CDM test standard was used. The ± 1 kV ESD voltages are directly charged into the $V_{\rm SS}$ pin that is connected with the p-type substrate of the test chip, and then the corresponding separated $V_{\rm DD}$ pin of the selected power-rail ESD clamp circuit is touched by external ground. After CDM test with ESD voltage of ± 1 kV, the leakage current of power-rail ESD clamp circuits under 1.8-V bias was rechecked to be within 20% variation of its initial value. CDM ESD characterization is highly dependent on the package type, die size, and the adopted ESD test method [21]. A chip with large parasitic capacitance from the package or from the large die size often has a lower CDM ESD robustness.

VI. CONCLUSION

Some of advanced on-chip power-rail ESD clamp circuits with feedback loop have been found to suffer the latchup-like failure after system-level ESD tests. A modified design on the power-rail ESD clamp circuit with NMOS+PMOS feedback, by using NMOS reset function to turn off the ESD-clamping NMOS after system-level ESD tests, has been successfully verified in a 0.18-μm CMOS process. The proposed power-rail ESD clamp circuit with NMOS reset function can sustain the system-level ESD stress of over ± 10 kV without causing latchup-like failure after system-level ESD tests. The proposed power-rail ESD clamp circuit has the advantages of smaller *RC* area, high ESD robustness, and no latchup-like failure, which is much suitable for CMOS ICs in system applications.

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REFERENCES

[1] S. Voldman, *ESD: Circuit and Devices*. New York: Wiley, 2006.
[2] Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level ESD Association, Standard Test Method ESD STM5.1–2001, 2001.
[3] C. Duvvury, R. Rountree, and O. Adams, "Internal chip ESD phenomena beyond the protection circuit," *IEEE Trans. Electron Devices*, vol. 35, pp. 2133–2139, Dec. 1998.
[4] M.-D. Ker, "Whole-chip ESD protection design with efficient $V_{\rm DD}$-to-$V_{\rm SS}$ clamp circuit for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.
[5] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. EOS/ESD Symp.*, 1993, pp. 233–237.
[6] P. Tong, W. Chen, R. Jiang, J. Hui, P. Xu, and P. Liu, "Active ESD shunt with transistor feedback to reduce latchup susceptibility or false triggering," in *Proc. IEEE Int. Phys. Failure Anal. Integr. Circuits Symp.*, 2004, pp. 89–92.
[7] S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1–5.
[8] J. Smith and G. Boselli, "A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symp.*, 2003, pp. 8–16.
[9] J. Li, R. Gauthier, and E. Rosenbaum, "A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symp.*, 2004, pp. 273–279.
[10] *EMC – Part 4–2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*, IEC 61000–4-2 International Standard, 2001.
[11] N. Shimoyama, M. Tanno, S. Shigematsu, H. Morimura, Y. Okazaki, and K. Machida, "Evaluation of ESD hardness for fingerprint sensor LSIs," in *Proc. EOS/ESD Symp.*, 2004, pp. 75–81.
[12] D. Smith and A. Wallash, "Electromagnetic interference (EMI) inside a hard disk driver due to external ESD," in *Proc. EOS/ESD Symp.*, 2002, pp. 32–36.
[13] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in an 8-bits microcontroller to solve the system-level ESD issue on keyboard," in *Proc. EOS/ESD Symp.*, 1999, pp. 352–360.

[14] C.-C. Yen and M.-D. Ker, "Failure of on-chip power-rail ESD clamp circuits during system-level ESD test," in *Proc. IEEE Int. Reliability Physics Symp.*, 2007, pp. 598–599.
[15] Electrostatic Discharge Simulator Noise Laboratory Co., Ltd., Japan, NoiseKen ESS-2002 & TC-825R.
[16] M.-D. Ker and S.-F. Hsu, "Component-level measurement for transient-induced latch-up in CMOS ICs under system-level ESD considerations," *IEEE Trans. Device Mater. Reliab.*, vol. 6, no. 3, pp. 461–472, Sep. 2006.
[17] *Electrostatic Discharge Sensitivity Testing – Machine Model – Component Level*, Standard Test Method ESD STM5.2–1999, ESD Association, 1999.
[18] M.-D. Ker and W.-Y. Lo, "Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 2, pp. 319–334, 2003.
[19] M. Stockinger, J. Miller, M. Khazhinsky, C. Torres, J. Weldon, B. Preble, M. Bayer, M. Akers, and V. Kamat, "Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symp.*, 2003, pp. 17–26.
[20] *Electrostatic Discharge Sensitivity Testing – Charge Device Model – Component Level*, Standard Test Method ESD STM5.3.1–1999, ESD Association, 1999.
[21] Y.-W. Hsiao and M.-D. Ker, "Investigation on discharge current waveforms in board-level CDM ESD events with different board sizes," in *Presentations of the 2nd Int. ESD Workshop*, 2008, pp. 284–296.

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