

## Durham Research Online

---

### Deposited in DRO:

16 December 2011

### Version of attached file:

Published Version

### Peer-review status of attached file:

Peer-reviewed

### Citation for published item:

Bryant, A. and Yang, S. and Mawby, P. and Xiang, D.W. and Ran, L. and Tavner, P.J. and Palmer, P.R. (2011) 'Investigation into IGBT  $dV/dt$  during turn-off and its temperature dependence.', IEEE transactions on power electronics., 26 (10). pp. 3019-3031.

### Further information on publisher's website:

<http://dx.doi.org/10.1109/TPEL.2011.2125803>

### Publisher's copyright statement:

© 2011 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

### Additional information:

## Use policy

---

The full-text may be used and/or reproduced, and given to third parties in any format or medium, without prior permission or charge, for personal research or study, educational, or not-for-profit purposes provided that:

- a full bibliographic reference is made to the original source
- a [link](#) is made to the metadata record in DRO
- the full-text is not changed in any way

The full-text must not be sold in any format or medium without the formal permission of the copyright holders.

Please consult the [full DRO policy](#) for further details.

# Investigation into IGBT $dV/dt$ during Turn-Off and its Temperature Dependence

Angus Bryant, *Member, IEEE*, Shaoyong Yang, *Member, IEEE*,  
Philip Mawby, *Senior Member, IEEE*, Dawei Xiang, Li Ran, *Senior Member, IEEE*  
Peter Tavner, *Senior Member, IEEE* and Patrick Palmer, *Member, IEEE*

**Abstract**—In many power converter applications, particularly those with high variable loads such as traction and wind power, condition monitoring of the power semiconductor devices in the converter is considered desirable. Monitoring the device junction temperature in such converters is an essential part of this process. In this paper, a method for measuring the IGBT junction temperature using the collector voltage  $dV/dt$  at turn-off is outlined. A theoretical closed-form expression for the  $dV/dt$  at turn-off is derived, closely agreeing with experimental measurements. The role of  $dV/dt$  in dynamic avalanche in high-voltage IGBTs is also discussed. Finally, the implications of the temperature dependence of the  $dV/dt$  are discussed, including implementation of such a temperature measurement technique.

**Index Terms**—Power electronics, power semiconductor device, converter, reliability, dynamic avalanche.

## I. INTRODUCTION

Controlling the reliability of power semiconductor devices is becoming increasingly important. Electrical power conversion using power electronic systems is critical in both the generation and efficient use of sustainable energy. As the use of sustainable energy increases, the need for reliable conversion systems becomes more important. Power electronic converters for both traction (automotive and rail) and wind power generation, to name two examples, are subject to large junction temperature swings during normal operation that are not typical of other power converter applications. For wind power in particular, the widely-varying and intermittent nature of the wind speed and the low converter modulation frequencies (as low as a few hertz for large pole-number, direct drive machines) has a severe effect on device reliability due to the resulting deep thermal cycling [1]. As increasing use of offshore wind farms is made, converter reliability is particularly important since the access for maintenance or repair is severely limited due to adverse weather conditions [2], [3].

While reliability modelling tools are now coming into use in the converter design stage, e.g. [4]–[6], there still exists a need for condition monitoring of devices during the lifetime

This work was supported by the Engineering and Physical Sciences Research Council, grants EP/E02744X/1 and EP/E026923/1, and by the Schiff Foundation, Cambridge University.

Angus Bryant, Shaoyong Yang and Philip Mawby are with the School of Engineering, University of Warwick, Coventry, CV4 7AL, U.K.

Dawei Xiang, Li Ran and Peter Tavner are with the School of Engineering, University of Durham, Durham, DH1 3LE, U.K.

Patrick Palmer is with the Centre for Advanced Photonics and Electronics, Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K.

of the converter [7], [8]. This is particularly the case in the example of offshore wind turbines because of their limited access. Such methods of condition monitoring depend on measuring the device temperature or other precursors over the lifetime of the converter [9]. This may be used in thermal cycle counting [4], [10], [11] to estimate the consumed lifetime of the converter and hence allow predictive maintenance to take place. Additionally, shut-down of the converter may take place if the device temperature suddenly increases as a precursor to packaging and device failure [12].

However, sensing the junction temperature during converter operation is notoriously difficult. The three main methods that have been reported for sensing the IGBT junction temperature are:

- Change in on-state collector voltage ( $V_{CE(sat)}$ ) with temperature at a given load current [13].
- Change in gate parameters (transconductance, threshold voltage) with temperature [14]–[17].
- Estimation of device losses and hence junction temperature from converter operating conditions and the packaging and heatsink thermal impedance [10], [18]–[20].

The first suffers from the difficulty in obtaining an accurate measurement of a few millivolts change in  $V_{CE}$  in the on-state against a background of  $V_{CE}$  switching to several hundred or thousand volts in the off-state. The second relies on measuring the rate of change of both the collector current and gate voltage during turn-on, or measuring the exact instance of collector current increase when the gate voltage crosses the threshold voltage, neither of which is straightforward. The last, while not requiring any difficult sensing methods, relies on knowing the packaging thermal impedance; however towards the end of life the thermal resistance increases due to solder degradation, leading to an underestimate of the temperature.

An alternative parameter which changes with temperature is the rate of change of collector voltage,  $dV_{CE}/dt$ , during IGBT turn-off. This is usually at its most positive during the main rise in collector voltage; therefore it may be sensed directly from the IGBT voltage, or indirectly from the time delay in turn-off and the resulting distortion in the converter PWM waveform [21]. The latter may utilise harmonic identification methods to detect the small change in IGBT turn-off time resulting from  $dV/dt$  changes with junction temperature. The  $dV/dt$  depends on the junction temperature, load current, collector voltage and IGBT gate circuit, with much of this

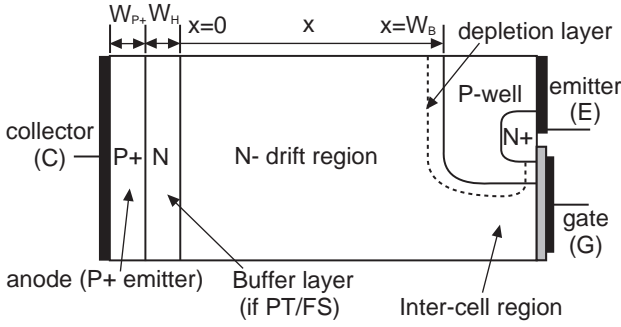


Fig. 1. Basic IGBT structure, shown for a planar device.

dependence due to the charge stored within the IGBT. While previous work has examined the physics behind the collector voltage rise at turn-off [22]–[25], it does not form a closed-form expression for the  $dV/dt$  and thus the dependencies in the IGBT cannot be fully analysed. Furthermore, as high-voltage IGBTs with ratings above 4.5 kV are increasingly in use, there is an opportunity for an improved understanding to be gained of the role of  $dV/dt$  in the onset of dynamic avalanche in high-voltage IGBTs.

This paper examines the theory behind the IGBT collector voltage  $dV/dt$  during turn-off, and develops an analytical model for it in terms of physical device parameters and operating conditions. This is compared with experimental measurements, followed by the application to temperature sensing for condition monitoring.

## II. IGBT TURN-OFF OPERATION

### A. Overview of the Turn-Off Process

The structure of an IGBT is dominated by a wide lightly-doped N- drift (base) region, sandwiched between a P+ emitter (the anode) and a P-well/MOS gate region. The gate structure may contain a lateral channel, giving a planar IGBT, or a vertical channel situated alongside a trench gate. At the anode there may be an N-type buffer layer, giving a punch-through (PT) or field-stop (FS) device, as opposed to a non-punch-through (NPT) device. Fig. 1 shows a classic planar IGBT structure.

Regardless of the structure of a particular device, the behaviour of the carriers in the drift region is governed by the ambipolar diffusion equation (ADE):

$$D \frac{\partial^2 p(x, t)}{\partial x^2} = \frac{p(x, t)}{\tau} + \frac{\partial p(x, t)}{\partial t} \quad (1)$$

The concentration of excess carriers  $p(x, t)$  is determined by the boundary conditions at each end of the drift region. In most IGBTs the long high-level lifetime  $\tau$  (typically a few  $\mu\text{s}$  to tens of  $\mu\text{s}$ ) gives rise to a long diffusion length  $L_a = \sqrt{D\tau}$ , where  $D$  is the ambipolar diffusivity.  $L_a$  is typically similar in length to, or longer than, the drift region width  $W_B$ , giving rise to an almost linear excess carrier density distribution  $p(x)$ . Fig. 2 shows a plot of the hole concentration across the drift region (under the gate) for a NPT planar IGBT, generated using Silvaco ATLAS [26] simulations.

During turn-off the stored charge must be evacuated; this sets rate of rise in collector voltage,  $dV_{CE}/dt$ , as the charge

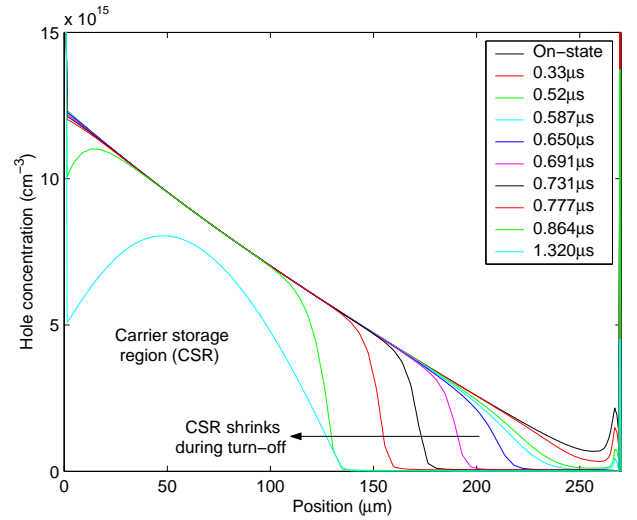


Fig. 2. ATLAS simulation of IGBT turn-off for a NPT DMOS structure, showing the hole concentration profile as the CSR shrinks. The collector current  $I_C$  starts to fall between  $0.777\mu\text{s}$  and  $0.864\mu\text{s}$ , and the current tail (phase 5) commences between  $0.864\mu\text{s}$  and  $1.320\mu\text{s}$ .

is extracted and the depletion layer expands. Fig. 3 shows a typical NPT IGBT inductive turn-off waveform, with the five phases of turn-off described as follows:

- 1) The gate voltage  $V_{GE}$  falls to a level set by the MOS channel current (approximately proportional to the collector current  $I_C$ ). The MOS channel is in linear operation during this phase.
- 2) The MOS channel is now in saturated operation. The Miller capacitance  $C_{GC}$  charges through the gate and the collector voltage  $V_{CE}$  starts to rise.
- 3) Once the accumulation layer under the gate has disappeared, the Miller capacitance decreases suddenly (when  $C_{acc}$  becomes zero in appendix I of [27]) and  $V_{CE}$  increases sharply.  $dV_{CE}/dt$  is now limited by the rate at which the depletion layer can expand.
- 4) Once  $V_{CE}$  has reached approximately the supply voltage  $V_{DC}$  the freewheel diode can turn on. This allows  $I_C$  to fall to a level  $I_{CT}$  set by the remaining stored charge, and the collector  $V_{CE}$  exhibits the classic overshoot from discharging the stray inductance.
- 5) The current tail now begins, and  $I_C$  is now set only by the remaining stored charge and recombination rate. The tail current is strongly dependent on the high-level carrier lifetime  $\tau$  in the drift region and the charge remaining in the N-base.

### B. $dV/dt$ Dependency and the Need for an Improved Model

The collector voltage rises during phase 3 because of a small reduction in the IGBT gate voltage  $V_{GE}$ , as expected because the gate drive voltage  $V_{GG}$  is now zero or negative. This causes a slight reduction in the MOS channel current  $I_{ch}$ , while in the on-state this provides the electron current into the N-base to maintain the required level of stored charge. Reducing this slightly causes stored charge to be extracted, allowing the depletion layer to expand and the collector voltage to rise.

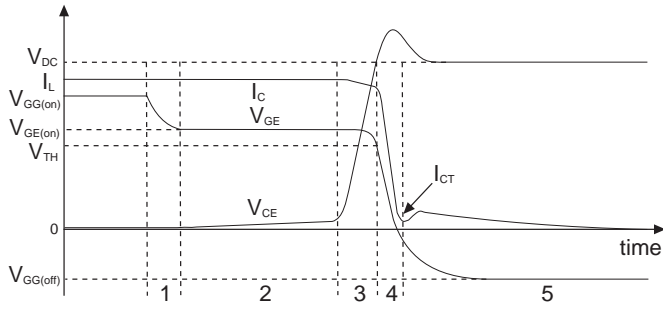


Fig. 3. Detail of a typical NPT IGBT inductive turn-off process, showing the five phases of IGBT turn-off.

Once the collector current falls in phase 4, the MOS channel current falls too and the MOS channel can turn off.

This process is analysed in references [22]–[24]. Both give similar expressions for the  $dV/dt$ , dependent on the “instantaneous current”  $i$  which forces the depletion layer expansion and rise in collector voltage; see appendix I for further details. The expression in [24] is:

$$i = \frac{\varepsilon A p_0}{W_B N_B} \frac{dV_{CE}}{dt}, \quad (2)$$

where  $p_0$  is the excess carrier density in the on-state at the anode PN-junction,  $\varepsilon$  is the silicon permittivity,  $A$  is the active chip area,  $N_B$  is the drift region doping and  $W_B$  is the drift region width as in Fig. 1. This may be considered to be a capacitive expression, linking the  $dV/dt$  to the current  $i$  via a charge extraction capacitance  $C_O$ :

$$i = C_O \frac{dV_{CE}}{dt}, \quad (3)$$

$$C_O = \frac{\varepsilon A p_0}{W_B N_B}. \quad (4)$$

Using typical values for a 1700 V planar NPT IGBT, with  $p_0 = 8 \times 10^{15} \text{ cm}^{-3}$ ,  $W_B = 266 \text{ }\mu\text{m}$ ,  $A = 1 \text{ cm}^2$  and  $N_B = 10^{14} \text{ cm}^{-3}$ , the charge extraction capacitance  $C_O$  in equation (4) is approximately 3.2 nF. This remains approximately constant with collector voltage. In comparison, the depletion layer capacitance,  $C_{dep}$ , defined in appendix I, decreases from 410 pF at  $V = 50 \text{ V}$  to 167 pF at  $V = 300 \text{ V}$ ; clearly this is small in comparison.

While the expression in equation (2) gives an estimation for the instantaneous current to force the charge extraction, it does not relate directly to the load current  $I_C$ . This may be many times larger than the instantaneous current  $i$ . Hence this does not result in a closed-form expression for  $dV/dt$ , giving an incomplete explanation for the mechanisms behind the collector voltage rise. This is particularly important because a full understanding is needed for explanation of the temperature dependency of  $dV_{CE}/dt$  at turn-off.

The factor omitted in previous work is the role of the MOS channel. This provides negative feedback from the collector voltage to the gate voltage, stabilising the  $dV/dt$  during phase 3. If the gate voltage falls too much, the MOS channel current falls, causing a reduced electron current into the remaining

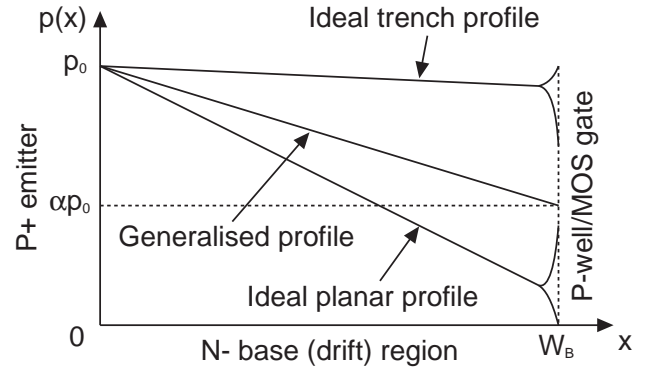


Fig. 4. Charge profile for ideal planar ( $\alpha=0$ ) and trench ( $\alpha=1$ ) carrier density distributions. The generalised carrier density distribution, with an intermediate carrier density level,  $\alpha p_0$ , at the cathode is also shown.

stored charge and hence an increase in  $dV_{CE}/dt$ . This causes, through the Miller capacitance  $C_{GC}$ , extra current to flow into the gate, opposing the reduction in gate voltage. Therefore in addition to the role of the stored charge in limiting the  $dV/dt$  there is a strong coupling with the MOS channel and gate circuit. The latter is obvious from the conventional role played by the gate resistance  $R_G$  in controlling the switching speed.

### III. ANALYTICAL MODEL

A model is now required to relate the  $dV/dt$ , gate drive characteristics, collector current and temperature dependent device parameters. The derivation proceeds as follows. Firstly, the level of stored charge affects the rate of its extraction at turn-off. Secondly, the stored charge depends on the collector current and P+ emitter (anode) recombination. Thirdly, the rate of extraction also depends on the action of the MOS channel and the Miller capacitance  $C_{GC}$ . Finally, these are combined to give the closed form expression with temperature dependence.

#### A. Stored Charge and Carrier Injection

In modelling the charge extraction capacitance, there are two assumptions that are made. Firstly, the high-level lifetime  $\tau_{HL}$  in the drift (base) region is sufficiently high so that the excess carrier density curve  $p(x)$  is approximately linear. Secondly, the high lifetime ensures that the carrier density profile of the remaining stored charge not yet swept out by the expanding depletion layer remains constant during turn-off. The carrier density within the conductivity-modulated drift region (carrier storage region, CSR) in the on-state, shown in fig. 4, can then be approximated by:

$$p_0(x) = p_0 \left( 1 - \frac{(1-\alpha)x}{W_B} \right) \quad (5)$$

where  $p_0$  is the excess carrier density in the on-state at the anode PN-junction and  $W_B$  is the drift region width.  $\alpha$  sets the carrier density at the MOS end of the base region, which depends on the technology (planar or trench) and relative widths of the P-well and intercell (MOS gate) regions. This is illustrated in fig. 4 for “ideal” planar and trench carrier density distributions.

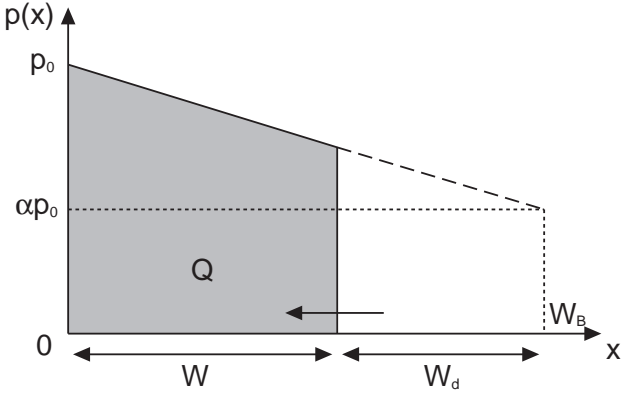


Fig. 5. Charge extraction and CSR shrinkage during IGBT turn-off. The CSR width  $W$  is decreasing and the boundary is moving towards  $x = 0$ .

$p_0$  is found by solving for the carrier density gradient  $\partial p/\partial x$  at the anode junction as described in appendix II, giving:

$$p_0 = \sqrt{\frac{bI_C}{qAh_p(b+1)}}. \quad (6)$$

$h_p$  is the P-emitter recombination parameter, as defined in appendix II, and  $b = \mu_n/\mu_p$  is the ratio of the mobilities. The critical role of  $h_p$ , therefore, is to set the level of excess charge injected into the N-base. As the P+ emitter doping level is increased,  $h_p$  decreases as shown in appendix II and therefore  $p_0$  increases as expected. This therefore affects the charge extraction capacitance, equation (4), and hence the  $dV/dt$  at turn-off.

### B. Charge Extraction Capacitance

As the depletion layer expands and the CSR shrinks, the boundary between the two at  $x = W$  moves towards  $x = 0$ , see fig. 5. The rate of change of total charge  $Q$  in the CSR can be expressed as follows by the charge control equation, shown for electrons here (a corresponding version exists for holes):

$$\frac{dQ}{dt} = I_{n2} - I_{n1} - \frac{Q}{\tau_{HL}} \quad (7)$$

$I_{n2}$  is the electron current at the cathode end of the CSR, equal to the MOS channel current  $I_{ch}$ , and  $I_{n1}$  is that at the anode end, equal to the emitter recombination current. In the on-state, assuming that  $\tau_{HL}$  is large, the approximation  $I_{n2} \approx I_{n1} \approx bI_C/(b+1)$  can be made. When the depletion layer is expanding during phase 3, the charge is extracted because  $I_{n2} < I_{n1}$ , i.e.  $I_{ch} < bI_C/(b+1)$ . This difference, defined here as  $\Delta I_{ch}$ , is approximately equal to  $-dQ/dt$ . ( $\Delta I_{ch}$  should strictly include the displacement current from the depletion capacitance  $C_{dep}$ ; however, since  $p_0 \gg N_B$  and as discussed earlier and in appendix I, this may be neglected.) Hence:

$$\Delta I_{ch} = \frac{bI_C}{b+1} - I_{ch} = -\frac{dQ}{dt} \quad (8)$$

$$= -\frac{dQ}{dW} \frac{dW}{dV_{CE}} \frac{dV_{CE}}{dt} \quad (9)$$

$V_{CE}$  is related to the depletion layer width  $W_d = W_B - W$  by:

$$W_d = \sqrt{\frac{2\varepsilon V_{CE}}{qN_T}}. \quad (10)$$

$N_T$  is the effective carrier density in the depletion region, consisting of the drift region doping level  $N_B$  and the extra carriers arising from the electron and hole currents flowing through the depletion layer. Appendix III discusses this in more detail.

The charge remaining in the CSR is found by integrating the carrier density from  $x = 0$  to  $W$ , Fig. 5:

$$Q = qA \int_0^W p_0 \left(1 - \frac{(1-\alpha)x}{W_B}\right) dx \quad (11)$$

Differentiating and substituting equations (10,11) into equation (9) gives an expression for the rate of change of charge:

$$\Delta I_{ch} = \frac{p_0}{N_T} \left[ \alpha \frac{\varepsilon A}{W_d} + (1-\alpha) \frac{\varepsilon A}{W_B} \right] \frac{dV_{CE}}{dt} \quad (12)$$

Hence, with  $C_{dep}$  defined as  $\varepsilon A/W_d$  and  $C_{min}$  defined as  $\varepsilon A/W_B$ , the charge extraction capacitance  $C_O$  is defined by and related to  $\Delta I_{ch}$  by:

$$\Delta I_{ch} = C_O \frac{dV_{CE}}{dt} \quad (13)$$

$$C_O = \frac{p_0}{N_T} [\alpha C_{dep} + (1-\alpha)C_{min}] \quad (14)$$

The significant role played by the stored charge in increasing  $C_O$  is clear here. As the stored charge increases with  $p_0$ , the change in MOS channel current,  $\Delta I_{ch}$ , required to achieve a particular  $dV/dt$ , must increase. It is also clear from equation (14) that the value of  $C_O$  changes with voltage, depending on the value of  $\alpha$ . In ideal planar IGBTs, with  $\alpha = 0$ ,  $C_O$  is constant with  $V_{CE}$  since there is no contribution of  $C_{dep}$ ; in ideal trench IGBTs ( $\alpha = 1$ )  $C_O$  is a direct multiple of the depletion layer capacitance and varies significantly with  $V_{CE}$ . In practice  $\alpha$  is always greater than zero, even in planar IGBTs.

### C. Negative Feedback via the MOS Channel

The change in channel current  $\Delta I_{ch}$  is caused by a small reduction in gate voltage from the MOS saturation (plateau) value in phase 2. Defining the latter as  $V_{GE(on)}$  – which is clearly dependent on the load (collector) current, equation (15) – and assuming the reduction in gate voltage,  $\Delta V_{GE}$ , is small, this gives the relationship between  $\Delta I_{ch}$  and  $\Delta V_{GE}$  in equation (17):

$$I_{ch} = \frac{bI_C}{b+1} = \frac{K_p}{2} (V_{GE(on)} - V_{TH})^2 \quad (15)$$

$$\Delta I_{ch} = K_p (V_{GE(on)} - V_{TH}) \Delta V_{GE} \quad (16)$$

$$= g_m \Delta V_{GE} \quad (17)$$

As the collector voltage rises, the current flowing out of the gate,  $I_G$ , mostly consists of the gate-collector capacitance current (assuming that the  $dV_{GE}/dt$  is small):

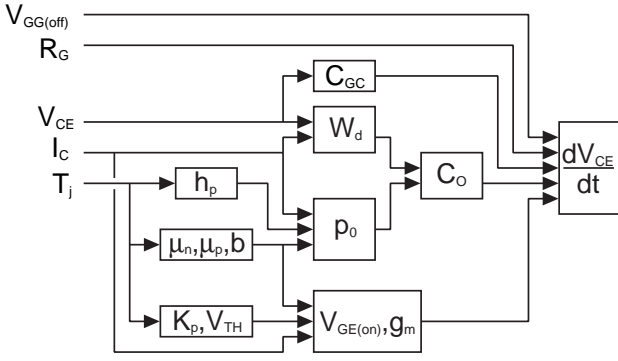


Fig. 6. Summary of dependency of  $dV_{CE}/dt$  on operating conditions and temperature-dependent parameters, described in function blocks.

$$I_G = C_{GC} \frac{dV_{CE}}{dt}. \quad (18)$$

Hence, with  $\tau_G = R_G C_{GC}$ ,

$$V_{GE(on)} - V_{GG(off)} = \frac{\tau_G}{C_O} I_{ch}, \quad (19)$$

where  $V_{GG(off)}$  is the gate drive voltage (zero or negative). Substituting equation (17) and rearranging gives the closed-form expression for the  $dV/dt$ :

$$\frac{dV_{CE}}{dt} = \frac{1}{\tau_G} \left( \frac{V_{GE(on)} - V_{GG(off)}}{1 + \frac{C_O}{g_m \tau_G}} \right) \quad (20)$$

This expression for  $dV/dt$  is expected, since if there is very little or no stored charge ( $C_O \rightarrow 0$ ) then it is set solely by the gate resistance and gate-collector capacitance. It is also equivalent to the expression given in [28], but with the inclusion of the stored charge via  $C_O$ . However as the level of stored charge increases with  $C_O$ , the  $dV/dt$  reduces and is ultimately limited by the level of stored charge. Reducing the gate resistance  $R_G$  below a certain level to increase the  $dV/dt$  and hence the switching speed does not produce any further effect since the  $dV/dt$  is limited by the stored charge in the IGBT.

#### D. Temperature and Operating Condition Dependency

A summary of the dependencies of all parameters within the expression for  $dV/dt$  is given in Fig. 6. Both the junction temperature  $T_j$  and the collector (load) current  $I_C$  have significant influences, and the instantaneous collector voltage  $V_{CE}$  affects the  $dV/dt$  too. The junction temperature affects the  $dV/dt$  through the MOS channel parameters  $V_{TH}$  and  $K_p$  and the emitter recombination parameter  $h_p$  (via the stored charge).

The temperature dependencies of  $\mu_n$ ,  $\mu_p$ ,  $V_{TH}$  and  $K_p$  are relatively well-determined [29]. That of  $h_p$  is less well-determined; a discussion of this is given in appendix II.B.

The device parameters were estimated from datasheet values using the procedures in [30]. The transfer characteristics were obtained using a Tektronix 371B curve tracer with the device placed in an environmental chamber to control the

TABLE I  
IGBT PARAMETERS

Parameter	Symbol	Value
Device area	$A$	$0.5 \text{ cm}^2$
Base width	$W_B$	$100 \text{ } \mu\text{m}$
Base doping	$N_B$	$8 \times 10^{13} \text{ cm}^{-3}$
Emitter recomb. param.	$h_p$	$1.7 \times 10^{-13} \text{ cm}^4 \text{ s}^{-1}$
Saturation velocity	$v_{sat}$	$1 \times 10^7 \text{ cm.s}^{-1}$
Intercell area ratio	$a_i$	0.5
Cathode charge ratio	$\alpha$	0.5
MOS channel conductance	$K_p$	$7.8 \text{ A.V}^{-2}$
MOS threshold voltage	$V_{TH}$	6.7 V
Electron mobility	$\mu_n$	$1400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$
Hole mobility	$\mu_p$	$450 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$
Gate resistance	$R_G$	$15 \text{ } \Omega$

temperature. Fig. 11 shows the transfer characteristics, both experimental and fitted, with the temperature dependencies given in equations (21) and (22). Table I shows the necessary device parameters for this work.

$$K_p = K_{p0} \left( \frac{300}{T_j} \right)^{0.8} \quad (21)$$

$$V_{TH} = V_{TH0} - 6.775 \times 10^{-3} (T_j - 300) \quad (22)$$

The temperature dependency exponent  $k$  for the emitter recombination parameter  $h_p$ , as in equation (50), was set to 0.5. Temperature dependencies for  $\mu_n$  and  $\mu_p$  were taken from [29]; that for  $v_{sat}$  was based on data in [31] and used a linear change of  $-10^4 \text{ cm.s}^{-1} \text{ K}^{-1}$ . It is assumed that  $V_{GG(off)}$  is zero during phase 3.

## IV. EXPERIMENTAL OBSERVATIONS

### A. Switching Test Results

The dependence derived in equation (20) may be validated by performing inductive switching tests on IGBTs. In this work, a planar non-punch-through (NPT) IGBT rated at 1200 V and 50 A was tested under inductive switching conditions. The switching waveforms at turn-off were recorded at different device temperatures, load currents and supply voltages to study the effects of these conditions on  $dV_{CE}/dt$ , and to compare quantitatively with predictions from equation (20).

Turn-off waveforms at supply voltages of 160 V and 300 V and a load current of 50 A are shown in figs. 7 and 8 respectively. Note that the  $dV/dt$  decreases as the temperature increases.

The  $dV/dt$  is not constant during switching because, as explained in section III-D, the capacitances  $C_O$  and  $C_{GD}$  vary with  $V_{CE}$ . The maximum  $dV/dt$  occurs when  $V_{CE} = V_{DC}$ , as evident in Figs. 7 and 8. Furthermore, the relatively high stray inductance used in the experimental setup, giving large voltage overshoots, arises from the extra length of the commutation loop from the use of the environmental chamber. However the stray inductance does not determine the maximum  $dV_{CE}/dt$  because it only affects phase 4 of the turn-off process after  $V_{CE}$  has exceeded  $V_{DC}$ , i.e. when the freewheel diode turns on and  $dI_C/dt \ll 0$ .

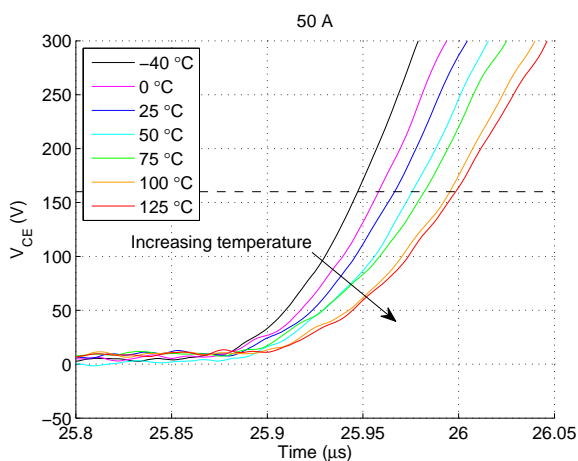


Fig. 7. Turn-off waveforms for  $V_{CE}$  at a supply voltage of 160 V and a load current of 50 A, shown with varying temperature. All traces are shown in reference to the supply voltage of 160 V.

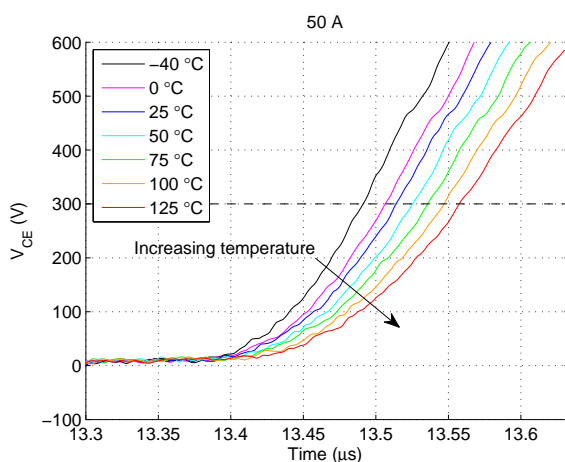


Fig. 8. Turn-off waveforms for  $V_{CE}$  at a supply voltage of 300 V and a load current of 50 A, shown with varying temperature. All traces are shown in reference to the supply voltage of 300 V.

The maximum gradient was calculated from the curves at all temperatures, load currents and supply voltages for comparison with the predicted  $dV/dt$  values. The resulting experimentally-measured maximum  $dV/dt$  values are shown in figs. 9 and 10, with linear fits shown. The slope of  $6.746 \text{ V}\cdot\mu\text{s}^{-1}\text{K}^{-1}$  is common to all curves. The vertical offset is dependent on the current and supply voltage.

### B. Discussion

The resulting dependencies of  $dV/dt$  against temperature, load current and supply voltage are shown with the experimental measurements in figs. 12 and 13. There is gentle curvature to the dependencies evident in the calculated curves that is not shown in the measured values.

The values for the calculated charge extraction capacitance  $C_O$  are shown in fig. 14. This varies from approximately 16 nF at 300 V, 10 A and  $-40^\circ\text{C}$ , to 36.5 nF at 160 V, 50 A and  $125^\circ\text{C}$ . As expected, this increases with current and temperature, but decreases with voltage since the depletion layer width  $W_{d2}$  increases with voltage. The ratio  $C_O/(g_m\tau_G)$  is plotted in fig. 15. Values for this ratio range from 1.24 at 160 V, 50 A and

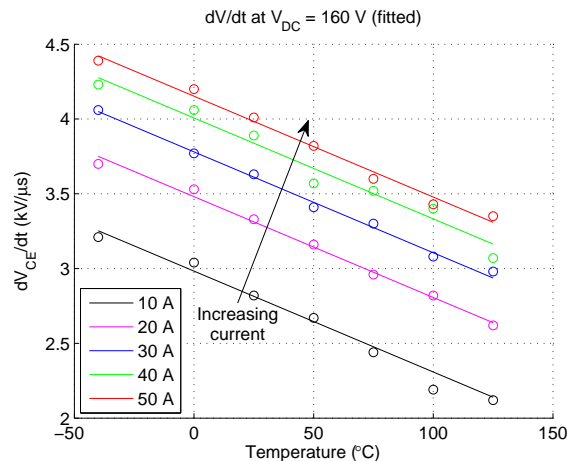


Fig. 9. Measured  $dV/dt$  values and linear fitted curves against temperature for varying load currents at a supply voltage of 160 V.

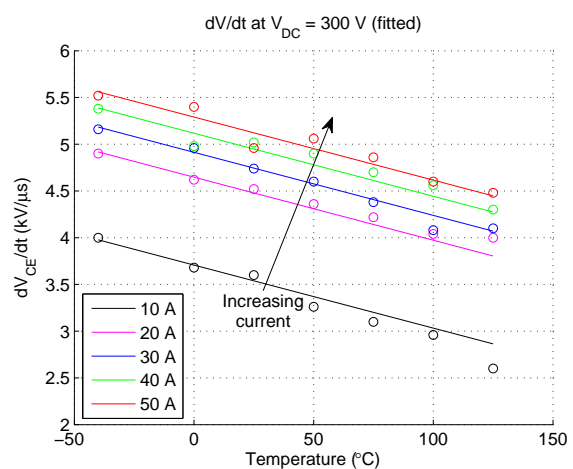


Fig. 10. Measured  $dV/dt$  values and linear fitted curves against temperature for varying load currents at a supply voltage of 300 V.

$-40^\circ\text{C}$ , to 3.07 at 300 V, 10 A and  $125^\circ\text{C}$ . This shows that the charge extraction capacitance  $C_O$  is comparable to the  $g_m\tau_G$  product in determining the  $dV/dt$  in phase 3 of turn-off, although it becomes less significant at higher currents as  $g_m$  increases more than  $C_O$ . This suggests that the charge extraction capacitance is limiting the  $dV/dt$  to a similar extent as, or more than, just the gate feedback alone.

The comparison of predicted and measured  $dV/dt$  in figs. 12 and 13 shows that the prediction in equation (20) generally fits the measured  $dV/dt$  well. There is some discrepancy at low currents. The reason for this is unclear, although the trend of results is in agreement. This is not an issue, however, if the  $dV/dt$  curves against temperature and current are obtained experimentally and used as a look-up table for estimating the device temperature from the  $dV/dt$ . Indeed, the practically linear variation of  $dV/dt$  with temperature may make the look-up table implementation simpler. Furthermore, because the supply voltage  $V_{DC}$  will typically be fixed in a voltage source converter, the maximum  $dV/dt$  will usually be at the same voltage. Since the gate resistance  $R_G$  and supply voltage

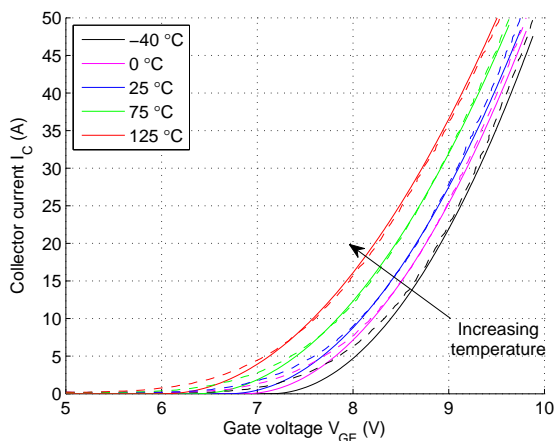


Fig. 11. IGBT transfer characteristics at varying temperature. Dotted: experiment, solid: fitted curves using equation (15).

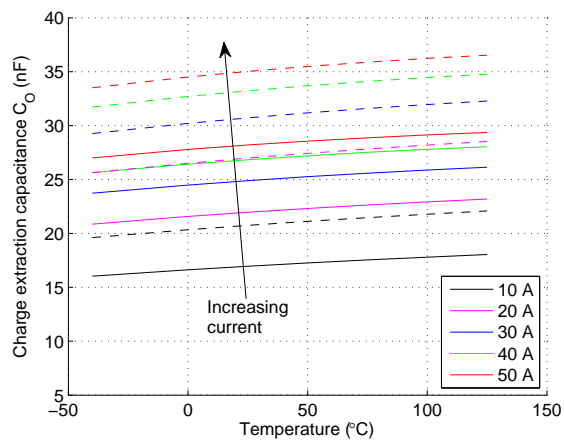


Fig. 14. Variation in charge extraction capacitance  $C_O$  with temperature, load current and supply voltage. Dotted: 160 V, solid: 300 V.

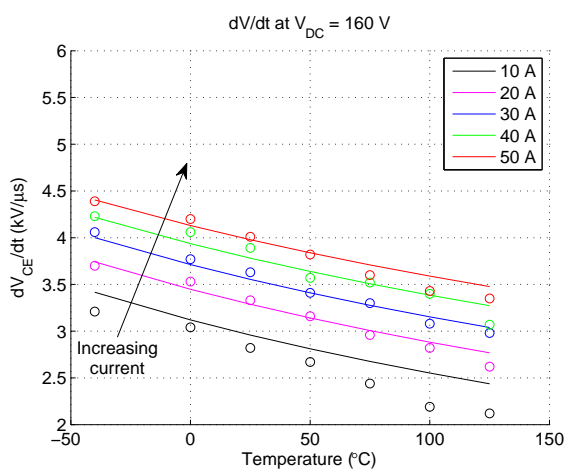


Fig. 12. Modelled dependence of  $dV/dt$  on temperature at a supply voltage of 160 V, shown for different load currents.

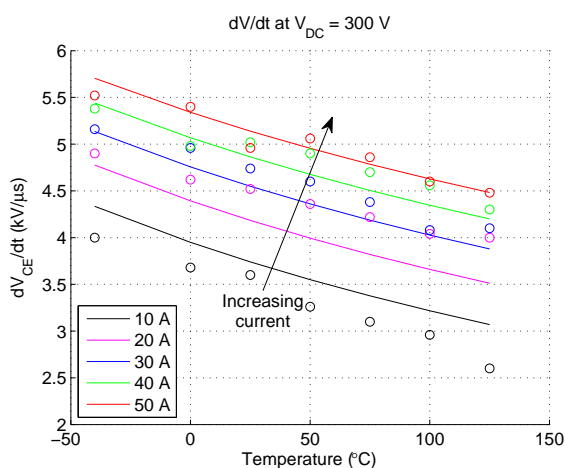


Fig. 13. Modelled dependence of  $dV/dt$  on temperature at a supply voltage of 300 V, shown for different load currents.

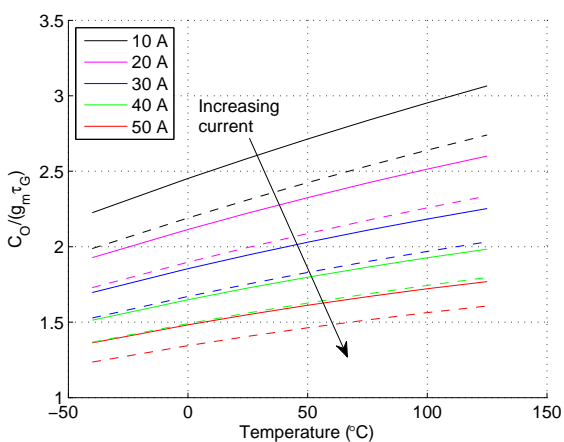


Fig. 15. Variation in ratio  $C_O/(g_m \tau_G)$  with temperature, load current and supply voltage. Dotted: 160 V, solid: 300 V.

$V_{DC}$  are fixed, the only dependencies that need to be tracked with converter operation are the junction temperature  $T_j$  and collector current  $I_C$ , equal to the load current  $I_L$  until the end

of phase 1-3.

Here the values for  $\alpha$  and  $a_i$  were both 0.5. It is logical that they are similar or the same; indeed the carrier density at the MOS end of the carrier storage region is not zero in a planar IGBT, and to a large extent is determined by the intercell area ratio  $a_i$  [32], [33].

This method may also be used as an additional means to check the value for  $h_p$  and its temperature dependence exponent  $k$  if all other parameters are known. The temperature dependency of  $h_p$  was also found to give the best fit with  $k = 0.5$ . This is much less than the value of 2.5 suggested for an abrupt junction by [34] and agrees with the assumption made in [35]. This deviation from the expression for an abrupt junction is to be expected, since a typical NPT IGBT typically has a shallow P emitter (anode) implanted into an N- substrate, known as a transparent emitter. This results in a significant variation in the emitter recombination, hence the temperature dependency will be different from that of an abrupt junction. This suggests that further work is needed in this area to derive a formal temperature dependency for  $h_p$  valid for emitters



found in NPT and soft punch-through/field-stop devices.

The  $dV_{CE}/dt$  in phase 3 also affects the rate of current fall  $dI_C/dt$  in phase 4, by virtue of the necessity to reduce the current in the stray inductance. A higher  $dV_{CE}/dt$  takes the voltage higher while the current falls, speeding its fall. This further reduces the total turn-off time of the IGBT.

## V. CONSEQUENCES OF DV/DT DEPENDENCY

### A. Use of $dV/dt$ for Temperature Estimation

As shown in figs. 7 and 8, the resulting increase in turn-off time  $\Delta t$  arising from the  $dV/dt$  change is approximately 50 ns for a temperature increase from 25 °C to 125 °C for the device studied. This is small relative to the switching period, typically in the range of 20  $\mu$ s to 1 ms for IGBT converters. However it may be detected by harmonic identification methods outlined in [21], which shows that the  $dV/dt$  is indeed a useful method in sensing the IGBT temperature.

There is, of course, the option of measuring the  $dV/dt$  directly from the switching waveforms. Although the details are beyond scope of this paper, such a method would be feasible using a capacitor to sense the  $dV/dt$ . Since the load current during any switching cycle is known in a typical converter – often from a current sensor providing control of the current – the maximum  $dV/dt$  at turn-off is then the only measurement required to estimate the IGBT temperature. The look-up table would be easily implemented in the converter controller, whether it is a DSP or FPGA. Real-time cycle counting as in [10] could then form an estimate of the remaining lifetime of the converter, based on the actual device temperature history observed.

### B. The Role of $dV/dt$ in Dynamic Avalanche

In high-voltage IGBTs there is a greater chance than in low-voltage IGBTs of dynamic avalanche during turn-off [36], [37]. This occurs when the collector voltage  $V_{CE}$  is rising towards the supply voltage  $V_{DC}$ . At high voltages the electric field at the drift region/P-well junction is sufficient to initiate avalanche, with the generated electrons flowing through the depletion layer from the the P-well to the remaining CSR. There is negligible avalanche in the intercell region of the device. Indeed, the ability of the impact ionisation to supply the shrinking CSR with sufficient electron current allows the MOS channel to turn off, with the gate voltage  $V_{GE}$  falling below the threshold voltage  $V_{TH}$ . This may also be seen from the point of view of the reduction in MOS channel current,  $\Delta I_{ch}$ : if the hole current becomes too high and hence the electron current too low, then  $\Delta I_{ch}$  is large. With fewer electrons in the region of the channel, more holes flow through the P-well and high-field region instead and thus increase the rate of impact ionisation. The removal of current from the MOS channel requires that all remaining current – both hole and electron – flows through the P-well. This phenomenon reduces  $dV_{CE}/dt$  as  $V_{CE}$  approaches the supply voltage due to the extra charge resulting from carriers generated by impact ionisation.

The discussion in [37] notes that the onset of dynamic avalanche is not solely determined by the  $I$ - $V$  switching locus

passing through the RBSOA curve, but also dependent on the gate resistance  $R_G$ . However, it does not explain *how* the gate resistance affects the onset of avalanche. The relationships in equations (13) and (20) complete the analysis of dynamic avalanche. For high-voltage IGBTs with ratings above 4.5 kV, the resulting  $dV/dts$  are very large. In order to achieve these values of  $dV/dt$ ,  $\Delta I_{ch}$  must be very large. This is especially the case since for such IGBTs the base doping  $N_B$  is small, giving a large value for  $C_O$ . This value of  $\Delta I_{ch}$  tends to reduce the MOS channel current to zero before  $V_{CE}$  reaches the supply voltage and, since the voltage and thus maximum electric field in the depletion layer are high, it forces the avalanche current to flow. Only by choosing a sufficiently high value of  $R_G$ , thus increasing  $\tau_G$ , is the  $dV/dt$  reduced so that  $\Delta I_{ch}$  is smaller and hence the MOS channel does not turn off. It should be noted that some high-voltage IGBTs are capable of undergoing dynamic avalanche safely during turn-off [38] and smaller values of  $R_G$  may be used as such to reduce the turn-off switching losses.

## VI. CONCLUSIONS

A theoretical closed-form expression has been derived here for the IGBT collector voltage  $dV/dt$  during IGBT turn-off. It has been shown that the  $dV/dt$  is limited by both the gate circuit – including the gate resistance and gate-collector (Miller) capacitance – and the level of stored charge in the lightly-doped base (dirft) region. Consequently the  $dV/dt$  is affected by temperature, the load current and the collector voltage.

Experimental measurements have been taken, and the theoretical expression has been shown to follow the experimental observations closely at higher currents. The result is a complete understanding of the mechanism of this phase in the IGBT switching process, and the role of the temperature-dependent device parameters in determining the  $dV/dt$  at turn-off. Additionally, it has been shown that the  $dV/dt$  is critical in controlling the onset of dynamic avalanche in high-voltage IGBTs.

The consequence of the temperature dependency of the IGBT collector voltage  $dV/dt$  is its potential use as a means of detecting the junction temperature of the IGBT, which is beneficial in condition monitoring of power devices in converter applications.

## ACKNOWLEDGEMENTS

The authors would like to thank Lynton Mogridge of Somerford Consulting, Carl Johnstone of National Grid PLC and Roger Critchley of Alstom Grid for their helpful suggestions and advice.

## APPENDIX I – PREVIOUS WORK ON DV/DT

The process of charge extraction and rise in  $V_{CE}$  is analysed in references [23], [24]. Both give similar expressions for the  $dV/dt$ , dependent on the “instantaneous current”  $i$  which forces the depletion layer expansion and rise in collector voltage. That in [23] is:

$$i = qAp_0 \frac{\sinh\left(\frac{1}{L_a} \sqrt{\frac{2\varepsilon V_{CE}}{qN_T}}\right)}{\sinh\left(\frac{W_B}{L_a}\right)} \sqrt{\frac{\varepsilon}{qN_T V_{CE}}} \frac{dV_{CE}}{dt} \quad (23)$$

$$N_T = N_B + \frac{\beta_{PNP} I_C}{(1 + \beta_{PNP}) q A v_{sat}}. \quad (24)$$

$p_0$  is the excess carrier density in the on-state at the anode PN-junction.  $N_T$  is the effective doping level, taking account of the carrier flow through the depletion region.  $I_C$  is the collector current, which is practically constant at the load current  $I_L$  during phase 3 of turn-off.  $\beta_{PNP}$  is the gain of the internal PNP transistor in the IGBT,  $v_{sat}$  is the carrier saturation velocity,  $A$  is the active device area,  $q$  is the electron charge and  $\varepsilon$  is the permittivity of silicon. This may be simplified by assuming that  $L_a \gg W_B$ , which results in the sinh terms being small:

$$\sinh\left(\frac{1}{L_a} \sqrt{\frac{2\varepsilon V_{CE}}{qN_T}}\right) \approx \frac{1}{L_a} \sqrt{\frac{2\varepsilon V_{CE}}{qN_T}}, \quad (25)$$

$$\sinh\left(\frac{W_B}{L_a}\right) \approx \frac{W_B}{L_a}, \quad (26)$$

$$i \approx \frac{qAp_0 \sqrt{\frac{2\varepsilon V_{CE}}{qN_T}} \sqrt{\frac{\varepsilon}{qN_T V_{CE}}}}{\frac{L_a W_B}{L_a}} \frac{dV_{CE}}{dt}. \quad (27)$$

This then gives the same expression as in [24]:

$$i = \frac{\varepsilon Ap_0}{W_B N_T} \frac{dV_{CE}}{dt}. \quad (28)$$

This also agrees with the expressions in [22], [39] for the  $dV/dt$ , which is expressed using variables defined here as:

$$i = C_{bcj} \left(1 + \frac{1}{b}\right) \left[1 + \frac{p_0}{6N_B}\right] \frac{dV_{bc}}{dt}, \quad (29)$$

where  $C_{bcj}$  is the P-well depletion layer capacitance and  $V_{bc} \approx V_{CE}$  is the P-well depletion layer voltage. In [40] it is shown that a similar expression results from the model in [41]. Such expressions for the output capacitance of the IGBT result are also used in small-signal analysis of IGBT switching transients in [42], [43].

In comparison, the displacement capacitance  $C_{dep}$  is given by

$$i_{disp} = \frac{\varepsilon A}{W_d} \frac{dV_{CE}}{dt} = C_{dep} \frac{dV_{CE}}{dt}, \quad (30)$$

$$W_d = \sqrt{\frac{2\varepsilon V_{CE}}{qN_T}}, \quad (31)$$

where  $W_d$  is the depletion layer width. A geometrical split between the collector-emitter capacitance  $C_{CE}$  and the gate-collector (Miller) capacitance  $C_{GC}$  is often applied to  $C_{dep}$  [29], [44].

## APPENDIX II – EMITTER RECOMBINATION

### A. Dependence of Stored Charge on Emitter Recombination

$p_0$  from equations (5,6) is found by solving for the carrier density gradient  $\partial p/\partial x$  at the anode junction:

$$\frac{\partial p}{\partial x} = \frac{1}{2qA} \left( \frac{I_n}{D_n} - \frac{I_p}{D_p} \right), \quad (32)$$

$$I_p = I_C - I_n, \quad (33)$$

$$I_n = qAh_p p_0^2. \quad (34)$$

This gives the following expression for  $p_0$ :

$$p_0 = \frac{D(1-\alpha)}{2h_p W_B} \left( \sqrt{1 + \frac{2h_p W_B^2 I_C}{qADD_p(1-\alpha)^2}} - 1 \right), \\ \approx \sqrt{\frac{bI_C}{qAh_p(b+1)}}, \quad (35)$$

where  $b = \mu_n/\mu_p$  is the ratio of the mobilities, approximately equal to 3 at room temperature.

$h_p$  is the P-emitter recombination parameter, as defined for an abrupt junction in [34], [45] as:

$$h_p = \frac{1}{N_A^-} \coth\left(\frac{W_P}{L_{n(P)}}\right) \frac{D_{n(P)}}{L_{n(P)}}. \quad (36)$$

$D_{n(P)}$ ,  $L_{n(P)} = \sqrt{D_{n(P)}\tau_{n(P)}}$  and  $\tau_{n(P)}$  are the electron (minority) diffusivity, diffusion length and lifetime respectively in the P+ emitter.  $N_A^-$  is the emitter doping level and  $W_P$  is the P+ emitter width. The parameter  $h_p$  is therefore equivalent to the minority saturation current density  $I_{sne}$ , with

$$I_{sne} = qAh_p n_i^2, \quad (37)$$

where  $n_i$  is the intrinsic carrier concentration.  $h_p$  has alternatively been related to the Gummel number  $G$  by  $G = 1/h_p$ , although such a relationship should be used with care [46]. In [47] the effect of varying the Gummel number, i.e.  $h_p$ , on the on-state/switching loss trade-off is studied.

### B. Emitter Recombination through a Buffer Layer

Punch-through and field-stop devices have a relatively highly-doped N-type buffer layer between the P+ anode and N- drift region, which acts to stop the depletion layer from reaching the anode while the voltage across it is still increasing. Typical doping densities of this layer are  $N_H = 10^{16}$ - $10^{17}$  cm<sup>-3</sup>. Due to its high doping, the holes injected across it from the anode into the N-base region act as minority carriers. The buffer layer acts to reduce the injection efficiency of holes into the base region, and reduces the level of stored charge in the base region. Also, the flow of holes from the emitter into the buffer layer is governed by low-level injection due to the relatively high doping level of the buffer layer exceeding the hole (minority) concentration.

Classic analysis for high-gain, low-injection-level bipolar transistors may be used to determine the buffer layer behaviour due its narrow width. Fig. 16 shows the buffer layer in detail. The hole concentration decreases from the P+ emitter towards

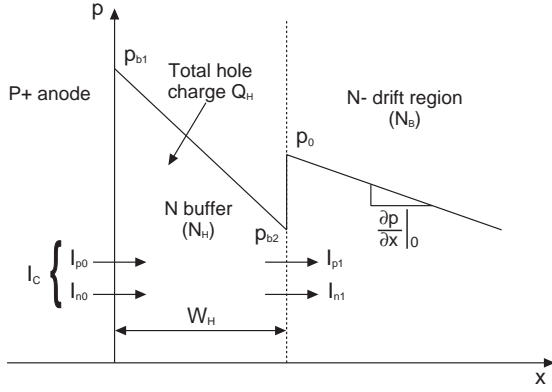


Fig. 16. Simplified characteristics of the hole concentration distribution in the buffer layer region for punch-through and field-stop IGBTs.

the N- drift region. Application of the continuity equation for holes, expressed as a charge control equation, gives:

$$\frac{dQ_H}{dt} = -\frac{Q_H}{\tau_{pH}} + I_{p0} - I_{p1} \quad (38)$$

where  $Q_H$  is the total hole charge, expressed as:

$$Q_H = \frac{qAW_H(p_{b1} + p_{b2})}{2} \quad (39)$$

and  $\tau_{pH}$  is the minority (hole) lifetime in the buffer layer. The gradient of the hole concentration may be approximated as follows, giving the hole current at the N- drift region boundary  $I_{p1}$ :

$$I_{p1} = \frac{qAD_{pH}(p_{b1} - p_{b2})}{W_H} \quad (40)$$

where  $D_{pH}$  is the hole diffusivity in the buffer layer. This linear approximation is valid since the diffusion length  $L_{pH} = \sqrt{D_{pH}\tau_{pH}}$  is much greater than the buffer layer width  $W_H$ . It is also equivalent to the classic bipolar transistor charge equation in reference [48], where the forward and reverse transit times  $\tau_F$  and  $\tau_R$  are equal to  $W_H^2/(2D_{pH})$ :

$$I_{p1} = \frac{qF}{\tau_F} - \frac{qR}{\tau_R} \quad (41)$$

The boundary carrier density  $p_{b1}$  is dependent on the electron recombination current at the anode (equation (42)): note that this is low-level injection due to the high donor concentration  $N_H$ . That at the drift region boundary,  $p_{b2}$ , is related to the ambipolar carrier density at the buffer layer/drift region boundary ( $p_0$ ) by the high-level injection condition (equation (43)).

$$I_{n0} = qAh_p N_H p_{b1} = \frac{I_{sne} N_H p_{b1}}{n_i^2} \quad (42)$$

$$p_{b2} = \frac{p_0^2}{N_H} \quad (43)$$

In the on-state, the rate of change of charge  $dQ_H/dt$  is zero. Substituting  $I_C = I_{n0} + I_{p0}$  and equations (39,40,42,43) into (38) gives an expression for the steady-state charge  $Q_H$ :

$$Q_H = \frac{I_C + qA \left( h_p + \frac{2D_{pH}}{W_H N_H} \right) p_0^2}{\frac{1}{\tau_{pH}} + \frac{2h_p N_H}{W_H} + \frac{2D_{pH}}{W_H^2}} \quad (44)$$

Elimination of  $Q_H$  to get  $I_{p1}$ , the hole current into the drift region, in terms of the collector current  $I_C$  and the ambipolar carrier density  $p_0$  yields the following:

$$I_{p1} = \frac{I_C - \frac{qAW_H p_0^2}{N_H \tau_{pH}} - qAh_p p_0^2}{\frac{W_H^2}{2D_{pH}\tau_{pH}} + \frac{h_p N_H W_H}{D_{pH}} + 1} \quad (45)$$

As the buffer layer width  $W_H$  tends to zero, the expression reduces to the NPT case as expected:

$$I_{p1} = I_C - qAh_p p_0^2 \quad (46)$$

Also, since  $W_H^2/(2D_{pH}\tau_{pH}) \ll 1$ , and typically  $h_p \gg W_H/(N_H \tau_{pH})$ , the electron current into the drift region  $I_{n1} = I_C - I_{p1}$  can be approximated as follows:

$$I_{n1} = \frac{KI_C}{1+K} + \frac{qAh_p p_0^2}{1+K} \quad (47)$$

$$K = \frac{N_H W_H h_p}{D_{pH}} \quad (48)$$

The first term in equation (47) involving  $I_C$  is the extra electron current consisting of electrons attracted to the relatively high N-type doping of the buffer layer. The second term is that expected from recombination into the anode under high-level injection conditions. Assuming that  $I_{n1}$  is given by  $bI_C/(b+1)$ , substitution of this into equation (47) results in an effective emitter recombination parameter  $h_{p(eff)}$ :

$$h_{p(eff)} = h_p \left( \frac{b}{b-K} \right). \quad (49)$$

As the buffer layer width  $W_H$  and doping  $N_H$  increase,  $K$  increases, causing an increase in  $h_{p(eff)}$ , and reduced stored charge injection into the N-base, as expected.

### C. Emitter Recombination Temperature Dependency

The temperature dependency of  $h_p$  is not well-determined. The general dependence may be expressed as follows, with the exponent  $k < 0$  and  $T_0$  typically equals 300 K:

$$h_p = h_{p0} \left( \frac{T_0}{T_j} \right)^k. \quad (50)$$

However the value of  $k$  varies between references, with different values in the range 0.5–2.5 from [34], [35], [49], [50]. It is suggested in [35] that the Gummel number  $G \propto T^{0.5}$ , i.e.  $h_p \propto T^{-0.5}$ , because the minority emitter recombination takes place mainly in the highly-doped part of the emitter where the lifetime, mobility and emitter doping level are independent of temperature. There are further complicating factors too. For punch-through or field-stop IGBTs, the value of  $h_p$  from the P+ emitter is increased by the N-buffer, resulting in an

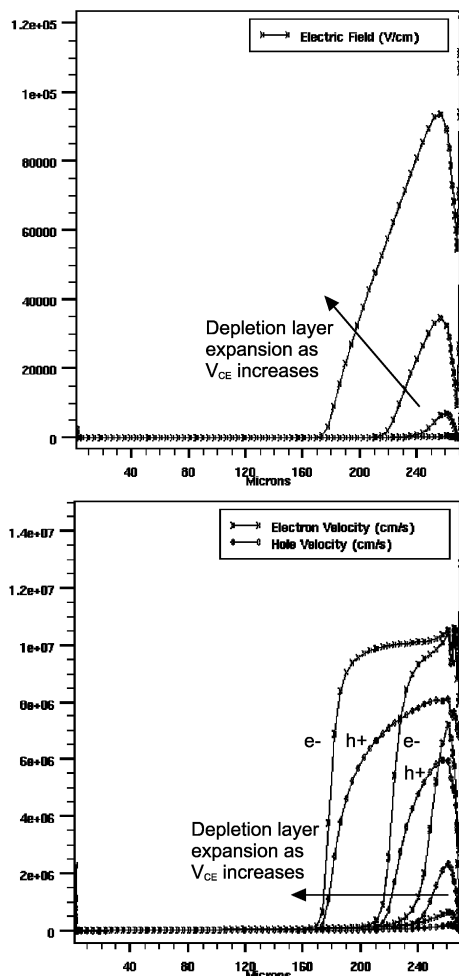


Fig. 17. Carrier velocity within the depletion region of an IGBT during turn-off. Upper: electric field distribution, lower: carrier velocity.

overall  $h_{p(eff)}$  which gives less charge injected into the N-base (see appendix II.B). In addition, a diffused P+ emitter (anode) will give a different expression for  $h_p$  from that of the abrupt junction in equation (36) due to the values of  $N_A^-$ , and therefore  $L_{n(P)}$  and  $D_{n(P)}$ , changing throughout the emitter width; the resulting temperature dependence for a diffused junction will be correspondingly complex. What is clear, though, is that in all cases equation (50) results in decreasing  $h_p$  with increasing temperature, and increased stored charge injection and an increase in  $C_O$ .

### APPENDIX III – EFFECTIVE CARRIER DENSITY IN THE DEPLETION REGION

$N_T$  is the effective carrier density in the depletion region, consisting of the drift region doping level  $N_B$  and the extra carriers arising from the electron and hole currents flowing through the depletion layer:

$$N_T \approx N_B + \frac{|J_p| - |J_n|}{qu_{sat}}, \quad (51)$$

where  $J_p$  and  $J_n$  are the hole and electron current densities respectively. In equation (24), taken from [23], the electron current contribution is omitted, which is incorrect since  $J_n$ , flowing from the MOS channel, forms a significant part of the

total current. However, the assumption in equation (51) that the particle currents in the depletion layer are at saturated velocity  $v_{sat}$  is not entirely accurate. Since holes are less mobile than electrons, but have similar saturation velocities, the electric field required to cause velocity saturation for holes is greater than for electrons. For medium- and high-voltage IGBTs ATLAS simulations show that the hole and electron velocities vary considerably within the depletion layer. Fig. 17 shows this for a 1.7 kV planar NPT IGBT. Using the following equation, as in [29], may give a better estimation of  $N_T$ :

$$N_T \approx N_B + \frac{I_C}{qAv_{sat}}, \quad (52)$$

### REFERENCES

- [1] M. Bartram, I. von Bloh, and R. D. Doncker, "Doubly-fed-machines in wind-turbine systems: Is this application limiting the lifetime of IGBT-frequency-converters?" in *PESC Conf. Rec.*, Aachen, June 2004, pp. 2583–2587.
- [2] S. Watson, B. Xiang, W. Yang, P. Tavner, and C. Crabtree, "Condition monitoring of the power output of wind turbine generators using wavelets," *IEEE Trans. Energy Conversion*, accepted for publication.
- [3] D. McMillan and G. Ault, "Quantification of condition monitoring benefit for offshore wind turbines," *Wind Engineering*, vol. 31, no. 4, pp. 267–285, 2007.
- [4] A. Bryant, P. Mawby, P. Palmer, E. Santi, and J. Hudgins, "Exploration of power device reliability using compact device models and fast electro-thermal simulation," *IEEE Trans. Industry Applications*, vol. 44, no. 3, pp. 894–903, May 2008.
- [5] D. Hirschmann, D. Tissen, S. Schröder, and R. D. Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," in *PESC Conf. Rec.*, Jeju, June 2006.
- [6] L. Wei, J. McGuire, and R. Lukaszewski, "Analysis of PWM frequency control to improve the lifetime of PWM inverter," in *ECCE Conf. Rec.*, San Jose, September 2009.
- [7] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," in *ECCE Conf. Rec.*, San Jose, September 2009.
- [8] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters - a review," *IEEE Trans. Power Electronics*, 2010, accepted for publication.
- [9] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics," *IEEE Trans. Reliability*, vol. 58, no. 2, pp. 271–276, June 2009.
- [10] M. Musallam and C. Johnson, "Real-time compact thermal models for health management of power electronics," *IEEE Trans. Power Electronics*, vol. 25, no. 6, pp. 1416–1425, June 2010.
- [11] M. Ciappa, F. Carbognani, P. Cova, and W. Fichtner, "A novel thermomechanics-based lifetime prediction model for cycle fatigue failure mechanisms in power semiconductors," *Microelectronics Reliability*, vol. 42, pp. 1653–1658, 2002.
- [12] U. Scheuermann, "Reliability of pressure contacted intelligent integrated power modules," in *ISPSD Conf. Rec.*, Santa Fe, June 2002.
- [13] Y.-S. Kim and S.-K. Sul, "On-line estimation of IGBT junction temperature using on-state voltage drop," in *IAS Conf. Rec.*, St Louis, October 1998, pp. 853–859.
- [14] D. Barlini, M. Ciappa, A. Castellazzi, M. Mermet-Guyennet, and W. Fichtner, "New technique for the measurement of the static and of the transient junction temperature in IGBT devices under operating conditions," *Microelectronics Reliability*, vol. 46, pp. 1772–1777, 2006.
- [15] D. Barlini, M. Ciappa, M. Mermet-Guyennet, and W. Fichtner, "Measurement of the transient junction temperature in MOSFET devices under operating conditions," *Microelectronics Reliability*, vol. 47, pp. 1707–1712, 2007.
- [16] H. Chen, V. Pickert, D. Atkinson, and L. Pritchard, "On-line monitoring of the MOSFET device junction temperature by computation of the threshold voltage," in *PEMD Conf. Rec.*, Dublin, April 2006, pp. 440–444.
- [17] A. Ammous, B. Allard, and H. Morel, "Transient temperature measurements and modeling of IGBTs under short circuit," *IEEE Trans. Power Electronics*, vol. 13, no. 1, pp. 12–25, January 1998.

- [18] M. Musallam, P. Acarnley, C. Johnson, L. Pritchard, and V. Pickert, "Estimation and control of power electronic device temperature during operation with variable conducting current," *IET Circuits, Devices & Systems*, vol. 1, no. 2, pp. 111–116, April 2007.
- [19] M. Musallam, C. Johnson, C. Yin, C. Bailey, and M. Mermet-Guyennet, "Real-time life consumption power modules prognosis using on-line rainfall algorithm in metro applications," in *ECCE Conf. Rec.*, Atlanta, September 2010, pp. 970–977.
- [20] R. Krümmner, T. Reimann, G. Berger, J. Petzoldt, and L. Lorenz, "On-line calculation of the chip temperature of power modules in voltage source converters using the microcontroller," in *EPE Conf. Rec.*, Lausanne, 1999.
- [21] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant, and P. Mawby, "Condition monitoring solder fatigue in a power module by inverter harmonic identification," *IEEE Trans. Power Electronics*, submitted for review.
- [22] A. Hefner and D. Blackburn, "An analytical model for the steady-state and transient characteristics of the power insulated-gate bipolar transistor," *Solid-State Electronics*, vol. 31, no. 10, pp. 1513–1532, 1988.
- [23] F. Calmon, J. Chante, B. Reymond, and A. Senes, "Analysis of the IGBT  $dv/dt$  in hard switching mode," in *EPE Conf. Rec.*, vol. 1, Seville, 1995, pp. 234–239.
- [24] A. Ramamurthy, S. Sawant, and B. Baliga, "Modeling the  $dv/dt$  of the IGBT during inductive turn off," *IEEE Trans. Power Electronics*, vol. 14, no. 4, pp. 601–606, July 1999.
- [25] W. Feiler, W. Gerlach, and U. Wiese, "On the turn-off behaviour of the NPT-IGBT under clamped inductive loads," *Solid-State Electronics*, vol. 39, no. 1, pp. 59–67, 1996.
- [26] "Web address: <http://www.silvaco.com/>," ATLAS is part of Silvaco's TCAD software.
- [27] A. Bryant, Y. Wang, S. Finney, T.-C. Lim, and P. Palmer, "Numerical optimization of an active voltage controller for high-power IGBT converters," *IEEE Trans. Power Electronics*, vol. 22, no. 2, pp. 374–383, March 2007.
- [28] P. Jeannin, D. Frey, and J. Schanen, "Sizing method of external capacitors for series association of insulated gate components," in *EPE Conf. Rec.*, Graz, September 2001.
- [29] P. Palmer, E. Santi, J. Hudgins, X. Kang, J. Joyce, and P. Eng, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE Trans. Power Electronics*, vol. 18, no. 5, pp. 1220–1229, September 2003.
- [30] A. Bryant, X. Kang, E. Santi, P. Palmer, and J. Hudgins, "Two-step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and PIN diode models," *IEEE Trans. Power Electronics*, vol. 21, no. 2, pp. 295–309, March 2006.
- [31] C. Jacoboni, C. Canali, G. Otiaviani, and A. A. Quaranta, "A review of some charge transport properties of silicon," *Solid-State Electronics*, vol. 20, pp. 77–89, 1977.
- [32] L. Lu, A. Bryant, E. Santi, J. Hudgins, and P. Palmer, "Physics-based model of planar-gate IGBT including MOS side two-dimensional effects," *IEEE Trans. Industry Applications*, accepted for publication.
- [33] W. Feiler, W. Gerlach, and U. Wiese, "Two-dimensional analytical models of the carrier distribution in the on-state of the IGBT," *Solid-State Electronics*, vol. 38, no. 10, pp. 1781–1790, 1995.
- [34] H. Schlagenotto and W. Gerlach, "On the effective carrier lifetime in p-s-n rectifiers at high injection levels," *Solid-State Electronics*, vol. 12, pp. 267–275, 1969.
- [35] A. Zekry, "The dependence of diffusion length, lifetime and emitter Gummel number on temperature and doping," *Archiv für Elektrotechnik*, vol. 75, pp. 147–154, 1992.
- [36] P. Rose, D. Silber, A. Porst, and F. Pfirsch, "Investigations on the stability of dynamic avalanche in IGBTs," in *ISPSD Conf. Rec.*, Santa Fe, June 2002, pp. 165–168.
- [37] T. Ogura, H. Ninomiya, K. Sugiyama, and T. Inoue, "Turn-off switching analysis considering dynamic avalanche effect for low turn-off loss high-voltage IGBTs," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 629–635, April 2004.
- [38] M. Rahimo, A. Kopta, S. Eicher, U. Schlapbach, and S. Linder, "Switching-self-clamping-mode "SSCM", a breakthrough in SOA performance for high voltage IGBTs and diodes," in *ISPSD Conf. Rec.*, Kitakyushu, May 2004, pp. 437–440.
- [39] A. Hefner, "An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electronics*, vol. 5, no. 4, pp. 459–468, October 1990.
- [40] A. Githiari, "The design of semiconductor switches for high voltage applications," Ph.D. dissertation, University of Cambridge, Cambridge, UK, 1996.
- [41] R. Kraus, P. Türkes, and J. Sigg, "Physics-based models of power semiconductor devices for the circuit simulator SPICE," in *PESC Conf. Rec.*, Fukuoka, 1998, pp. 1726–1731.
- [42] P. Palmer and J. Joyce, "Circuit analysis of active mode parasitic oscillations in IGBT modules," *IEE Proc. - Circuits Devices Systems*, vol. 150, no. 2, pp. 85–91, April 2003.
- [43] A. Githiari and P. Palmer, "Analysis of IGBT modules in the series connection," *IEE Proc. - Circuits Devices Systems*, vol. 145, no. 5, pp. 354–360, October 1998.
- [44] A. Hefner, "An investigation of the drive circuit requirements for the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electronics*, vol. 6, no. 2, pp. 208–219, April 1991.
- [45] A. Herlet, "The forward characteristic of silicon power rectifiers at high current densities," *Solid-State Electronics*, vol. 11, pp. 717–742, 1968.
- [46] H. Schlagenotto and H. Maeder, "Spatial composition and injection dependence of recombination in silicon power device structures," *IEEE Trans. Electron Devices*, vol. ED-26, no. 3, pp. 191–200, March 1979.
- [47] D. Green, K. Vershinin, M. Sweet, and E. Narayanan, "Anode engineering for the insulated gate bipolar transistor a comparative review," *IEEE Trans. Power Electronics*, vol. 22, no. 5, pp. 1857–1866, September 2007.
- [48] R. Dutton and Z. Yu, *Technology CAD: Computer Simulation of IC Processes and Devices*. Boston: Kluwer Academic Publishers, 1993.
- [49] A. Hefner, "A dynamic electro-thermal model for the IGBT," *IEEE Trans. Industry Applications*, vol. 30, no. 2, pp. 394–405, March 1994.
- [50] L. Mussard, P. Tounsi, P. Austin, G. Bonnet, J.-M. Dorkel, and J. Saiz, "Power component models with thermally dependent parameters for circuit simulator," in *EPE Conf. Rec.*, Toulouse, September 2003.



**Angus Bryant** (S'02–M'06) received the M.Eng. degree in electrical and information sciences and the Ph.D. degree in power electronics from Queens' College, Cambridge University, Cambridge, U.K., in 2001 and 2005, respectively. He was a Research Fellow at the School of Engineering, University of Warwick, Coventry, U.K., where he worked on power device modelling. He became an Assistant Professor at the University of Warwick in 2007. Since 2010 he has been with Convertteam UK Ltd, where he is involved with design of low- and

medium-voltage drives.

His main interests are semiconductor device modelling, simulation and characterization of power electronic systems, power module reliability and thermal modelling, and optimization and testing of power electronic systems under realistic loading conditions.



**Shaoyong Yang** (M'06) received B. Eng and M.Eng degrees in Electrical Engineering from Shandong University in 1996 and China Electric Power Research Institute in 1999 respectively. He received a PhD in power electronics at University of Birmingham in 2005. He joined the University of Warwick in 2007. His main interests are power electronics reliability, cryogenic power electronics, power electronics application in power system and renewable systems, power system analysis and distribution generation.

Dr. Yang is a recipient of China Science and Technology Advancement Prize (silver), 2003.



**Philip Mawby** (S'85–M'86–SM'01) graduated and received the B.Sc. and Ph.D. degrees in Electronic and Electrical Engineering from the University of Leeds, U.K., in 1983 and 1987, respectively. During his Ph.D., partly carried out at the GEC Hirst Research Centre, Wembley, U.K., he studied GaAs/AlGaAs heterojunction bipolar transistors for high-power radio frequency applications.

In 2005, he joined the University of Warwick, Coventry, U.K., as Chair of Power Electronics. Before that, he was with the University of Wales, Swansea, U.K. for 19 years and held the Royal Academy of Engineering Chair for power electronics, where he established the Power Electronics Design Center, which has been involved in a whole range of areas relating to power electronics and interaction with SMEs in Wales as well as larger international companies. He has been internationally recognized in the area of power electronics and power device research. He was also involved in the development of device simulation algorithms, as well as optoelectronic and quantum-based device structures. He has authored or coauthored more than 70 journal papers and 100 conference papers. His current research interests include materials for new power devices, modeling of power devices and circuits, and power integrated circuits.

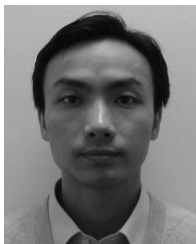
Prof. Mawby has been involved in many international conference committees, including the International Symposium on Power Semiconductor Devices, the European Power Electronics, the Bipolar/BiCMOS Circuits and Technology Meeting, and the European Solid-State Device Research Conference. He is a Chartered Engineer, a Fellow of the Institution of Engineering and Technology, and a Fellow of the Institute Physics. He is a Distinguished Lecturer for the IEEE Electron Devices Society.



**Peter Tavner** (SM'08) received an M.A. degree in engineering sciences from Cambridge University, U.K., in 1969 and a Ph.D. degree from Southampton University, U.K., in 1978.

Currently, he is a Professor of New and Renewable Energy at the School of Engineering and Computing Science, Durham University, U.K. He was the Group Technical Director of FKI Energy Technology, Loughborough, U.K. His research interests include electrical machines for the extraction of energy from renewable sources and their connection to electricity systems, electromagnetic analysis, the application of condition monitoring to electrical systems, and the use of converters with electrical machines.

Prof. Tavner received the Institution Premium Award of the Institution of Electrical Engineers, U.K.



**Dawei Xiang** received the Ph.D. degree in electrical engineering from the College of Electrical Engineering, Chongqing University, Chongqing, China, in 2006. From October 1999 to September 2000, he was an M.Sc. exchange student at the University of Electrocommunications, Tokyo, Japan.

From January to December 2004, he was a Visiting Scholar at Durham University, Durham, U.K., where he has been a Research Associate since 2007. His current research interests include the development of condition monitoring methods for power electronics reliability improvement, analysis and control of power electronics applied in drive systems, power systems, and renewable energy systems.



**Patrick R. Palmer** (M'87) received the B.Sc. and Ph.D. degrees in electrical engineering from the University of London, London, U.K., in 1982 and 1985, respectively. He joined the faculty of the Department of Engineering, University of Cambridge, Cambridge, U.K., in 1985, and that of St. Catharines College, Cambridge, in 1987. He became an Associate Professor in the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada, in 2004, and a Reader in electrical engineering at the University of Cambridge, in 2005. He is currently with the Centre for Advanced Photonics and Electronics, Department of Engineering, University of Cambridge. His research is mainly concerned with the characterization and application of high-power semiconductor devices, computer analysis, and simulation and design of power devices and circuits, and as well as fuel cells. He has extensive publications in his areas of interest. He is the holder of two patents. Dr. Palmer is a Chartered Engineer in the U.K.

Cambridge, in 2005. He is currently with the Centre for Advanced Photonics and Electronics, Department of Engineering, University of Cambridge. His research is mainly concerned with the characterization and application of high-power semiconductor devices, computer analysis, and simulation and design of power devices and circuits, and as well as fuel cells. He has extensive publications in his areas of interest. He is the holder of two patents. Dr. Palmer is a Chartered Engineer in the U.K.



**Li Ran** (M'98–SM'07) received the Ph.D. degree in power systems engineering from Chongqing University, Chongqing, China, in 1989.

Currently, he is the Lecturer in Electrical Power and Control, School of Engineering, University of Durham, Durham, U.K. His research interests include application of power electronics in power systems and renewable energy systems such as wave and wind energy converters.

Dr. Ran received the Stanley-Gray Award from the Institute of Marine Engineers, London, U.K., in 1999, for his work on interconnection of offshore oil rigs. He is a member of the IEEE Power Electronics, Industry Applications, and Power Engineering Societies.