Investigation of Body-Tie Effects on Ion Beam Induced Charge Collection in Silicon-On-Insulator FETs using the Sandia Nuclear Microprobe.

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Silicon-on-insulator (SOI) technology exhibits three main advantages over bulk silicon technology for use in radiation environments. (1) SOI devices are immune to latchup, (2)the volume of the sensitive region (body) and hence total charge collection per transient irradiation is much reduced in SOI devices and (3) the insulating layer blocks charge collection from the substrate (i.e., no funneling effect). This effectively raises the single event upset threshold for the SOI device. However, despite their small active volume SOI devices are still vulnerable to single event effects (SEE). Inherent in the SOI transistor design is a parasitic *npn* bipolar junction transistor (BJT), where the source-body-drain acts as an emitter-base-collector BJT. An ion strike to a floating (not referenced to a specific potential) body can create a condition called snapback, where excess minority carriers in the drain-body junction forward bias the source-body junction, causing the parasitic BJT to turn on and inject current into the drain. Tying the body to the source limits the emitter-base current and reduces the sensitivity of the device to single ion strikes. Unfortunately, the body-tie loses effectiveness with distance due to resistivity, and in regions far enough from the tie the BJT is still in effect.

Using the Sandia nuclear microprobe we have created charge collection maps of SOI FETs which have different body-tie designs. Comparisons of the experiment to DAVINCI simulations are also presented. Effects of body-ties and operating voltage on snap-back thresholds are also presented and predictions of performance in radiation environments made for the different designs.

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1. Introduction

In the last twenty-five years single event effects (SEE) have become a major concern for the operators of microelectronic devices in elevated radiation environments, as is the case for orbital or high altitude electronic systems. The extremely high density of electron-hole pairs created along the path of an incident high-energy ion strike distorts the electric fields in a semiconductor device in a manner which extends the depletion region well into the substrate of the device. This in turn causes large amounts of charge to be collected from a relatively long section (on the order of tens of micrometers) of that path via both drift and diffusive collection mechanisms. This is the well-known "funnel effect" first described nearly twenty years ago [1] and illustrated in Fig. 1a. At the circuit level this ion-induced charge can cause various problems including a change of memory state (single event upset or SEU), latchup (SEL) or even permanent damage ("hard" failures) such as gate rupture (SEGR) [2].

A very popular and efficient method of "hardening" semiconductors against SEE is to reduce the volume from which ion-induced charge can be collected through the use of silicon-on-insulator (SOI) technologies[3]. In these technologies the active regions of the semiconductor are fabricated in a thin, top layer of silicon which is separated from the silicon substrate by a buried insulating layer, most commonly silicon dioxide (sapphire is also used). The thickness of the active film region determines the SOI transistor mode of operation: fully depleted, partially depleted or "bulk-like". Fig. 2a shows a typical partially depleted n-channel SOI MOSFET (metal-oxide-silicon field effect transistor). The top (active) silicon region is generally the thickness of the original wafer (150-300 nm) and the heavily doped source and drain regions extend the entire depth of the silicon to border directly upon the buried oxide. The buried oxide is generally on the order of 300 nm thick. While the mode of

preparation of the buried oxide is important for total radiation dose effects, it is not pertinent to SEE which only depend upon the geometry and doping of the electrically active top silicon region. This particular technology also employs shallow trench isolation to reduce lateral parasitic bipolar effects in the CMOS inverter structure. In this type of SOI transistor the gate voltage does not deplete the entire depth of the active region underneath the gate (known as the "body" region), the conductive channel being created only at the top of the body film – hence the name "partially depleted" SOI (PD-SOI).

One of the benefits of this design for mitigating SEE is illustrated in Fig. 1b which shows and ion strike to a PD-SOI transistor. In contrast to bulk silicon (Fig. 1a), the insulating buried oxide layer does not allow charge generated in the substrate to be collected by the electrically active junctions in the thin top region of the device. The only electrons collected are those actually produced within the top silicon region. This order of 50x reduction in charge collection depth from about 10 μm in bulk silicon to a few hundred nm in PD-SOI should result in a much higher SEU threshold (a measure of the amount of charge deposition needed to cause SEU) for SOI technology when compared to bulk silicon [4,5].

A second benefit of SOI design is the reduced area of p-n junctions in the transistor as compared to bulk designs. The source and drain regions extend the entire depth of the silicon film to the buried oxide and hence have no depletion regions underneath them (as do exist in bulk silicon). The only depletion regions which exist in the PD-SOI transistor are between the body and the heavily doped source and drain regions. This reduced p-n junction area leads to significant reductions in SEU cross-section (a measure of the SEU sensitive area) for SOI integrated circuits (ICs) compared to bulk silicon [5].

Unfortunately, a bipolar charge amplification mechanism (illustrated in Fig. 2b) exists within SOI MOSFETs which may be the limiting factor in their SEU performance. The current generated by an ion strike to the body region of a partially depleted SOI MOSFET can be amplified by the parasitic bipolar junction transistor (BJT) inherent in the device (source/body/drain = emitter/base/collector). In the n-channel SOI transistor case for example the electrons generated in the body by an ion strike are quickly swept into the drain and source leaving the holes behind. These holes raise the body potential (known as Floating Body Effect or FBE) and forward bias the inherent lateral parasitic BJT (n-source/p-body/n-drain). This bipolar effect will amplify the charge collected at the drain by an amount equal to the current gain (β) of the parasitic BJT (i.e., $Q_c = (1+\beta)Q_i$ where Q_c is the charge collected at the drain and Q_i is the charge induced by the incident ion). β increases with decreasing channel length, to the point that very short SOI transistors could be more sensitive to SEU than bulk devices [3]. In an extreme case the FBE can trigger a high current state known as single event snapback (SES – sometimes also known as single transistor latch) if the channel conduction is sustained by regenerative impact ionization effects near the body-drain junction [6,7]. Impact ionization is the creation of more electron-hole pairs by the electron current in the body region. Snapback requires both a minimum potential difference between source and drain (the threshold drain voltage) and a source of electrons in the channel. These can be supplied either by an ion strike or electrically, by operation of the gate to open the channel.

Reduction of FBE is therefore key to achieving SEE resistant SOI technology. To reduce FBE SOI transistors are designed with body ties which hold the body region at a fixed potential (usually the source potential) [3]. Effective body tie design is an extremely

important feature for realizing SEE hard circuits in SOI. Effectiveness of the body-tie increases as separation of the tie from the ion strike location decreases. In this paper we use focused heavy ion microbeam experiments, electrical testing and 3D numerical simulations to study charge collection and snapback in PD-SOI transistors with different body tie parameters. Impact ionization and SES are shown to be important effects in submicron length n-channel SOI devices. The results have implications for radiation hardness testing of SOI technologies.

2. Experiment

A. Test Devices

The devices tested in this report are body-tied, n-channel PD-SOI transistors designed and fabricated at Sandia's Microelectronic Development Laboratory using the 5V CMOS6rs process (includes shallow trench isolation for radiation hardening). The FETs have a drawn gate-length of 0.6 mm, a gate-oxide thickness of 12.5 nm, a buried oxide thickness of ~370 nm and an active silicon region thickness of ~170 nm. Transistors with body channel widths varying from 20 to 1.1 μm were tested.

B. Body Ties

The body ties tested to date are conventional body-tied-to-source (BTS) configurations as illustrated in Fig. 3. The body is independently tied at both ends of the channel by p-type regions which are shorted directly to the source by silicidation. The distance between the p+ body tie and the channel is about 0.5 μm for these CMOS6rs transistors.

C. Measurements

Electrical characterization of snapback in this technology was performed using an HP 4062 parametric analyzer. The drain current (I_{ds}) was measured as the gate voltage (V_{gs}) was

swept from accumulation to depletion (negative to positive for n-channel transistors) at different drain biases (V_{ds}). The lowest V_{ds} for which I_{ds} remained high at zero gate voltage was considered the SES threshold voltage ($V_{ds(SES)}$). Systematic measurements of ion-induced snapback threshold drain voltage as a function of body width were made on the Sandia nuclear microprobe by scanning focused 35 MeV Cl^{+6} or 40 MeV Cu^{+7} ions over the device under test while monitoring the drain power supply current. In additional experiments, I_d and body (I_b) ion-induced transients from 28 MeV Si^{+5} or 40 MeV Cu^{+7} impacts were simultaneously recorded using our time-resolved-ibicc (TRIBICC) system with a 1- GHz TEK680 digitizer (9). This system allows us to scan the ion beam over the FET and collect up to 64x64 point maps of device response while minimizing damage to the active region by (1) storing one complete transient per ion strike, and (2) deflecting the beam away during the period the system requires to digitize and store each transient (~0.1 to 1s).

D. Simulations

Simulations were performed using the three-dimensional device/circuit simulator Davinci (10). Simulations of both transistor response and circuit level SEU have been performed. An impact-ionization model is included in Davinci; its impact upon results was tested by performing some simulations both with and without the model active.

3. Results and Discussions

Results of the SES drain voltage ($V_{ds(SES)}$) threshold measurements are shown in Fig. 4. Included are plots of the measured $V_{ds(SES)}$ versus gate width for 35 MeV Cl^{+6} impacts (surface LET of around 18 MeV-cm^2/mg), 40 MeV Cu^{+7} (surface LET of around 29 MeV-

cm^2/mg) impacts and electrical sweeps. It is interesting to note that the $V_{ds}(SES)$ threshold is extremely similar for all three conditions. This, along with the fact that using 20 MeV C^{+3} ions we were not able to initiate snapback at all in these devices, suggests that SES exhibits saturation behavior; once an ion strike (or electrical opening of the channel) can supply a certain amount of charge to the body region, snapback is initiated. A higher LET particle which deposits more charge will not significantly alter the voltage threshold. This is consistent with electrical response in that once the snapback condition is initiated, raising V_{gs} more does not lower the snapback drain voltage threshold. This finding may have positive implications for future snapback mitigation efforts in that susceptibility to heavy-ion SES may well be predictable with electric testing. Note in Fig. 4 that thresholds predicted using the Davinci simulator for several channel widths also match with experiment. Simulations of devices with other channel widths are pending.

Since the body tie effect is limited by the channel resistance, these transistors should be most sensitive to ion-induced SES at the center of the body, farthest from the contacts at both ends of the channel. Fig. 5 shows a plot of the charge collected at the drain following the ion strike of focused (~1 μm resolution in scan direction) , 40 MeV Cu^{+7} as the beam is scanned across the width of a 0.6x20 μm channel. The drain was biased at 5.3V (above the SES threshold) through a capacitively de-coupled bias tee. Strikes to the center four microns of the body induce SES which result in drain currents on the order of 1 mA . Strikes outside this central region are close enough to the body-ties that the bipolar amplification effect is more limited and regenerative impact-ionization levels are not reached. We have plotted here the charge integrated over 72 ns following the ion strike. In our system the bias tee capacitor is discharged over the course of a microsecond or so, which then draws the drain

bias voltage back below the SES threshold and terminates the snapback current. This is a very useful feature for producing SES maps in a timely manner with the microbeam. Typical "sub-snapback" current transients last on the order of a nanosecond in this system.

The effect of the BTS on the bipolar amplification of Q_I, the charge injected into the body, is illustrated in Fig. 6 for 28 MeV Si^{+5} ion strikes on a 0.6x20 μm device. Q_c, the charge collected at the drain is approximately equal to Q_I near the contact, but is almost twice Q_I for ion strikes near the center of the body at the furthest point from the BTS. As devices scale downward in size the increased bipolar amplification to expected from shorter channel lengths should be mitigated somewhat by the increased effectiveness of body ties due to narrower channel widths.

4. Summary

We have used the Sandia heavy-ion nuclear microprobe to induce single event snapback in SOI transistors. We have measured the inverse effect of distance from the body-tie (i.e. channel width) on SES drain voltage thresholds and bipolar charge amplification in the body region. In the future we will reproduce these type of measurements and simulations on devices with varying gate lengths to check for changing bipolar effects and on Body-Under-Source (BUSFET) tie designs where the source does not extend all the way to the buried oxide and the body contact runs under the entire width of the source. This effectively places the contact much closer to the channel. These devices are predicted to have much better SES resistance.

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Figure Captions

1. Ion penetration of a bulk (a) and an SOI (b) device. In SOI the buried insulating layer prevents charge generated in the substrate from being collected by the junctions of the device. After Colinge (3).

2. (a) Cross-section diagram of a typical partially depleted SOI n-channel transistor. (b) Holes created by an ion strike in the body region raise the body potential relative to the source. This activates the parasitic source/body/drain bipolar transistor which amplifies current to the drain. If the drain voltage is high enough the electrons in the channel can create more e-h pairs at the drain junction by impact ionization.

3. Plan view of test device body ties. The channel is tied at both ends by a single silicide region which forms both the body and source contact. Dotted lines indicate contact regions.

4. Measured and simulated SES threshold drain voltages as a function of gate width for CMOS6rs n-channel transistors. Simulations are for 35 MeV Cl^{+5} ion strikes. The similar threshold values for 40 MeV Cu (LET~29), 35 MeV Cl (LET~17) and electrically-induced SES suggest a saturation behavior to snapback.

5. Drain charge collected from 40 MeV Cu^{+7} strikes at different locations across the width of a 0.6x20 μm body. Due to resistance in the channel the effectiveness of the body-tie at preventing SES diminishes with distance from the contact points at both ends of the body.

6. Drain charge collected versus distance from the body- tie contact. For strikes near the body-tie floating body effects are limited and the bipolar amplification of the charge is reduced.

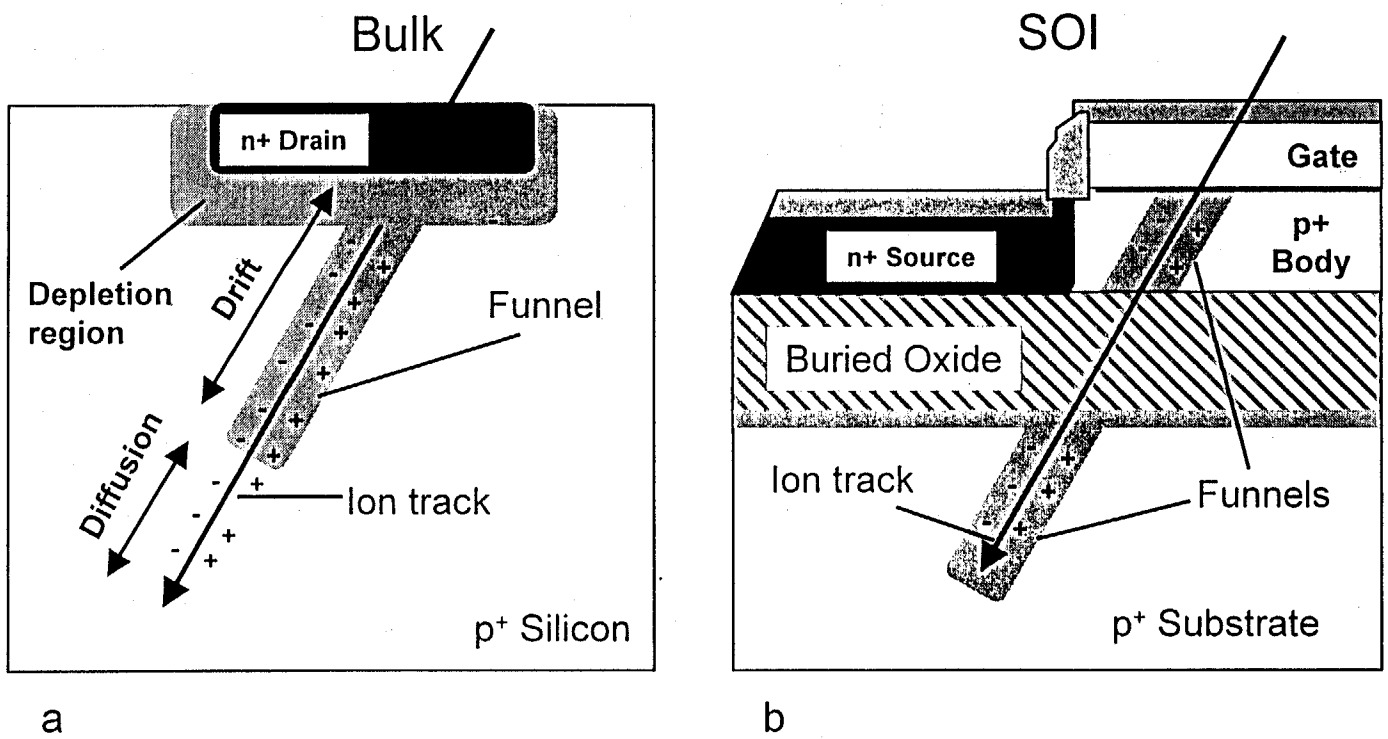
Bulk
n+ Drain
Depletion region
Drift
Funnel
Diffusion
Ion track
p+ Silicon
a
SOI
Gate
p+ Body
n+ Source
Buried Oxide
Ion track
Funnels
p+ Substrate
b

Fig. 1

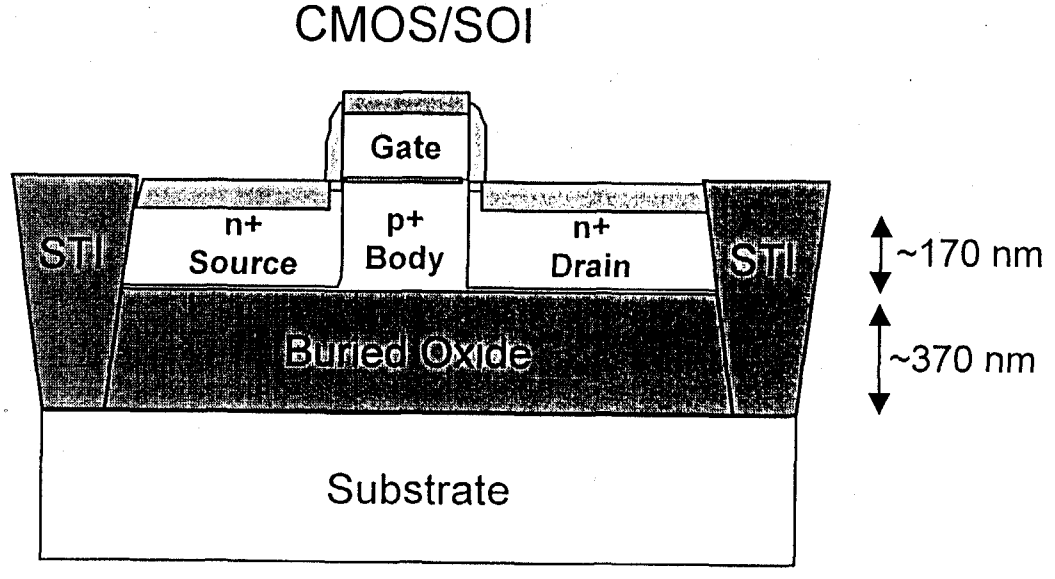
CMOS/SOI
Gate
STI
n+
Source
p+
Body
n+
Drain
STI
Buried Oxide
Substrate
~170 nm
~370 nm

Fig. 2a

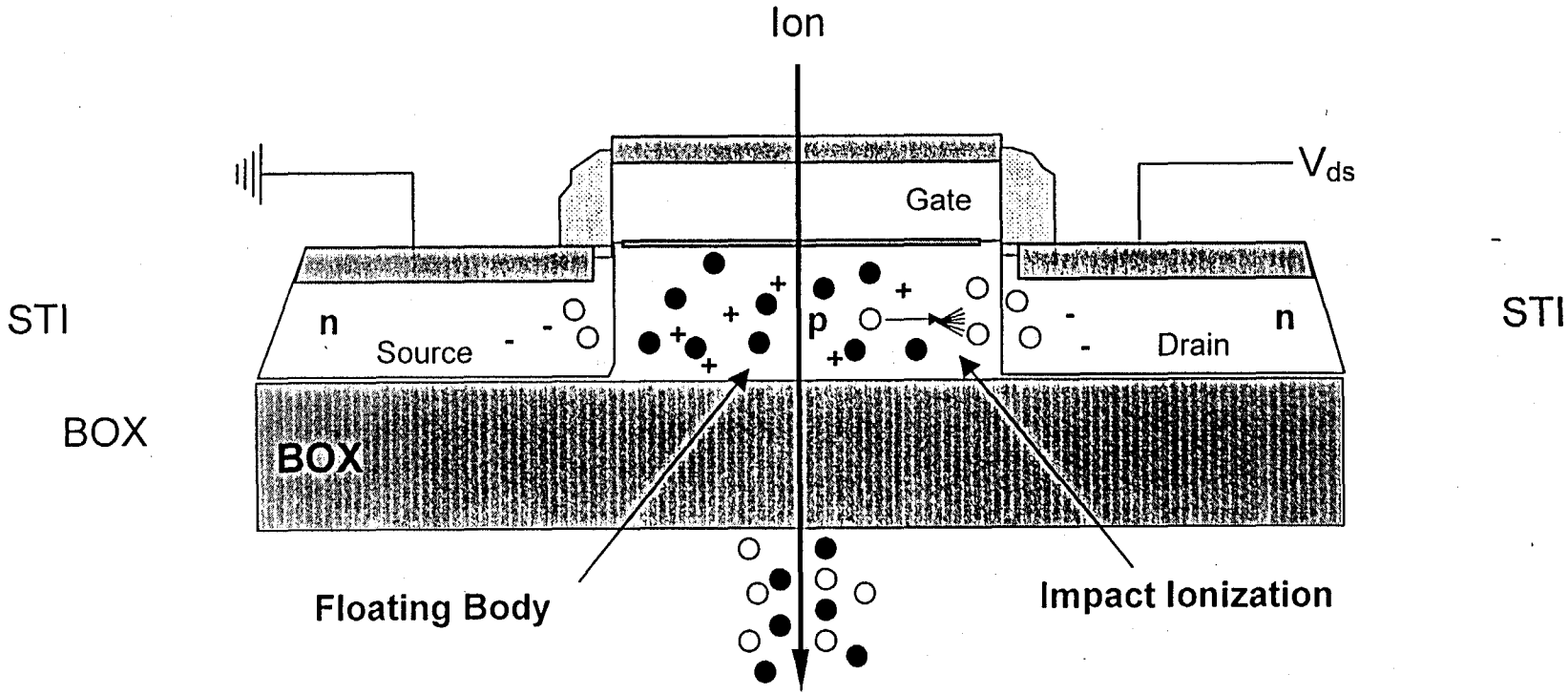
Ion
Gate
V_{ds}
STI
STI
n
Source
p
n
Drain
BOX
BOX
Floating Body
Impact Ionization

Fig. 2b

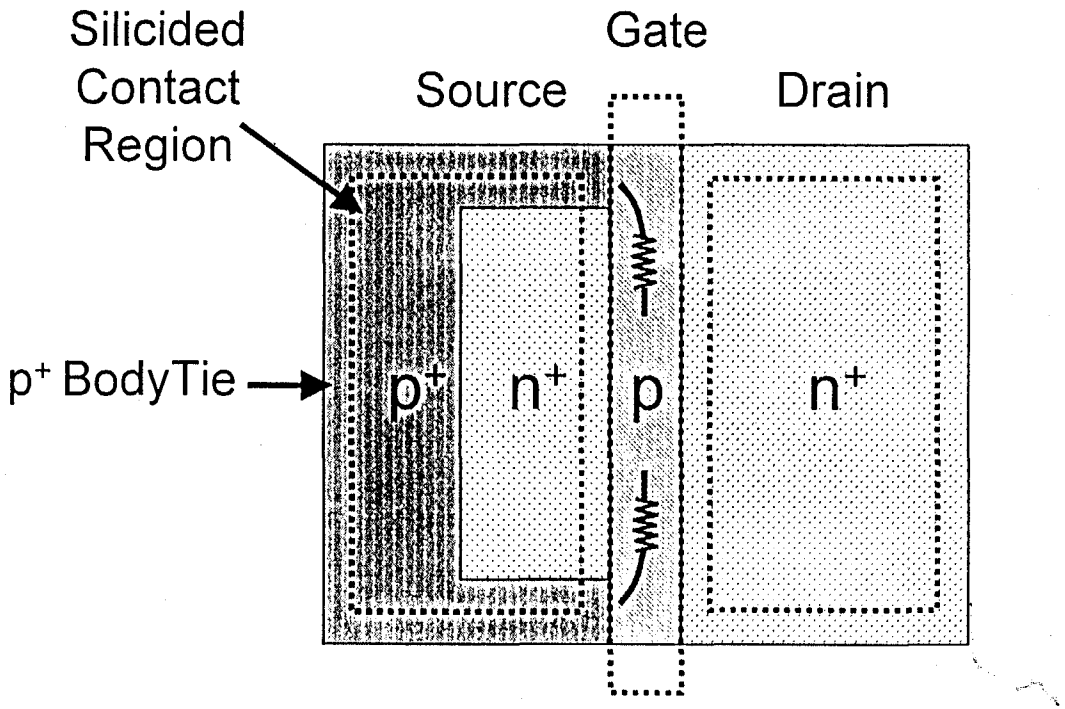

Fig. 3

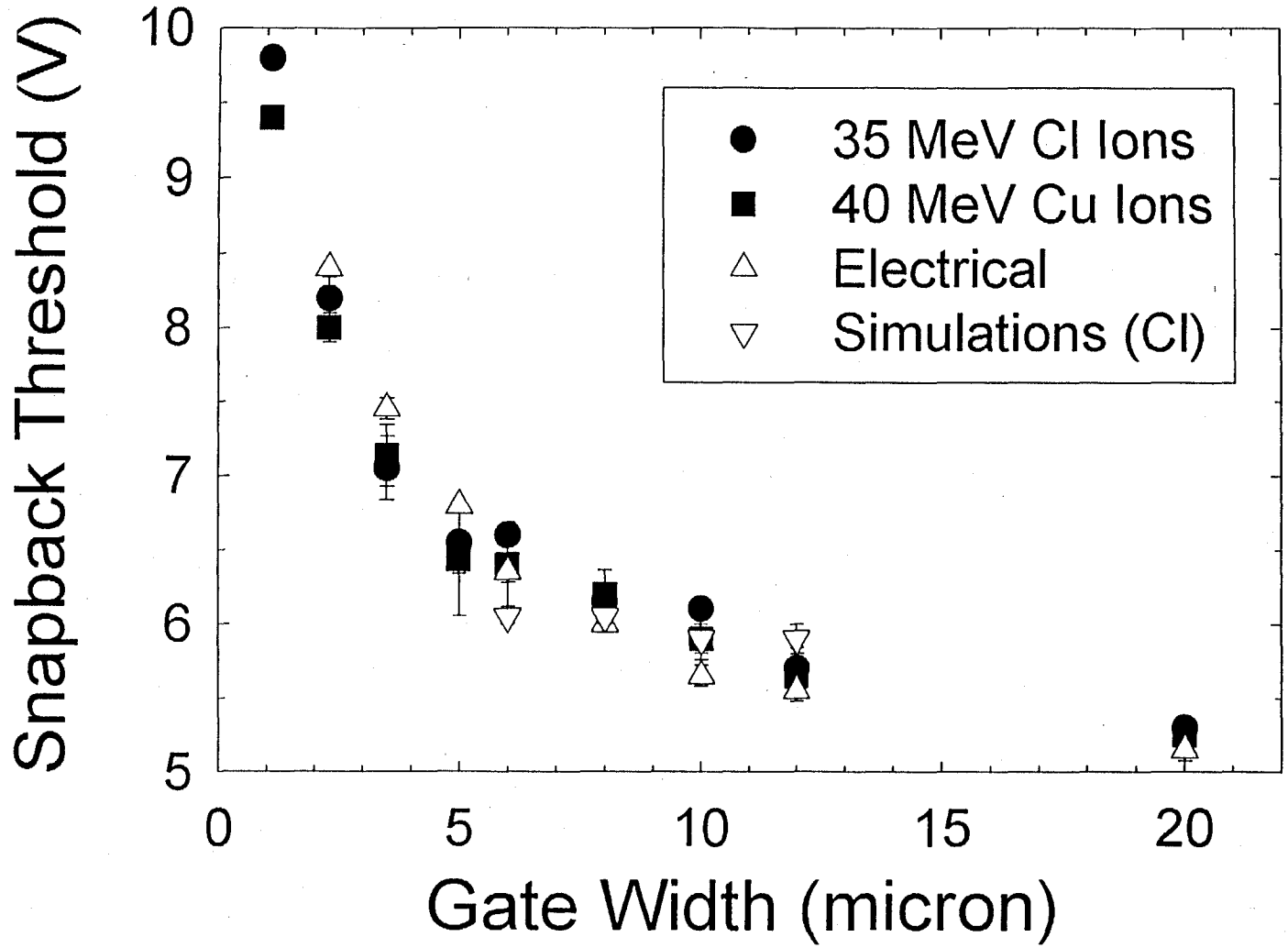
Snapback Threshold (V)
10
9
8
7
6
5
0
5
10
15
20
Gate Width (micron)
35 MeV Cl Ions
40 MeV Cu Ions
Electrical
Simulations (Cl)

Fig. 4

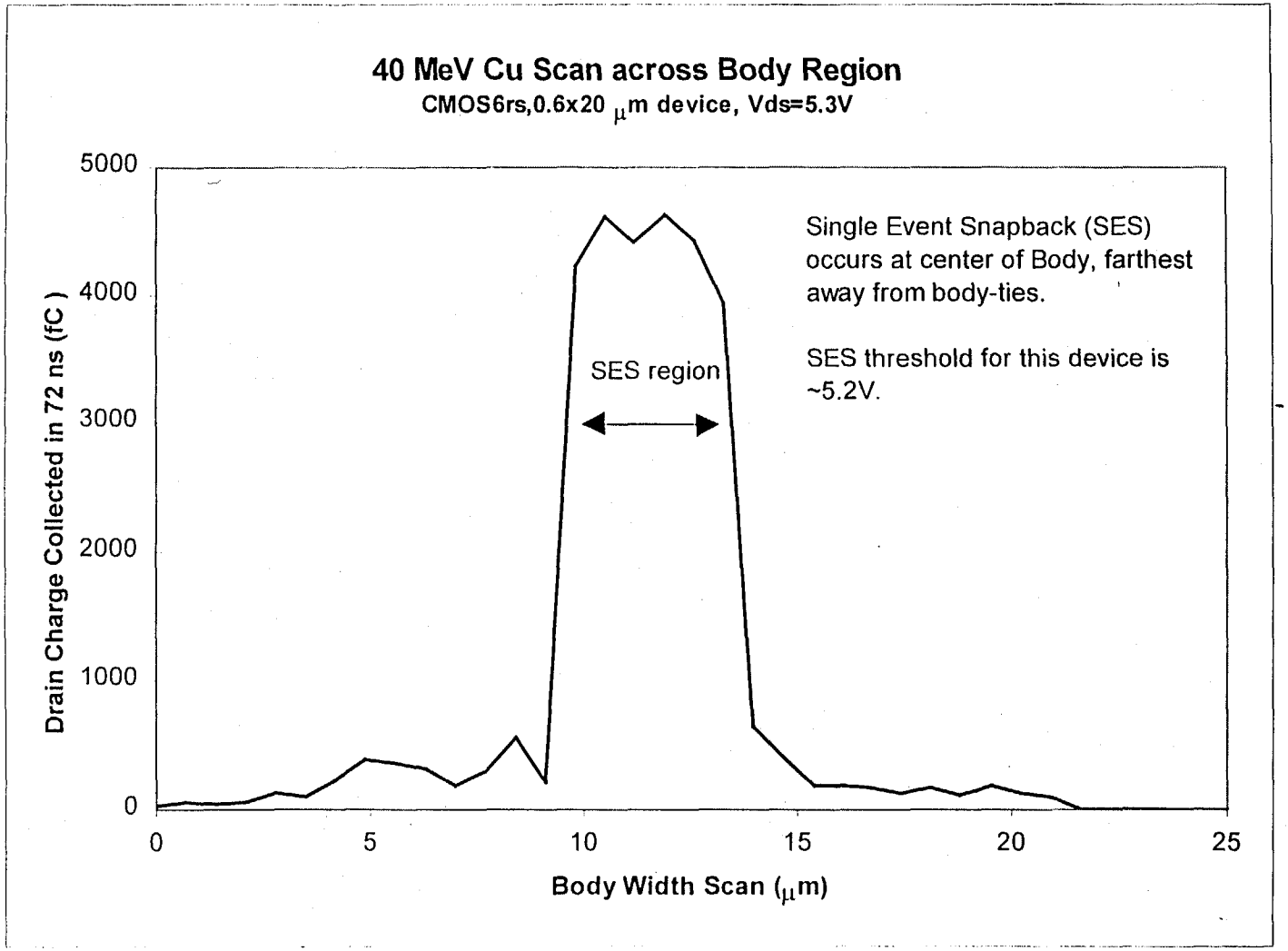
40 MeV Cu Scan across Body Region
CMOS6rs,0.6x20 μm device, Vds=5.3V
Drain Charge Collected in 72 ns (fC)
5000
4000
3000
2000
1000
0
0
5
10
15
20
25
Body Width Scan (μm)
SES region
Single Event Snapback (SES) occurs at center of Body, farthest away from body-ties.
SES threshold for this device is ~5.2V.

Fig. 5

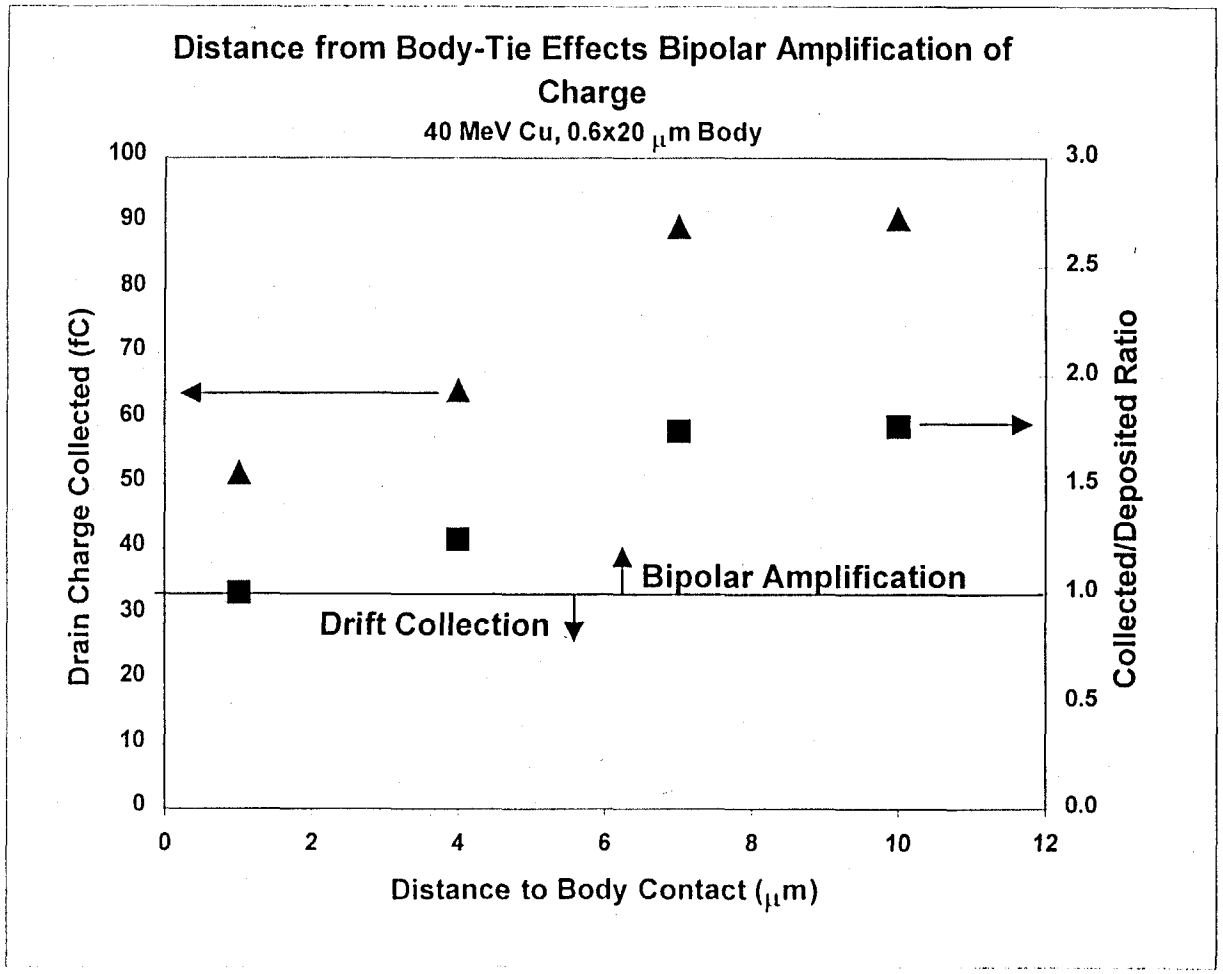
Distance from Body-Tie Effects Bipolar Amplification of Charge
40 MeV Cu, 0.6x20 μm Body
Drain Charge Collected (fC)
Collected/Deposited Ratio
Distance to Body Contact (μm)
Bipolar Amplification
Drift Collection
0
10
20
30
40
50
60
70
80
90
100
0.0
0.5
1.0
1.5
2.0
2.5
3.0
0
2
4
6
8
10
12

Fig. 6