Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation and MOSFET Characteristics

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Purpose

Circuit-level oxide degradation effects on CMOS inverter circuit operation and individual MOSFET behavior is investigated. Individual PMOSFET and NMOSFET devices are assembled off-wafer in the inverter configuration through a switch matrix. A range of gate oxide degradation mechanisms are induced by applying a ramped voltage stress (RVS) of various magnitudes to the input of the inverter. A novel circuit model is used to simulate the voltage transfer curves (VTCs) of degraded inverters. At the transistor level, increased gate leakage currents of nearly eight orders of magnitude are observed, in addition to severely reduced on-currents (> 50 percent reduction), and large threshold voltage (V_{th}) shifts (> 100 mV). At the circuit-level, stress of either polarity results in inverter performance degradation. For the DC characteristics, oxide degradation attributed to limited hard breakdown (LHBD) in the NMOSFET and hard breakdown (HBD) in the PMOSFET, results in decreased output voltage swing (> 260 mV). Under the same conditions, inverter degradation in the voltage-time (V-t) domain exposes much larger changes in performance. For instance, significant increase in the rise time results in the output voltage being pulled up to only 660 mV (V_{DD} = 1.8 V) before switching low. From a circuit reliability viewpoint, it may be possible for subsequent circuit stages to compensate for a few degraded devices, but in high-speed circuits, increased rise/fall and delay times may cause timing issues. Furthermore, increased gate or off-state leakage currents can potentially load previous circuit stages or result in increased power consumption. [*Keywords:* Circuit model, circuit reliability, CMOS, dielectric breakdown, gate oxide reliability, inverter degradation, MOSFEET degradation.]

Introduction

The continued importance of gate oxide breakdown and reliability may be a limiting factor in the future scaling of high performance CMOS integrated circuits [1, 2]. Many studies have been conducted on gate dielectric breakdown of individual MOS capacitors and an increasing number on MOSFETs (for an overview, see [3]). Only a limited number of investigations consider the effects of circuit-level stress on circuit performance and reliability [4-8]. Large integrated circuits with a large number of transistors have been the focus of many of these studies. In complex circuits, such as digital and RF, it has been demonstrated that hard breakdown (HBD) in multiple MOSFETS does not cause total circuit failure, but these circuits remain functional [7, 9]. And although it has been reported that subsequent circuit stages may be capable of compensating for a few degraded devices [7], increased rise/fall and delay times may result in potential timing issues in high-speed circuits. Furthermore, in complex integrated circuits, it may only be possible to examine the effects of stress on the circuit as a whole. Potential circuit reliability issues may be better understood by directly measuring the amount of gate oxide degradation in individual MOSFETs that have been

stressed within a circuit, which is the focus of this study. This is accomplished by stressing simple integrated circuit building blocks (SICBBs) such as transmission gates, current mirrors, and inverters, which are the focus of this study. Therefore, using simple circuits comprised of MOS devices that can be isolated from the circuit and characterized directly, can provide a foundation for understanding gate oxide degradation effects on large-scale circuits

Experimental

PMOSFET and NMOSFET transistors fabricated in a 0.16-µm/1.8-V CMOS technology with gate oxide thickness of 3.2 nm and gate dimensions of 25µm x 25µm are connected in an inverter configuration (Fig. 1) off-wafer via an Agilent E5250A low leakage switch matrix. Characterization and stress tests are performed with an Agilent 4156C Precision Semiconductor Parameter Analyzer, an Agilent 41501B pulse generator, an Agilent Infinium oscilloscope, and a probe station equipped with eight Cascade Microtech DCM positioners enclosed in a Faraday cage.

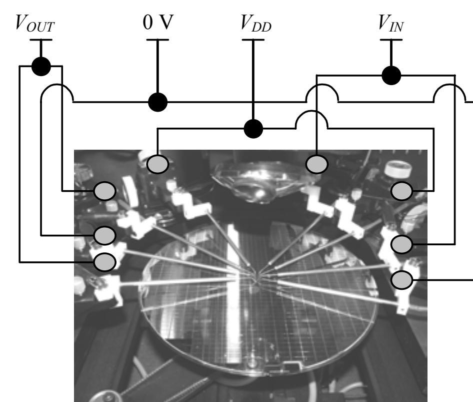


Figure 1. Wafer level inverter configuration for circuit-level stress experiments.

The flow chart in Fig. 2 simplifies the following procedures used during circuit-level stress experiments. The inverter circuits are investigated under both positive and negative stress conditions. A ramped voltage stress (RVS) is applied from input to output with the V_{DD} and GND terminals floating [10], as shown in Fig. 3. The

maximum value of the ramped voltage is varied to induce multiple degrees of gate oxide degradation, which ranged from 0 to +/- 8 V, 0 to +/- 10 V, 0 to +/- 12 V, and 0 to +/- 14 V. The former two RVS ranges have been shown to induce current limited hard breakdown (LHBD) [11, 12] while the latter two RVS ranges were used in an attempt to reproduce the data of [13]. A series of pre- and post-stress tests are conducted on the inverter to examine performance changes

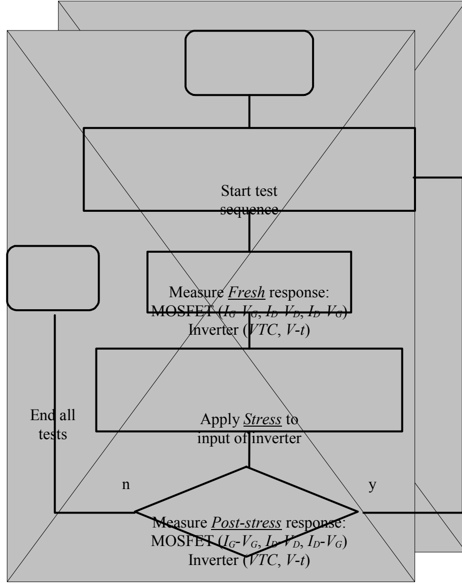


Figure 2. Flow chart.

in the inverter voltage transfer characteristics (VTCs) and voltage-time (V-t) domain characteristics. For inverter performance measurements, the input voltage (V_{IN}), power supply voltage (V_{DD}), test frequency, and duty cycle, were 1.8 V, 2.5 kHz, and 50 percent, respectively. In addition, all inverter leakage currents are monitored, pre- and post-stress, by connecting V_{OUT}, V_{DD}, and GND nodes to 0 V. See [14] for an overview of inverter circuit operation and other parameters discussed in this study.

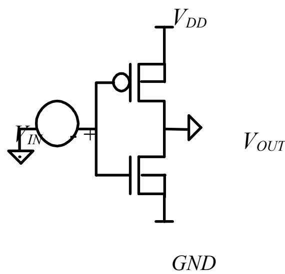


Figure 3. Inverter schematic. voltage source indicates stress was induced from V_{IN} to V_{OUT}.

The type and amount of degradation observed for each MOSFET, as a result of circuit-level stress, are identified by comparing pre- and post-stress gate leakage current versus gate voltage (I_G-V_G) measurements. I_G-V_G measurements are taken with the drain (D), source (S), and bulk (B) terminals at ground potential. The DC parameters selected for examining the effects of degradation on individual MOSFET characteristics before and after circuit-level stress are maximum drain current ($I_{D,MAX}$), on-current (I_{On}), off-current (I_{Off}), subthreshold slope (S). The absolute value of the data is plotted where appropriate.

Proposed Circuit Model

Various circuit models for stressed inverters have been proposed [13, 15]. It was reported [15] that the percolation path at the breakdown spot is primarily composed of phosphorus from the n+-polysilicon gate. This results in the formation of an ohmic contact to the n+ source/drain regions of the NMOSFET. It has been suggested that an ohmic model does not provide a good fit for experimental data of inverters [13] if the degradation mechanism observed is not comparable to hard breakdown (HBD). Furthermore, the diode effect for both transistors may be explained if the percolation path, or at least the contact to drain regions, is intrinsic silicon.

To simulate the operation of degraded inverter VTCs, the circuit model shown in the inset of Fig. 4(a) was used. The model is similar to that in [15]. However, rather than the PMOSFET, a resistor-diode pair is introduced to simulate gate-to-drain breakdown in the NMOSFET and the PMOSFET. The resistors from MOSFET gates (V_{IN}) to sources (V_{DD}, GND) are altered to accommodate the statistical distribution of the post-breakdown resistance of the percolation path. MOSFET threshold voltage shifts are included in the model to provide a closer fit to the experimental results. The Shockley diode equation [16] is given by:

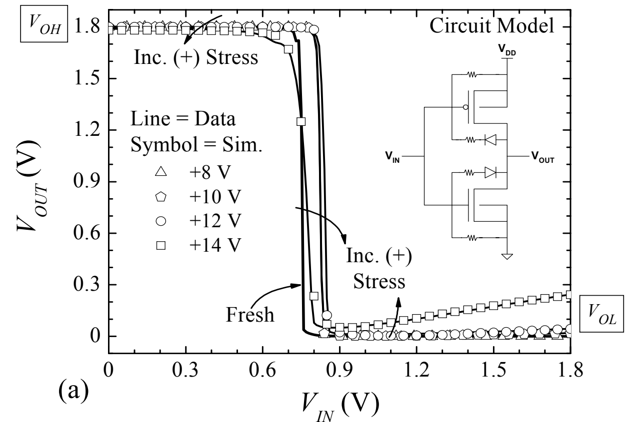
$$I_D = I_S \cdot [\exp(V_D / N \cdot V_t) - 1] \quad (1)$$

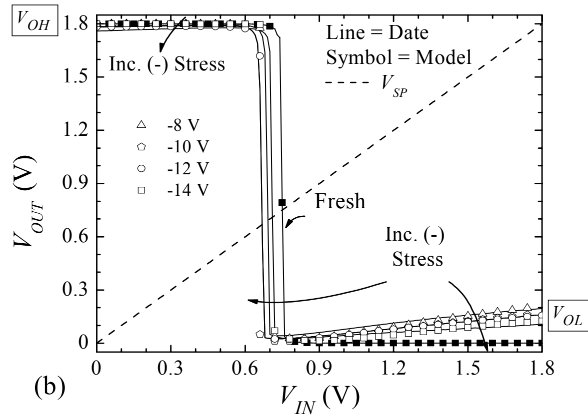
where the parameters are defined as saturation current (I_S), diode voltage (V_D), emission coefficient (N), and thermal voltage (V_t). Adjusting the variable, N, alters the bias voltage at which the diodes begin conducting.

Results

Inverter Performance

Experimental and simulated VTCs for inverters stressed in circuit-level configuration are shown in Fig. 4(a) and (b).



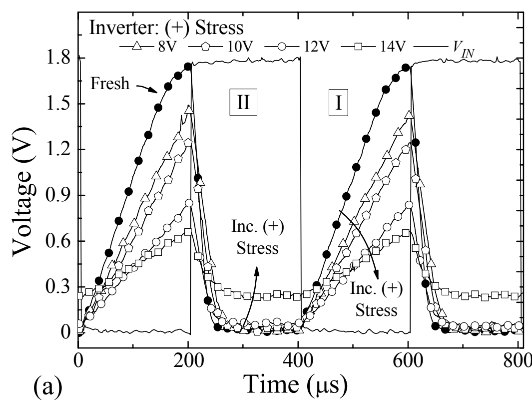


Solid lines represent experimental data and symbols indicate simulated VTCs. In general, as the magnitude of the positive stress increases [Fig. 4(a)], V_{OH} decreases and V_{OL} increases, resulting in decreased inverter output swing.

It is observed from Fig.4(a) that when the devices have suffered the highest degree of LHBD (NMOSFET) and HBD (PMOSFET), a decrease in V_{OH} by as much as 20 mV is observed. The change in V_{OL} is even greater showing an increase of as much as 240 mV. In general, the changes in V_{OL} occur at lower stress voltages than those in V_{OH}. V_{SP} initially increases or shifts right with increasing stress magnitude. At the highest stress voltages, V_{SP} decreases and is similar to that of the fresh inverter.

VTC results for negative circuit-level stress [Fig. 4(b)] are similar, but have slightly different trends. Compared to the positive stress case, V_{OH} and V_{OL} tend to decrease with increasingly negative stress. The change in V_{OH} is typically larger for negative stress than for positive stress, while V_{OL} is typically highest at low stress voltages, and then decreases with increasing stress voltage. V_{SP} tends to shift left and initially decreases with increasing stress magnitude, similar to the response observed in V_{OL}.

From the VTCs alone, it appears that the inverter performance has not been severely degraded at lower stress voltages. However, examining the time-domain behavior reveals otherwise. Shown in Fig. 5 are the time-domain responses, to a 2.5 kHz square wave input, of inverters that have been stressed with a (a) positive RVS and (b) negative RVS.



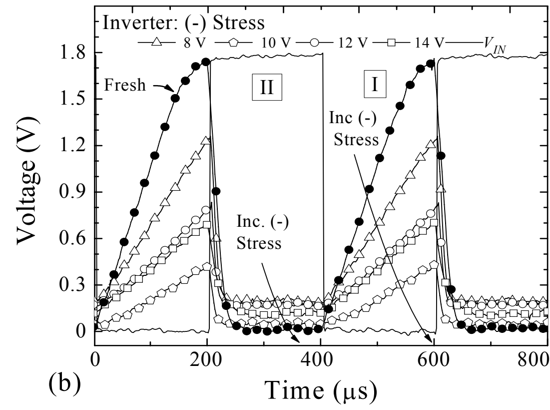


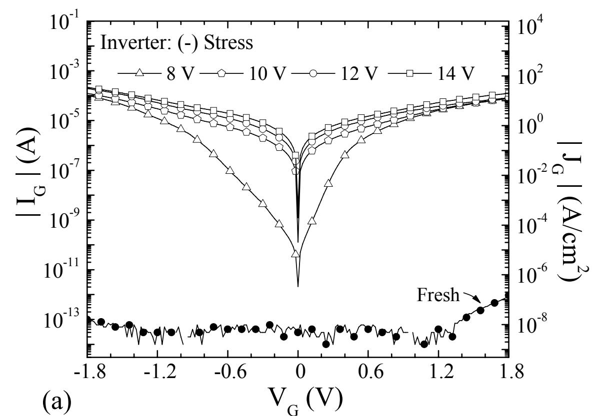
Figure 4. Inverter VTCs following (a) Positive and (b) negative voltage stress

Similar to the VTC operation, the inverter V-t domain describes two areas of interest, which are designated as region I and II. Region I is defined as the rising signal or PMOSFET pull-up portion. Region II corresponds with the falling signal or NMOSFET pull-down portion.

In general, after positive/negative stress, it is observed that as the stress magnitude is increased the inverter voltage output swing in the time domain is significantly decreased. It is interesting to note that the trends in region I and region II follow those trends observed in Fig. 4 for V_{OH} and V_{OL}, respectively, which are attributed to the NMOSFET being degraded to LHBD and the PMOSFET suffering HBD. However, under the same conditions, region I of (a) and (b) shows that $V_{Out,MAX}$ has decreased from 1.8 V fresh to 660 mV/440 mV, respectively. In comparison, V_{OH} decreased from 1.8 V fresh to 1.78 V post-stress. Conversely, for region II of (a) and (b), the voltage magnitude of $V_{Out,MIN}$ is very similar to that observed in V_{OL} from the transfer characteristics.

Unlike region I, which shows that as the stress magnitude is increased (positive or negative) $V_{Out,MAX}$ is significantly decreased, region II shows an opposite behavior for each stress polarity. For instance, in the positive stress case [Fig. 5(a)], $V_{Out,MIN}$ increases with increasing stress magnitude and reaches a maximum of 248 mV (ideal = 0 V). Alternatively, for negative stress [Fig. 5(b)] $V_{Out,MIN}$ increases with decreased stress magnitude to a maximum of 196 mV.

Inverter input leakage currents following (a) negative and (b) positive voltage stress are shown in Fig. 6.



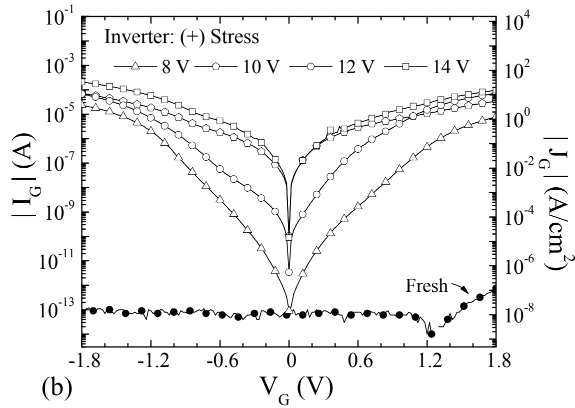


Figure 6. Fresh and post-stress inverter input leakage currents monitored for (a) negative and (b) positive stress experiments.

Various degrees of inverter degradation are observed for both stress polarities. Input leakage current is typically highest at -1.8 V for both cases. Furthermore, leakage currents for negative stress are generally higher at operating conditions (V_G = 1.8 V) where a difference of approximately 20 μA or more is observed, relative to positive stress of equal magnitude.

MOSFET Characteristics

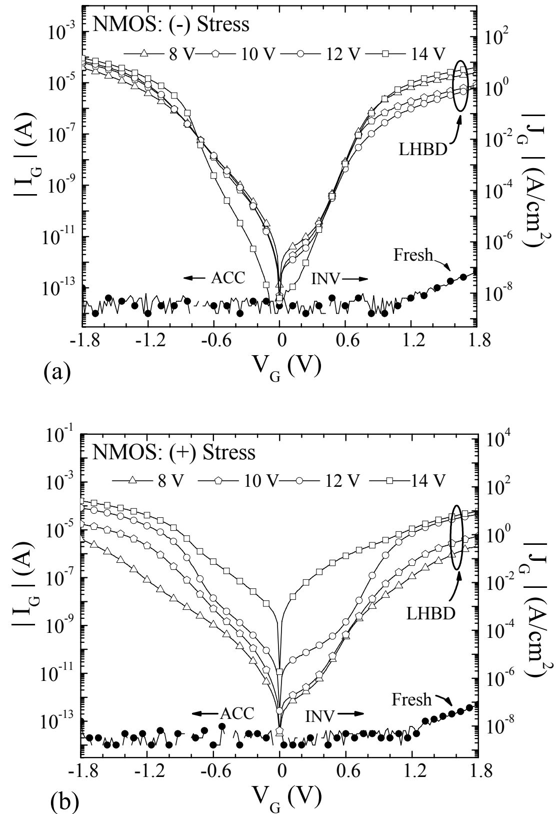
Gate leakage current results following negative and positive stress for the NMOSFET and PMOSFET are shown in Fig 7. In general, as stress magnitude increases, gate leakage current of both the NMOSFET and PMOSFET increases, as would be expected. The relationship between the proposed breakdown mechanism attributed to the leakage current response is not always easily identified, as indicated by the (?) in Fig.7(c) and (d). Typically the NMOSFET suffers limited hard breakdown (LHBD) [11, 12] for all stress voltages, while the PMOSFET is more likely to breakdown to a greater extent at higher stress voltages. In addition, the leakage current for negative stress [(a)/(c)] increases over one order of magnitude at +/- 1.8V, while positive stress [(b)/(d)] increases over two orders of magnitude. Comparison of Fig. 7(b) and (d) reveals that under multiple (+) V stress conditions, the NMOSFET suffers from LHBD while the PMOSFET has undergone HBD. This behavior is present for negative circuit-level stress as well [Fig. 7(a) and (c)]. Various breakdown modes have been induced in the PMOSFET, as indicated by the labels in Fig. 7(d), but similar modes are observed for each device after both positive and negative stress. As the stress magnitude increases, a large range of LHBD is observed, which at times is followed by HBD.

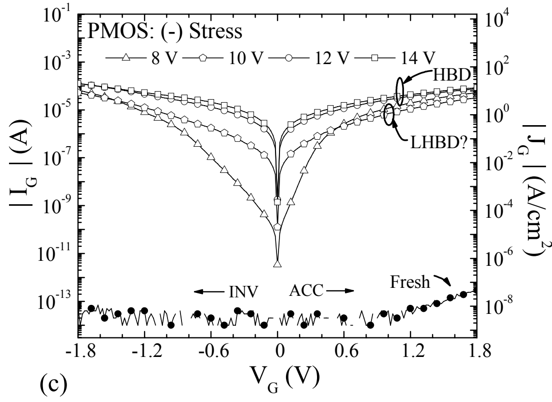
One of the more interesting observations, which is present at varying degrees for both devices under numerous stress conditions, is the difference in initial leakage current magnitude and characteristic between the low (< 0.9 V) and the high (> 0.9 V) voltage regimes. The first trend may be described more clearly by comparing Fig. 7(c) and (d). For the PMOSFET under (-) 8 V stress, the leakage current measured at V_G = 0 V is two orders of magnitude higher than the Fresh characteristic, while for (+) 8 V stress the leakage current at V_G = 0 V is consistent with the Fresh measurement.

The second observation is made relative to the characteristic or shape differences between the low and high voltage regimes. In this case, Fig. 7(b) easily identifies the two regions of interest. For each stress voltage in the range V_G > 0.9 V, their relative shape's are similar and the leakage current begins to level off as it approaches 1.8 V. Conversely, in the low voltage regime, the current may change slopes up to three times before entering the high voltage region, where the current increases more steadily. This behavior appears to be independent of the operating mode, as it present for both accumulation and inversion. However, this behavior is more pronounced in inversion mode, for both the NMOSFET and PMOSFET devices.

The subthreshold characteristics for the NMOSFET and PMOSFET devices following +/- V stress are shown in Fig. 8. The oxide degradation mechanism for each device was determined to be LHBD. It is observed that the subthreshold slope has increased by as much [illegible] the PMOS[illegible]) is observ[illegible] FET. Conve[illegible] T is greater after (+) V stress when compared to the NMOSFET.

Fig. 9 shows the I_D-V_D characteristics for each device after various degrees of (a)/(b) positive and (c)/(d) negative stress. Curves





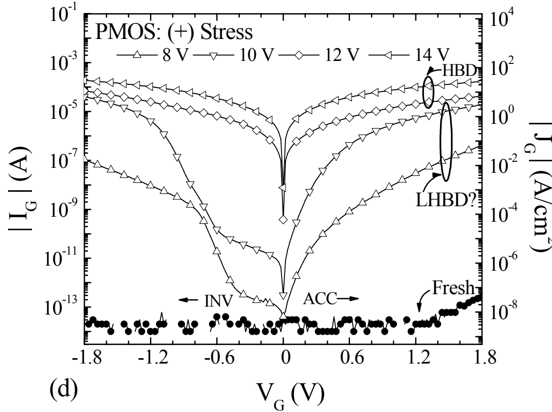


Figure 7. Post-stress I_G-V_G leakage current plots for (a) NMOS (- V), (b) NMOS (+ V), (c) PMOS (- V), and (d) PMOS (+ V) stress.

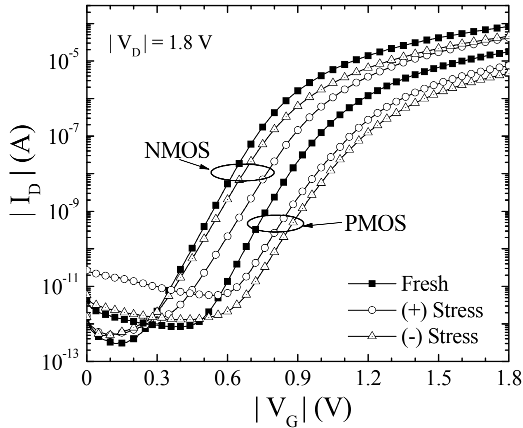


Figure 8. Comparsion of the log I_D-V_G characterstics for NMOS and PMOS devces.

for $|V_{Gate}|$ of 1.8 V are plotted, but the behavior is similar for lower gate voltages. Generally, as stress magnitude increases, a substantial decrease in $I_{D,MAX}$ is observed. However, from Fig. 9 it is apparent that different trends are observed for positive and negative stress. It is interesting to note that Fig. 9(a) and (c) are the result of LHBD in an NMOSFET, while Fig. 9(b) and (d) are the result of both LHBD and HBD in the PMOSFET.

In order to evaluate these results, each plot identifies two areas of interest are identified in each plot. A1 and A2 are designated as the linear and saturation regions, respectively [16]. The relationship between the drain-to-source voltage (V_{DS}), gate-to-source voltage (V_{GS}), and MOSFET threshold voltage (V_{th}) are given for each area in expressions (2) and (3).

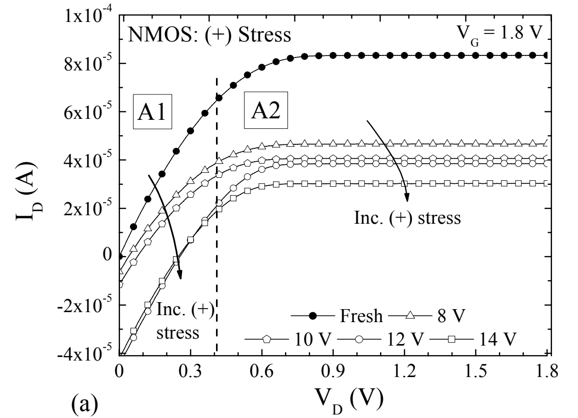
$$V_{DS} \leq V_{GS} - V_{th}, \text{ for A1} \quad (2)$$

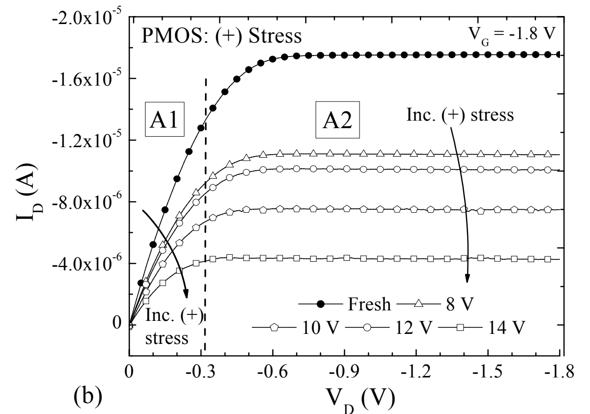
and

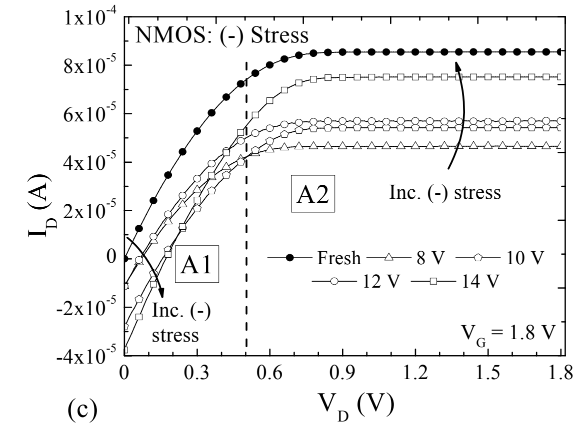
$$V_{DS} \geq V_{GS} - V_{th}, \text{ for A2.} \quad (3)$$

Additionally, region A1 requires that for the MOSFET to be turned "on", $V_{GS} > V_{th}$, otherwise $V_{GS} < V_{th}$ and the device is "off". It is observed from Fig. 9(a) and (b) that regions A1 and A2 follow a similar trend after positive stress of either the NMOSFET or the PMOSFET. Experimental results show that as the magnitude of the stress increases, $I_{D,MAX}$ decreases. However, regions A1 and A2 of Fig. 9(c) and (d) do not follow the same trend. Typically for negative stress, region A1 is similar to the positive stress results, yet the negative results for (c) region A2, indicate that at lower stress magnitudes $I_{D,MAX}$ for the NMOSFET decreases significantly compared to higher stress voltages. A similar trend for $I_{D,MAX}$ is observed for the PMOSFET(d) for stress resulting from HBD.

For a discussion concerning the effects of circuit-level stress on the MOSFET parameters transconductance (g_m) and threshold voltage (V_{th}) refer to [14].







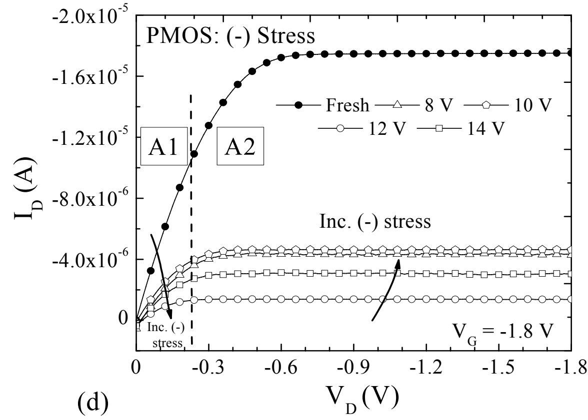


Figure 9. I_D-V_D results indicating $I_{D,MAX}$ degradation for (a) NMOS (+), (b) PMOS (+), (c) NMOS (-), and (d) PMOS (-) stress.

Discussion

Inverter Performance

Both stress polarities induced LHBD and/or HBD (Fig. 7) which resulted in reduced output swing of the inverter VTC (Fig. 4), comparable to observations in [5]. Shifts in inverter V_{SP} are also observed when the inverter is stressed (Fig. 4). As reported in [4], this could be due to interface state generation or charge trapping in the oxide [17], or possibly a combination of both. In general, as the stress magnitude is increased, V_{SP} increases. However, a clear correlation between stress magnitude and the amount of V_{SP} shift is not always apparent.

A link between VTC performance and region II of the V-t response can be seen by comparing V_{OL} (Fig. 4) and $V_{Out,MIN}$ (Fig. 5). The post-stress V-t results following positive and negative circuit-level stress, indicate that $V_{Out,MIN}$ is consistent with V_{OL} for both stress polarities. This may be explained by the difference in response of the NMOSFET to the polarity of the stress in the saturation region (A2) of the I_D-V_D characteristics [Fig. 9(c)]. For increasing negative polarity, a general increase in I_D is observed in the A2 region which should manifest a decrease in V_{OL} [Fig. 4(b)] and $V_{Out,MIN}$ [Fig. 5(b)]. However, the inverse relation is observed. The opposite occurs for positive stress polarity as seen in Fig. 4(a) and 5(a). The opposing circuit responses to changes in polarity may be due to the leakage currents at the various terminals of the inverter. These behaviors are currently being examined.

Unlike $V_{Out,MIN}$, the magnitude of the response for $V_{Out,MAX}$ does not match that of the VTC (Fig. 4 and 5). One particular discrepancy is observed with respect to the rise time. Several factors may attribute to the rise-time increase, such as a decrease in the effective carrier mobility of the PMOSFET due to interface states created during stressing [17], the large area of the devices, or the inverter device ratio being 1:1 (PMOS:NMOS), where a more ideal case would be a ratio of at least 2:1 [16]. Moreover, increased charging time for parasitic capacitances, due to increased leakage currents, may also limit the rise-time. However, if the test frequency is decreased significantly, the final $V_{Out,MAX}$ values approach those of the VTCs.

Perhaps the most important or viable observation is that the time-domain exhibits significant degradation compared to the VTCs under equal amounts of stress. This substantial difference prompts the question, which characteristic would be better suited for evaluating reliability limits for inverters? This study suggests that the time-domain be investigated when examining the effects of oxide degradation in the inverter circuit. When both devices behave more resistively (Fig. 9), the time domain behavior of the inverter will change. Furthermore, if the resistance of the inverter increases, the delay and transition times (t_r and t_f) [14] of the inverter will increase. The relationships between delay and resistance are given by [16]:

$$t_{plh} = (R_p)(C_{tot}) \tag{4}$$

and

$$t_{phl} = (R_n)(C_{tot}) \tag{5}$$

where t_{plh} and t_{phl} are defined as the propagation delay from low-to-high and from high-to-low, R_p and R_n are defined as the effective resistance (resistance between drain and source) of the PMOSFET and NMOSFET, and C_{tot} is the sum of all capacitive components on the out[...]o be underst[...]n is signific[...]ce is not a fa[...] both fresh and degraded devices.

MOSFET Characteristics

Changes in MOSFET parameters such as $I_{D,MAX}$, g_m, and the subthreshold characteristics were observed following circuit-level stressing. When the gate oxide suffers dielectric breakdown under circuit-level stress, gate control over the channel may be severely reduced (Fig. 9). This can alter the polarity of the current in the linear region (A1) thus inhibiting channel inversion. The differences observed in regions A1 and A2, particularly for negative stress, suggest that changes in the threshold voltage are less for lower stress voltages, which results in the degraded device turning on more quickly (steeper slope), thus saturating at a lower current level. Additionally, off-state currents often increase (Fig. 8) which can result in increased power consumption [16].

A range of oxide degradation occurs following circuit-level stress, such as LHBD and HBD. Of particular interest is the evidence that MOSFETs can independently experience different degradation mechanisms while in the inverter configuration [Fig. 7(a) and (c)]. For either polarity, the device suffering a higher degree of oxide degradation (Fig. 8 and 9) may be the dominant cause of circuit failure. Further, MOSFET inversion mode operation (Fig. 9) seems to be more heavily influenced by negative voltage stress, supported by leakage current data in Fig. 7. This suggests that the PMOSFET is influenced more by inversion stress and the NMOSFET by accumulation mode stress.

Comparing the leakage currents of degraded MOSFETs (Fig. 7)

to those of degraded inverters (Fig. 6), similarities between the two are evident. In addition, the trends observed for the low and high voltage regimes are observed in both cases. However, there are some differences that are currently under investigation, which may be attributed to current leakage at the drain, source, and bulk nodes of the devices.

Circuit Model

VTCs of positive and negative stressed inverters (Fig. 4) are fit well by varying a few parameters contained in the model. The development of this model came about after preliminary examination of the individual transistor leakage current components. The data suggests that the drain current is usually lowest and diode-like, whereas the substrate and/or source currents are usually highest and nearly linear (i.e. ohmic). However, these results may vary depending on the MOSFET operation mode being investigated. Consequently, these findings may be a result of the manner in which the inverter is stressed. The ideas presented here are only preliminary and are currently being extended.

It has been reported that in certain digital applications, the gate-to-source leakage current may generate a worst case scenario [6]. For this study, further examination of the leakage current components suggests that gate-to-substrate leakage currents may dominate the total leakage current. In addition to the preliminary analysis of the leakage currents, Spice simulations revealed that only gate-to-drain breakdowns seem to affect the inverter VTCs. Conversely, inverter time-domain performance was shown to be severely degraded when little to no gate-to-drain breakdown was observed (Fig. 5). These discrepancies can potentially be addressed by simulating the voltage-time domain behavior with the model presented in this study, or perhaps by incorporating other circuit elements. To perform this task, additional analysis of all MOSFET leakage currents is required and is currently being investigated.

Conclusion

Circuit-level stress effects on circuit operation and individual transistors were investigated. Circuit stress of either polarity, on the transistor-level, results in increased gate leakage current, decreased $I_{D,MAX}$, decreased g_m and increased V_{th} [14] for the NMOSFET and the PMOSFET. More compelling is the evidence that the NMOSFET and PMOSFET can suffer dissimilar oxide degradation mechanisms while in the inverter configuration.

Simulations of degraded inverter VTCs were accomplished using a new circuit model. Decreased inverter voltage output swing was observed in both the transfer characteristics and the time domain. However, more significant changes were observed with respect to the inverter rise and fall times. Hence, VTC measurements may show negligible inverter degradation; yet, V-t behavior of the inverter may be severely degraded. Consequently, the V-t data, presented for the first time, introduces a new characteristic for digital circuit reliability. Several published reports call for more suitable circuit reliability criterion [6, 7, 10].

In larger circuits, stages subsequent to a degraded SICBB may be able to compensate for adverse SICBB operation [7], however, increased rise/fall times and delays could lead to timing in high speed circuits. Although VTC degradation may be limited, large leakage and off-state currents can be present potentially inducing loading of previous circuit stages and increased power consumption [16]. It seems apparent that further investigation of circuit reliability is prudent.

Acknowledgments

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