Investigation of Electrode Electrochemical Reactions in $CH_3NH_3PbBr_3$ Perovskite Single-Crystal Field-Effect Transistors

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Keywords: field-effect transistor (FET), perovskite, single crystal

Abstract

Metal halide perovskite-based optoelectronic devices, including solar cells and light-emitting diodes, have attracted tremendous research attention globally in the last decade. Due to their potential to achieve high carrier mobilities organic-inorganic hybrid perovskite materials could enable high-performance, solution-processed field-effect transistors (FETs) for next-generation, low-cost, flexible electronic circuits and displays. However, the performance of perovskite FETs is hampered predominantly by device instabilities, whose origin remains poorly understood. Here we study perovskite single-crystal FETs based on methylammonium lead bromide ($MAPbBr_3$) and investigate device instabilities due to electrochemical reactions at the interface between the perovskite and gold source-drain top contacts. Despite forming the contacts by a gentle, soft lamination method we find evidence that even at such "ideal" interfaces a defective, intermixed layer is formed at the interface upon biasing of the device. Using a bottom-contact, bottom-gate architecture we show that it is possible to minimize such a reaction through a chemical modification of the electrodes, and this enables fabrication of perovskite single-crystal FETs with high mobility of up to ~15 cm^2/Vs at 80 K. Our work addresses one of the key challenges towards the realisation of high-performance solution-proceesed perovskite FETs.

Metal halide perovskites, such as $MAPbX_3$ (X= Cl, Br or I) have recently garnered tremendous research efforts for a broad range of photovoltaic and optoelectronic applications[1-7], due to their favorable optical and electronic properties such as tunable bandgap[2], high absorption coefficient[3], and high photoluminescence quantum yield[4]. In particular, the power-conversion efficiencies (PCEs) of perovskite solar cells have been boosted to over 23% (certified) from a starting point of 3.8% over the past few years[4–8]. Apart from the rapid developments of materials and device architectures, a thorough understanding of fundamental physical processes including charge-carrier transport will be needed for further breakthroughs in device performance. However, a comprehensive physical picture of the intrinsic charge transport in the metal halide perovskites, which is key to the operation of optoelectronic devices, remains elusive. In order to gain insight into the charge transport mechanism of perovskite semiconductors, field-effect transistors (FETs) provide a controlled way of measuring charge transport properties. However, perovskite-based FETs suffer from various instabilities and exhibit large hysteresis effects due to ion migration in the channel.[9-10] Several groups have reported FETs based on organolead halide perovskites, in particular methylammonium lead iodide ($MAPbI_3$)[11–17]. Wang *et al.*[15] fabricated single-crystal $MAPbI_3$-based FETs with mobilities up to 2.5 cm^2/Vs at low temperature. Senanayak *et al.*[14] obtained thin-film $MAPbI_3$ FETs which have a mobility of ~0.5 cm^2/Vs at 300 K and >2 cm^2/Vs at 100 K. However, these mobility values are still far from being satisfying. Furthermore, most attention to date has been focussed on $MAPbI_3$ and only few reports on $MAPbBr_3$ perovskite FETs[18] have been made. Theoretical calculations have shown that there is potential for achieving exceptionally high carrier mobility of over 1,000 cm^2/Vs at room temperature in $MAPbBr_3$ perovskite and evidence for such high mobility values has been seen, for example, in time-of-flight and transient reflectance spectroscopy[19-20]. However, to date only one paper has reported single-crystal $MAPbBr_3$ FETs and little is known about the factors that govern the performance and stability of these devices[18]. In this work, we investigate single-crystal $MAPbBr_3$ FETs and particularly focus on the characterization of electrochemical instabilities at the interface between the perovskite singe crystal and the gold source-drain contacts. The suppression of such instabilities is an important factor that governs the performance achievable in such devices. We form the interface by a soft-contact lamination technique on top of a perovskite single crystal, which minimizes as much as possible non-idealities of the interface structure during contact formation, such as intermixing. We do not claim,

however, that our interfaces are defect-free as the single-crystals are likely to contain a certain concentration of point defects, such as vacancies. Our aim here is not to study the physics of an ideal metal-semiconductor interface, as recently reported for two-dimensional transition metal dichalcogenides[21], but merely to have an as controlled system as possible to investigate the electrochemical stability of the interface during electrical biasing.

To establish a suitable performance baseline and comparison to our earlier work on thin-film $MAPbI_3$ FETs we first fabricated thin-film $MAPbBr_3$ devices employing the method reported in Ref.[14]. Unfortunately, although the same process conditions were used as for optimized $MAPbI_3$ devices, the device performance is very poor. The devices were top-gated with a Cytop gate dielectric and the perovskite films were deposited from a 0.75 M precursor solution in an acetate solvent, spin coated at 5000 rpm for 3 mins and annealed at 100 ºC for 5 mins. Even at low temperature of 100 K, mobilities are only on the order of 10^{-3} cm^2/Vs, which is much lower than that of $MAPbI_3$ devices, and hysteresis effects are very pronounced (Fig. 1A, B and Fig. S1, S2, respectively). No gate modulation is observed at temperatures above 240 K. Despite significant attempts made to optimize process conditions, we were unable to optimize the performance of $MAPbBr_3$ in the same way as we were able to do with $MAPbI_3$[14]. The detailed reasons for such low performance of the thin film devices are not clear, but it appears that under these process conditions $MAPbBr_3$ is more prone to ion migration than $MAPbI_3$ under similar process conditions.

Considering that perovskite polycrystalline thin films have uncontrolled morphological variations, ionic impurities and defects introduced during the fabrication process or associated with grain boundaries, we then grew $MAPbBr_3$ single crystals for device application, which can help reduce trap density, suppress ion migration and reveal intrinsic charge transport properties.[15-16,22-23] We employed the optimized anti-solvent vapor assisted crystallization method [24] to grow high-quality lead bromide perovskite single crystals on silicon oxide/silicon substrates. The morphology of the perovskite $MAPbBr_3$ single crystals was evaluated using scanning electron microscopy (SEM) and atomic force microscopy (AFM). The SEM image shows that the as-grown single crystals exhibit smooth surfaces, and the lateral size of the single crystals can reach up to 200 μm with the shape reflecting the underlying symmetry of the crystal lattice. The thickness of the as-grown single crystals could be

controlled by tuning the duration of growth, i.e. the thickness increases as the growth time increases. Crystal thickness is critical for device fabrication as too thick crystals woud make it difficult to achieve efficient charge injection in the staggered source-drain contact configuration that we use below. For example, single crystals with thickness of 1-5 μm were obtained with a 7-hour growth process, as shown in Fig. S3 and S4. This is still rather thick and makes it difficult to fabricate optimized bottom-gate, top-contact devices with low contact resistance. The corresponding selected area electron diffraction (SAED) patterns are shown in Fig. 2A, indicating the single crystal structure. The phase purity can be further confirmed by θ-2θ X-ray diffraction and Raman spectroscopy. The XRD diffraction peaks can be assigned to the family of (h00) lattice planes of a cubic perovskite crystal parallel to the substrate plan (Fig. 2B). The full-width at half maximum of (001) diffraction for perovskite single crystal was found to be 0.072° (Fig. S5), which is comparable to previous reports[12, 24]. In contrast, for thin films other diffraction peaks are observed indicating a polycrystalline structure with multiple grain orientations with respect to the substrate plane. Raman spectroscopy has been performed an excitation wavelength of 633 nm to avoid the fluorescence background (Fig. 2C). The observed broad Raman bands below 200 cm^{-1} are attributed to a number of individual lattice vibrations, which cannot be spectrally resolved, but similar observations have been made in the literature[25]. The low-frequency band at 325 cm^{-1} is related to the restricted rotation of the MA^+ in $MAPbBr_3$, in agreement with that of reported $MAPbBr_3$[26]. We also compared the photoluminescence (PL) decay of $MAPbBr_3$ thin films and single crystals (Fig. 2D), observing a shorter PL decay, i.e. larger trap-induced recombination rate, in the thin films compared to that in the single crystals. This result also indicates reduced trap density in the single crystals, in agreement with previous reports on perovskite single crystals[1-2]. Together, these structural studies clearly demonstrate that our perovskite single crystals are of high quality and should be suitable for integration into FETs.

In addition to the high-quality of the semiconductor layer, the electrode/semiconductor interface is also critical for achieving high performance FETs. For organo lead halide perovskites, this is a particularly important issue since the electrodes/perovskite interface effects have been reported to greatly influence the device performance of optoelectronic devices[27-29]. A conventional, vacuum-based metal deposition process, such as thermal evaporation method commonly used in device fabrication, is usually accompanied by the presence of highly energetic metal atoms and the bombardment of metal clusters

onto the perovskite surface, which produces interface metal diffusion and degrades the interface even before any voltage is applied. In order to provide a more ideal interface, which is less dependent on the details of the contact fabrication process, we used here a more gentle soft-contact metal electrode fabrication technique[21, 30-31], in which atomically flat metal electrodes are physically laminated onto the smooth $MAPbBr_3$ perovskite single crystal, avoiding the metal diffusion into the perovskite single crystal that usually occurs during thermal evaporation of electrodes. This technique also provides us with the ability to peel off the electrodes after device operation. In this way we can investigate any modifications of the interface structure during device operation by applying surface analytical techniques to the exposed surface of the perovskite crystal after peeling off the electrodes.

Top-contact devices of the perovskite single crystal were fabricated on Si/SiO_2 (300 nm) substrates by laminating two Au stripes as source and drain electrodes, and the devices were operated/poled for a period of 10 mins before the electrodes were removed. Interestingly, an unusual fluorescence quenching was clearly observed at the positively biased anode region after the poling measurement and became more significant with longer poling time, regardless of whether or not the gate electric field was present. In contrast, fluorescence under the negatively biased cathode region was not quenched by the poling process (Fig.3A and Fig. S6, S7). The PL peak for $MAPbBr_3$ can be found at 535 nm with the excitation of 405-nm laser, and we performed PL spectroscopy on three different positions of the poled perovskite single crystal shown in Fig. 3A. The spectral shape is similar, but there is clear evidence for PL quenching on the anode electrode area after electrical poling (Fig. 3B position 1). The most likely explanation for this observation is that an electrochemical reaction occurs at the perovskite/anode interface during biasing of the source-drain electrodes, which is also likely to be detrimental to the device performance. Recent work also reported the enhanced PL quenching of $MAPbI_3$ thin films after poling measurement, suggesting that the combination of field-induced ion migration and injected charge carriers leads to trap formation which are detrimental to the FET operation[32].

In order to better understand the nature of the electrochemical reaction we characterized the interfacial properties of the perovskite single crystal after poling measurements using a lateral device structure by means of atomic force microscopy (AFM) and scanning kelvin probe microscopy (SKPM). Au

electrodes could be easily peeled off by a tip to expose the poled perovskite single crystal. However, underneath the positive electrode we detected a thin residue on the surface of the perovskite crystal with a thickness of 16 nm (Fig. 3C), which was not present underneath the cathode. It should be noted that without bias application the Au electrode can be very easily and reproducibly peeled-off without leaving such residues. Thus the residue observed underneath the positively biased anode is very likely due to a perovskite-Au electrochemical interaction. SKPM measurements show that the surface potential of the anode area is more negative compared to the channel area, and the difference between them can be increased with the poling time, namely from -0.062 V for 2-minute poling to -0.164.5 V for 10-minute poling (Fig. 3C and Fig. S8). Futhermore, we have conducted high-resolution small area X-ray photoelectron spectroscopy (HR-XPS) analysis using the PHI 5000 versaprobe III to examine chemical state of the perovskite single crystal surface underneath the anode after poling and peeling off the Au electrodes. The XPS spectrum in Fig. 3D is performed on a small area (10×10 μm^2) of anode electrode area with the significant peaks at 84.4 eV and 87.9 eV, which is attributed to Au (0). In addition, two chemically shifted peaks with higher binding energy at 86.4 eV and 90.1 eV in the same area are assigned to ionized Au, as would be expected for the formation of $AuBr_x$ compound at the interface. This is clear evidence for a strong interaction between Au and perovskite during the electrical poling process. In contrast in the cathode area no such Au signal is observed (Fig. S9). This provides further evidence for an electrochemical reaction occurring during the poling process, and the residue is the product of this reaction.

To further investigate the mechamism of the electrochemical reaction, we performed time-of-flight secondary ion mass spectroscopy (ToF SIMS) with positive detection on the poled device (poled for 10 minutes) after peeling-off the Au electrodes (Fig. 4A-B and Fig. S10). In the surface scan (D1) we can clearly see the region in which residual gold ions remain underneath the peeled-off anode, while a reduction of the perovskite ions Pb^{2+} and Br^- signals can be observed at the same region, presumably because of a "shadowing" effect due to the Au-rich layer on the surface. In comparison, the region underneath the cathode does not show obvious changes of chemical composition. These observations provide direct evidence that underneath the positive electrode an electrochemical reaction occurs between the gold anode and the perovskite single crystal during the poling process. A possible mechanism for this is that negatively charged Br ions moved to the positive Au electrode during poling,

where Au was oxidized to form $AuBr_3$ according to $3Br^- - 3e + Au \rightarrow AuBr_3$. The reaction products are left on the surface of the perovskite crystals after peeling off the electrodes (Fig.3C). The reaction is limited to the surface region of the crystal, i.e. within a depth of less than 100 nm (D2, D3), no Au signal was detected in the bulk of the crystals (D4). The reaction is induced by poling here, but we found that it can also be induced by heating (Fig. S11).

We have explored the use of interlayers between the perovskite and the gold contacts in order to supress this interfacial electrochemical reaction. We first evaporated a layer of MoO_3 as a buffer layer between the soft-contact laminated Au and the $MAPbBr_3$ crystal and found that the PL quenching of $MAPbBr_3$ under the anode is significantly reduced after poling (Fig S12). This suggests that by such interfacial engineering we are able to reduce or eliminate the electrochemical reaction between the electrodes and the perovskite semiconductor. Unfortunately, such contact modification is not easy(compatible) to implement in a top-contact device as it would require additional patterning of the MoO_3 layer underneath the source-drain electrodes. It is challenging to precisely align a suitable shadow mask onto such a small single crystal, particularly in a glovebox environment; we therefore changed to a bottom-contact device architecture, where contact modification is much easier to achieve.

To fabricate $MAPbBr_3$ perovskite single crystal FETs we therefore used bottom-gate, bottom-contact FETs on a SiO_2/Si substrate with photolithographically patterned gold electrodes. This co-planar device configuration is also advantageous for minimizing the large access/contact resistance that would have resulted from the relatively large thickness of our perovskite crystals (1-5 μm) in top-contact devices. We explored different surface modification layers on the bottom-contact gold electrodes. MoO_3 is not compatible with the photolithographic patterning process performed in air, as its workfunction is strongly reduced when exposed to air[33]; we also attempted to evaluate polyethylenimine ethoxylated (PEIE)-modified Au despite its low workfunction, but found that such modification does not allow single crystal growth on the contacts. Instead we successfully employed the conducting polymer PEDOT:PSS (poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid) and the self-assembled monolayer pentafluorothiophenol (PFBT) as surface modification layers. We performed the FET measurements at 80 K in order to minimize ion migration effects in the device. With bare gold electrodes only a weak gate modulation and a high OFF current

is observed. With the PEDOT-PSS modified electrodes the device performance is only marginally improved. The best characteristics are obtained for PFBT modified electrodes, for which we can observe a significantly enhanced ON current, reduced OFF current and improved gate modulation. With PFBT modification the ON-OFF current ratio is improved from 10^2 to 10^6 over that of the device with unmodified Au electrodes. We extracted the mobility using the transconductance method in the saturation regime and found that the hole mobility μ could reach up to ~15 cm^2/Vs (Fig. 5A) at 80 K after the modification of Au by PFBT. To the best of our knowledge, this is also the highest field-effect mobility reported so far for metal halide perovskite FETs. In the PFBT-modified FET, the mobility is gate-voltage dependent at low V_G, yet becomes V_G independent at moderate V_G (−30 to −50 V) as shown in Fig. 5B. To assess the reliability of the mobility extraction, we compare the measured characteristics with that of an ideal transistor with characteristics according to $I_D = \frac{\mu C_i}{2}\frac{W}{L}(V_{GS} - V_{Th})^2$ and determine the mobility that such an ideal transistor would need to have to match the measured ON current at V_G = −60V [34] (Fig. S13). The effective mobility of the PFBT-modified Au contact device in our work is ~10 cm^2/Vs, suggesting that the reliability factor for the mobility extracted from the transconductance method is about 88.7%. In spite of the significant residual non-idealities and hysteresis in the device characteristics, which makes an accurate mobility determination more difficult, this analysis strongly supports our claim of a high mobility on the order of 10 cm^2/Vs in these optimized devices.

As shown in Fig. 5C, the mobility gradually decreases with increasing temperature and the hysteresis in the device characteristics between forward and reverse gate voltage sweeps becomes larger. Above 240 K, we are unable to observe a clear gate modulation of the current (Fig. S14). This suggests that our single crystals still contain a sufficiently high concentration of ionic defects that prevent observation of a clear field-effect at higher temperatures. The externally applied gate field is screened by the moving ions which leads to a reduction of the concentration of accumulated electronic carriers at the interface. At low temperatures, this ion migration as well as any residual electrochemical reaction at the interface are suppressed and the device can operate as a normal transistor [35].

It is interesting to note that despite the use of single crystals and our contact optimization it appears to be more difficult to suppress ion migration effects in $MAPbBr_3$ than in $MAPbI_3$[14]. This is confirmed

by calculations of the expected ion migration rate as a function of temperature and the corresponding activation energy E_A (see Computational Section) [36]. In ref. 36, the calculated E_A in $MAPbI_3$ are 2.31, 0.58, and 0.84 eV (Fig. S18) for the Pb, I, and MA, respectively. In comparison, the activation energies E_A for $MAPbBr_3$, calculated by the same method here, are 1.12, 0.45, and 0.66 eV (Fig. S18) for the Pb, Br, and MA, respectively. We find that the migration rate of the Br ion is larger than that of Pb and MA ion, and the Br ion migration rate at 80 K is lower by about 10 order of magnitudes than that at room temperature. This is likely to be the reason for the high-performance of PFBT-modified devices at low temperatures compared to that at room temperature. We also note that the structure of the perovksite crystals is known to undergo a structural phase transition around 235 K from a tetragonal, low-temperature structure to a cubic, high-temperature phase[37-38]. The simulations predict slight differences in the rate of Br ion migration between the two phases, but the dominant factor governing the rate of ion migration rate is the temperature. Our demonstration of high charge carrier mobility at low temperature gives hope that it might be possible to realize high performance $MAPbBr_3$ devices at room temperature. This will require optimised single crystal growth conditions that allow reducing the ionic defect concentration. We note that it has very recently been shown that $MAPbBr_3$ single crystals grown slowly from solution in between two solid substrates allow achieving room temperature operation with moderate mobilities of 2-3 cm^2/Vs, though hysteresis and stability characteristics were not reported in this paper.[18]

Finally, we would like to comment on the effect of the PEDOT and PFBT surface modification on the contact resistance. It might be argued that the contact modification may bring improvements in charge injection and contact resistance merely by modification of the work function as opposed to by minimization of electrochemical reactions at the interface. It is difficult to separate these two potential contributions to contact resistance and the instability in the device characteristics near room temperature and the residual ion migration make a quantitative analysis of contact resistance using conventional channel length scaling analysis challenging. However, the work functions of PEDOT:PSS- and PFBT-modified Au are smaller (4.9 eV) and larger (5.48 eV) than that of the unmodified Au surface (5.1 eV), respectively (Fig. S15). Since similar enhancements in FET performance are observed for both PEDOT:PSS and PFBT treatment, this suggests the performance improvement is not in fact a consequence of work function effects. Furthermore, we recorded the

current in the same device structure with different electrodes during the positive poling process (Fig. S16). It can be seen that in the PFBT modified devices there is significantly reduced hysteresis in the current voltage characteristics both at room temperature and at 80 K. This is further evidence that the PFBT surface modification does indeed lead to a suppression of the interfacial electrochemical reaction between gold and the perovskite.

In conclusion, we have reported that an electrochemical reaction occurs at the gold / $MAPbBr_3$ interface during electrical poling with a combination of electrical and spectroscopical investigations. The electrochemical reaction leads to the formation of defects in the perovskites, which manifest themselves in luminescence quenching of the perovskite underneath only the positively biased electrode and is detrimental to the device performance of $MAPbBr_3$ devices fabricated with normal gold electrodes. After inserting a buffer layer between the gold electrodes and perovskite, which is expected to alleviate the abovementioned electrochemical reactions, we have achieved individual $MAPbBr_3$ single crystal FETs with effective mobility values on the order of 10 cm^2/Vs at 80 K, which is higher by about four order of magnitudes than that of thin-film counterpart devices. Our work highlights the importance of contact engineering and suppression of interfacial electrochemical reactions to enable high performance perovskite FETs and has clear implications as well for other optoelectronic devices such as light-emitting diodes and solar cells-based on these materials.

Experiemental Section

Synthesis of $MAPbBr_3$ single crystal

All chemicals and regents were purchased from sigma-Aldrich and used as received unless noted otherwise. Antisolvent vapor-assisted crystallization (AVC) method was implemented in our work to grow high-quality $MAPbBr_3$ crystals according to previously reported procedures[24]. $PbBr_2$ and MABr (0.05 M) were dissolved in N,N-Dimethylformaide (DMF) and stirred at 100°C for approximately 1 h, yielding a homogeneous transparent solution. The resulting solution of $MAPbBr_3$ in DMF was then drop-cast onto the prepared substrate. The crystallization process was maintained with the slow diffusion of the antisolvent dichloromethane (DCM) vapor into the solution. $MAPbBr_3$ single crystals thus began to grow along the electrodes. All procedures were carried out in a nitrogen atmosphere excluding oxygen and water.

Device fabrication and characterization

$MAPbBr_3$ single crystal FETs

The transport measurement was performed on bottom-gate bottom-contact field-effect transistors. The devices were made on a Si/SiO_2 (300 nm) substrates which were successively cleaned by a sonication processes in deionized water, acetone and isopropanol. Standard lift-off photolithography was carried out on the cleaning substrates to define the source and drain electrodes (Cr/Au: 2nm/13nm). After oxygen plasma etching for 60 s, the Au electrodes were further modified with the self-assembled monolayer pentafluorothiophenol (PFBT). For PEDOT:PSS modification, an additional layer of PEDOT:PSS (~6 nm) is spin-coated on top of the gold after the thermal evaporation, then the source and drain electrodes comprising the Cr/Au/PEDOT:PSS tri-layer structure can be defined by the lift-off process. The temperature –dependent transport measurements were performed using a Desert Cryogenics low-temperature probe station.

$MAPbBr_3$ thin-film FETs

Thin film top-gate bottom-contact perovskite devices were fabricated on pre-cleaned glass substrates with photo-lithographically patterned Cr/Au electrodes. For the preparation of the precursor solution, Methylammonium bromide obtained from Dyesol Inc and Lead(II) acetate trihydrate (99.999%) purchased from Sigma-Aldrich Inc were mixed in N,N′-dimethylformamide in a 3:1 molar ratio to obtain a final concentration of 0.75 M. The precursor solution was then spin coated on top of the device substrates at 5000 rpm for 180 seconds and annealed at 100 °C for 5 minutes. A Cytop dielectric layer of thickness ~500 nm was spin-coated over the perovskite film and annealed at 90 °C for 20 min. This was followed by the evaporation of the Au gate electrode (25 nm) through a shadow mask to complete the device. The completed devices were characterized using an Agilent 4155B parameter analyzer operated in the pulsed mode operation as introduced earlier[14].

Scanning Kelvin probe microscopy measurements

Kelvin probe measurements were carried out with a Veeco Dimension 3100 AFM system in ambient atmosphere. The measurements were conducted with Pt/Ir-coated tips with a resonant frequency of 75 kHz.

Acknowledgements

This work was supported by the Ministry of Science and Technology of China (2016YFB0401100, 2017YFA0204704), the National Natural Science Foundation of China (21805284, 21873108), the Chinese Academy of Sciences (Hundred Talents Plan, Youth Innovation Promotion Association), the Strategic Priority Research Program (Grant No. XDB30000000 & XDB12030300)), the Engineering and Physical Sciences Research Council (EPSRC) through a programme grant (EP/M005141/1)) and the Royal Society through a Newton Fellowship. ToF-SIMS characterization was conducted at the Center for Nanophase Materials Sciences, which is a DOE Office of Science User Facility. The authors thank Prof. Dong Shi, Dr. Ye Zou, Prof. Cheng Li, Dr. Yao Zhao and Dr. Ye Fan for discussion.

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Figures

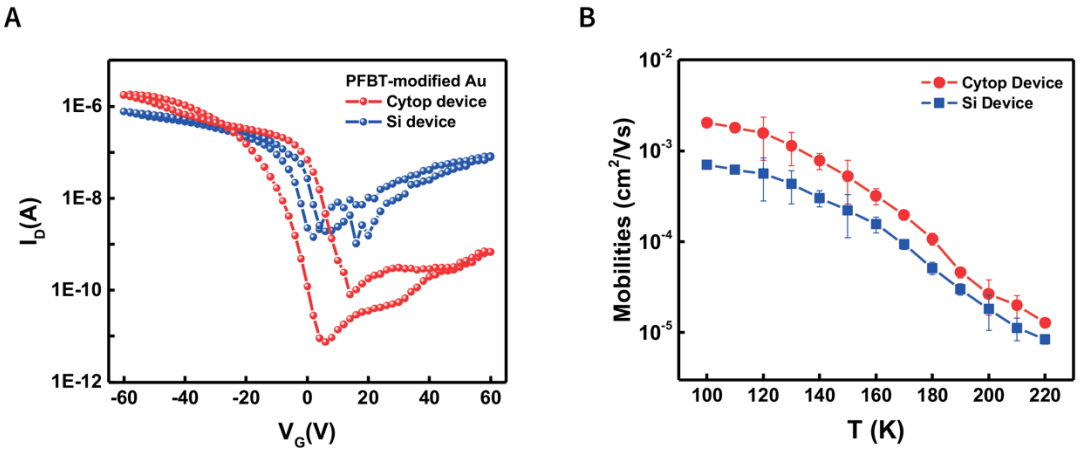

Figure 1. Electrical characterizations of thin-film $MAPbBr_3$ perovskite FETs. A) Transfer characteristics of the perovskite devices (L = 10 μm, W = 1 mm) at 100 K with top-gate, bottom-contact device with Cytop as the dielectric layer (labeled as Cytop device) and bottom-gate, bottom-contact device with SiO_2 gate dielectric (labeled as Si device). **B)** temperature-dependence of the mobility measured using Cytop device and Si device. Note that for temperatures above 240 K no gate modulation is observed. Error bars plotted for representative data points represent the standard deviation for measurements performed on three devices.

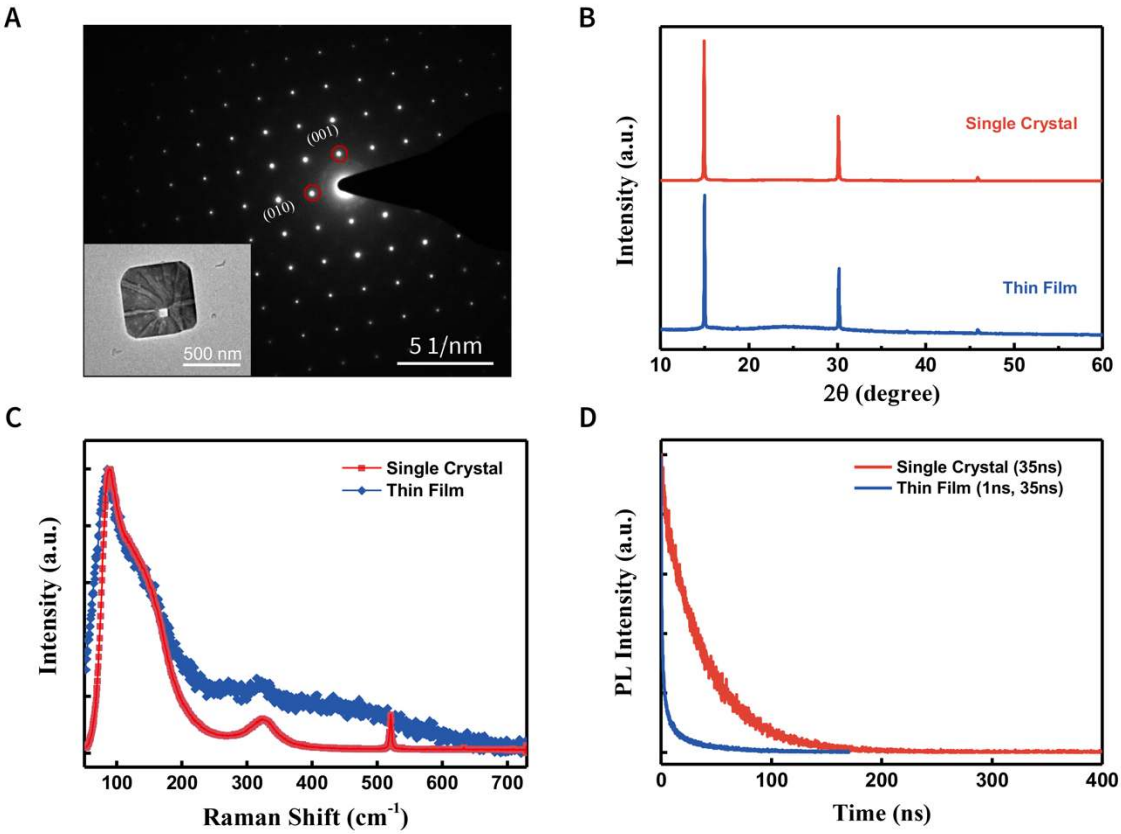

Figure 2. Structure chracterizations of lead bromide perovskite single crystals. A) TEM (Transmission Electron Microscope) image (inset) and the corresponding SAED pattern of an as-grown single crystal; **B)** θ-2θ XRD pattern, **C)** corresponding Raman spectra, in which the peak at 520 cm^{-1} is attributed to the silicon substrate, and **D)** time-resolved PL spectra of $MAPbBr_3$ single crystal and thin film, respectively.

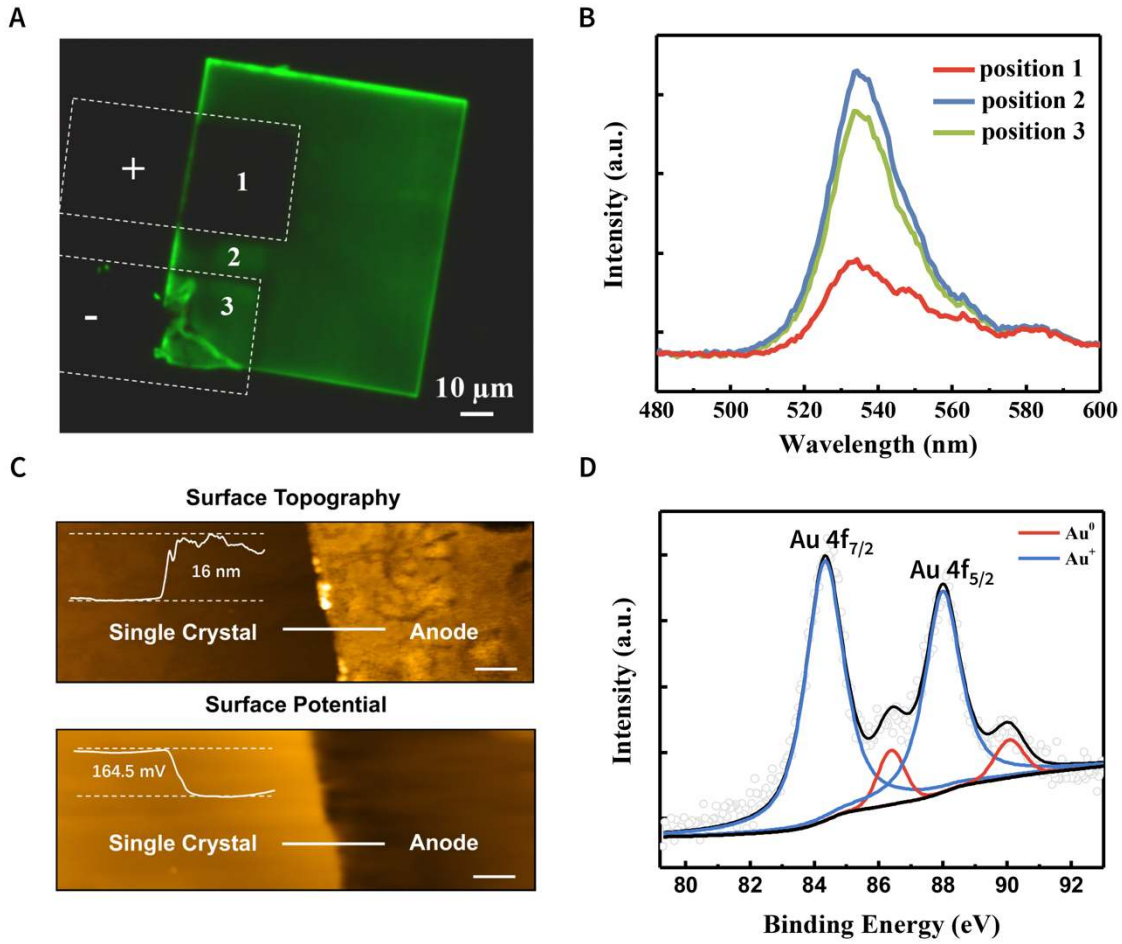

Figure 3. Mechanism study of the electrochemical reaction. A) fluorescent image of the perovskite single crystal with peeled-off Au electrodes. **B)** spatially resolved photoluminescence spectra on different positions on the poled perovskite device shown in A. **C)** the topography and its corresponding potential maps in SKPM profiles at the edge of the anode electrode after poling and peeling off the electrode (scale bar: 2 μm). **D)** High-resolution small area XPS spectrum of the poled perovskite device in the anode area (position 1) with an area of 10×10 μm^2.

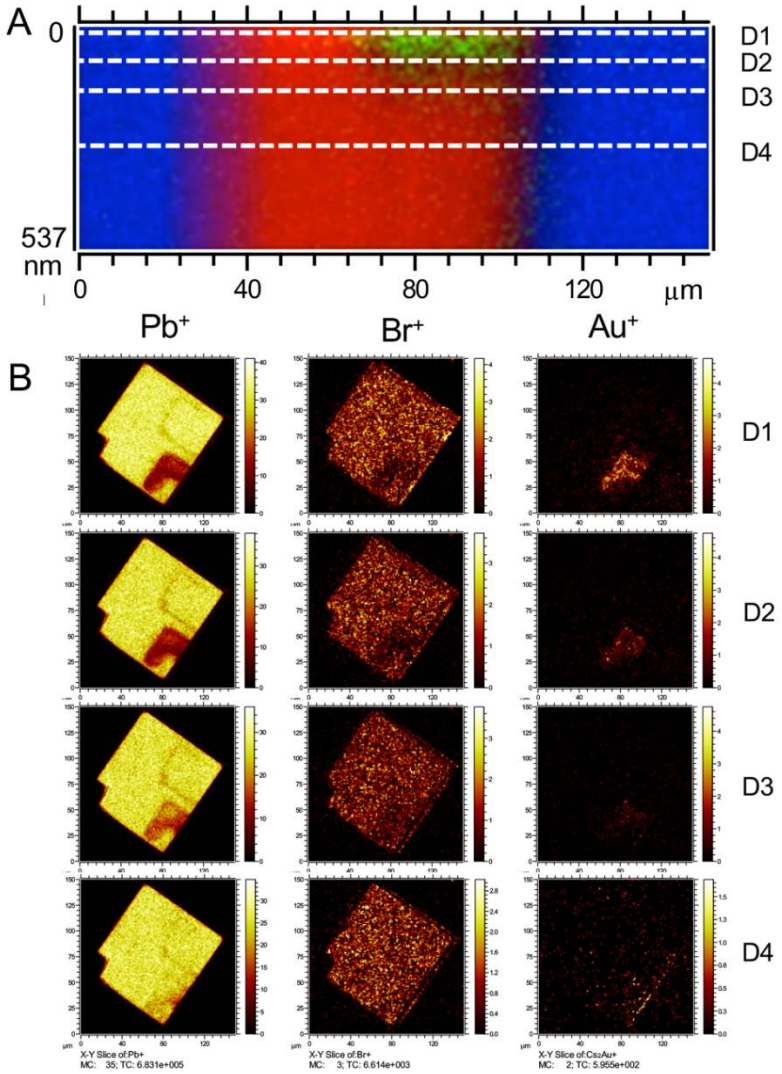

Figure 4. ToF SIMS characterization of the electrochemical reaction after poling. A) section mapping as a function of depth, (here blue, red and green represent Si, Pb and Au respectively), **B)** mapping in x-y plane (170 µm×150 µm) of $MAPbBr_3$ single crystals at different depth shown in A). D1-D4 indicate different depths into the crystal, where D1 corresponds to the surface of the crystal after peeling off the electrodes.

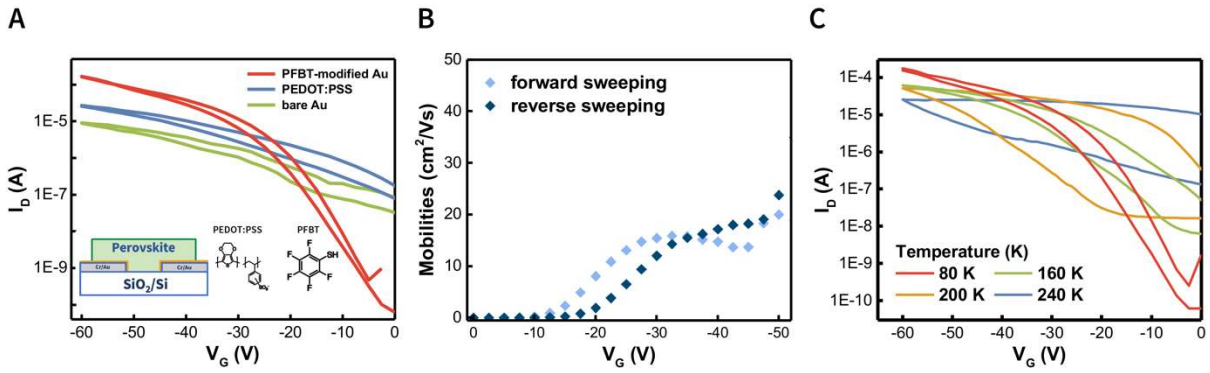

Figure 5. Electrical properties of single crystal perovskite FETs. A) Transfer characteristics at low temperature (80 K) of the devices with Au, PEDOT:PSS and PFBT-modified Au as source/drain electrodes (inset: FET device configuration). **B)** Gate-voltage dependence of saturation mobility μ at 80 K for PFBT-modified Au devices. **C)** Temperature evolution of $MAPbBr_3$ transfer characteristics with PFBT-modified Au as electrodes (drain voltage, V_D= -60 V).