Investigation of HV/HR-CMOS Technology for the ATLAS Phase-II Strip Tracker Upgrade

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Abstract: ATLAS has formed strip CMOS project to study the use of CMOS MAPS devices as silicon strip sensors for the Phase-II Strip Tracker Upgrade. This choice of

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sensors promises several advantages over the conventional baseline design, such as better resolution, less material in the tracking volume, and faster construction speed. At the same time, many design features of the sensors are driven by the requirement of minimizing the impact on the rest of the detector. Hence the target devices feature long pixels which are grouped to form a virtual strip with binary-encoded z position. The key performance aspects are radiation hardness compatibility with HL-LHC environment, as well as extraction of the full hit position with full-reticle readout architecture. To date, several test chips have been submitted using two different CMOS technologies. The AMS 350 nm is a high voltage CMOS process (HV-CMOS), that features the sensor bias of up to 120 V. The TowerJazz 180 nm high resistivity CMOS process (HR-CMOS) uses a high resistivity epitaxial layer to provide the depletion region on top of the substrate. We have evaluated passive pixel performance, and charge collection projections. The results strongly support the radiation tolerance of these devices to radiation dose of the HL-LHC in the strip tracker region. We also describe design features for the next chip submission that are motivated by our technology evaluation.

1. Introduction

Traditional silicon tracking systems in High-Energy Physics feature heterogeneous architecture of separately produced sensors and readout amplifier chips. As a consequence, their interconnect becomes a significant aspect of the system integration when the number of readout channels is in the range of 10s and 100s of million. Attempts to make monolithic sensors have been long made. One interesting example is HV-CMOS technology [1]. It attracted significant attention due to recent indications of its radiation hardness [2,3].

The indications instigated ATLAS to investigate this technology for its suitability for the upgraded strip tracker. (There is a similar program for pixel system [4].) The sensor design has to be pixelated to limit the amplifier's input capacitance and therefore noise. The consequence of this is a potential of reducing the active surface area by about a factor of two compared to the traditional design of two strip layers giving one 3D hit position using a small crossing angle [5]. An additional benefit is a better positional resolution. With less active area in the same volume, the tracker will have less radiation length. There is also a potential for shorter construction time, and reduced sensor cost.

In order to have a practical possibility of implementing the CMOS sensors for ATLAS Phase-II tracker upgrade, the design changes to the rest of the tracker have to be minimal. Therefore, the program aims at preserving the baseline architecture of staves and petals composed of modules, which in turn are composed of sensors and hybrids. The big difference compared to the baseline design is that a) the sensors have built-in amplifiers, b) the sensors have comparators and fast hit encoding engine in the peripheral region, c) the readout chips have only digital circuitry. The readout chips would still contain digital pipeline, trigger and command interfaces. They would be a simplified version of the current prototype chips. Due to the hit encoding in the sensors, the information exchange between the sensors and readout chips can be implemented on a fast digital bus, which uses far fewer wirebonds than the traditional scheme of 1 bond per channel.

While the CMOS sensors have a potential to bring in these attractive performance features, the key issue is their performance and radiation hardness for doses relevant for

the strip region: 60 Mrad and $2x10^{15}$ neq/cm^2 [5]. The first year of the evaluation program aims at characterizing the basic properties of the technology. We chose two foundries for this evaluation. One is HV-CMOS process from AMS with 350 nm feature size. It features a possibility of biasing the substrate of up to 120 V to provide a thin depletion region. The second process is HR-CMOS 180 nm from TowerJazz. It implements a high resistivity epitaxial layer on top of a substrate that can be used as a charge collection medium.

At the time of this writing we have results from AMS HV-CMOS process. We give their overview in this paper, with an emphasis on passive pixel tests. They are an important part of the monolithic sensor design, defining the signal level, influencing the attainable noise and spatial accuracy of the sensor. The passive pixel tests are a new aspect of this technology investigation compared to the earlier publications [2,3].

2. Test ASICs

With both technologies chosen for our evaluation we expect the signal level to be significantly smaller than for traditional hybrid strips or pixel systems. Therefore a special attention has to be payed to both the signal and noise level achievable. In case of the TowerJazz technology the depletion region is limited to that of maximal epitaxial layer thickness, of about 25 um. This aspect of the technology constraints the signal level one can expect to obtain. The AMS technology allows for use of higher bulk resistivities that could lead to higher signal level. This will be explored in future chip submissions (Section 4).

In order to facilitate the technology characterization, we had several test ASIC submissions. Their designs implemented test structures to enable several types of critical tests. To investigate signal-to-noise ratio and to develop design for a large scale chip, it is important to know signal level after bulk damage due to radiation. A key aspect of the noise performance is the pixel capacitance present on the amplifier input. The ASIC design toolkits cannot estimate these factors, so we included passive pixel structures to measure these parameters after irradiation.

Another key aspect of the CMOS sensors is amplifier implementation inside the pixel area, where as the comparators and digital processing are planned to be put in the sensor periphery to avoid extra noise. The finite density of signal lines running from each pixel to the periphery requires use of relatively long pixels, up to 800 μm. We included structures with varying length to study its effect on the performance.

The total of 3 test ASICs have been made to date:

- HVStripV1 chip in the HV-CMOS technology. It had test transistors, 2 rows of active pixels of 40x400 μm^2 size with discriminators and digital readout scheme, and pixel structures with analog readout.
- CHESS-1-AMS chip in the HV-CMOS technology. It contained test transistors, passive pixels of varying length, standalone amplifiers, and active pixels with embedded amplifiers (Figure 1). The chip also contained specialized structures: a large passive array to aid charge collection studies, and a passive pixel array near the edge to allow for depletion region studies with sidewise illumination. All test structures featured design rules for 120 V bias. The fraction of pixel area occupied by the collecting n-well was varied for the passive pixels. In

some test structures n-well area was 30% of the total pixel area, and in others it was 50%. The passive pixel test structure connection scheme is shown in Figure 2.

- CHESS-1-TJ chip in the HR-CMOS technology. Similarly to CHESS-1-AMS, it contained transistors, passive pixels, standalone amplifiers, and active pixels. In addition, it had a variation of the epitaxial layer thickness and different bulk types. The collecting diode geometry was varied for passive pixels.

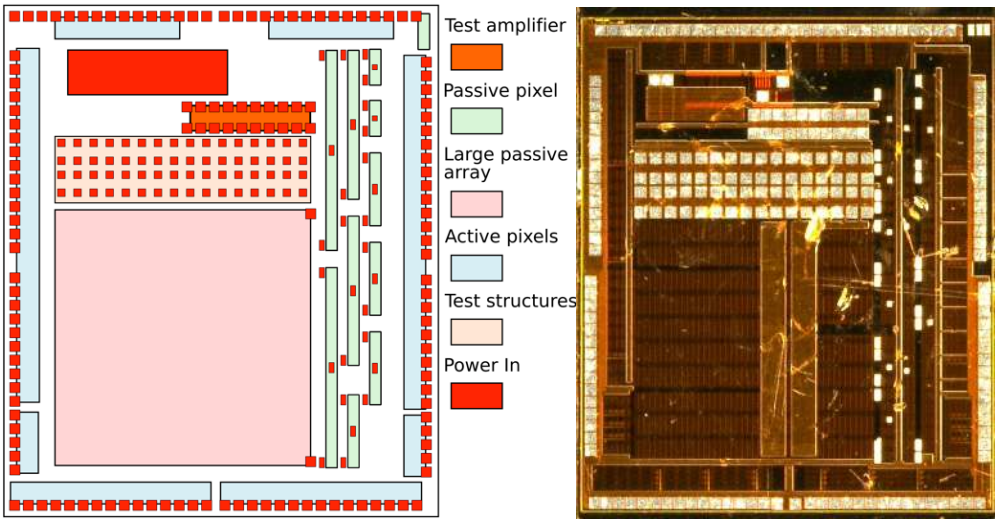

Figure 1. Layout schematics of CHESS-1-AMS chip (left) and a picture of fabricated device (right).

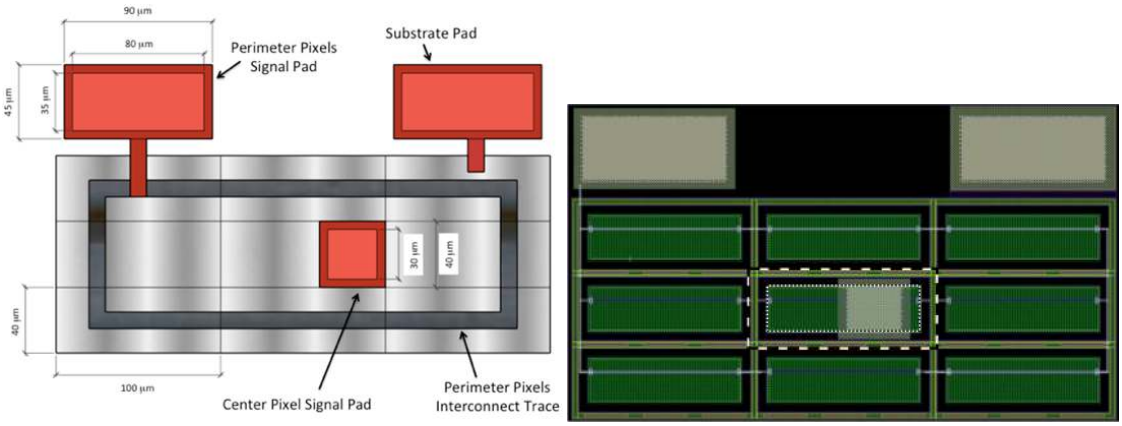

Figure 2. A sketch (left) and layout (right) of a passive pixel test structure. The central pixel location in the layout and its n-well are indicated with dashed and dotted lines respectively. It is surrounded by 8 peripheral pixels all connected together for test purposes. An additional contact biases the substrate.

CHESS-1 chips had implemented a different design philosophy, consistent with prior designs in these technologies. CHESS-1-AMS had the active pixel amplifiers embedded in the collecting n-wells. CHESS-1-TJ had the circuit placed in a separate well from the small collecting diode. In principle, both design choices can be implemented in either technology. This small collected diode design can drastically minimize the amplifiers input capacitance to arrive at a lower noise level. This is

important for the TowerJazz technology due to the limited signal level due to epitaxial layer thickness. However, the field geometry in the depleted region may be more complicated this case, especially after bulk damage after hadron irradiation. Therefore a special attention will have to be payed to both signal level and spatial signal uniformity for CHESS-1-TJ pixels.

The inclusion of passive pixels and standalone amplifiers in these test chips was intentional. We wanted to disambiguate the effects of radiation on the depleted region and other "sensor" effects from the evolution of amplifier performance with ionizing dose.

3. Test results

a) Passive Pixels

The passive pixel arrays allow us to investigate basic bulk and surface properties of the sensors. These characterizations are similar to what is typically done on the conventional passive sensors [6, 7]. The main differences are thin depletion region, about 15-20 μm with default value of bulk resistivity at 120 V bias, and the small pixel dimensions: 45 μm in width and between 100 and 800 μm in length.

One of the important assessments is charge collection study as a function of fluence. The details of the study will be reported elsewhere [8]. The results show a non-trivial dependence for the default value of 20 Ωcm, due to several phenomena. They include a presence of signal from diffusion before irradiation, a growth of depleted region due to fast acceptor removal [9], and an onset of trapping at high enough fluences. For the fluence range of interest to the strip tracker the minimum collected signal is about 1500 electrons.

Basic "surface properties" characterizations included IV, CV and inter-pixel resistance measurements. The leakage current values were comparable with losses in conventional BNC cables, therefore we used low-loss triaxial cables. To avoid stray currents going through the probe station we used a ground connection on the substrate contact pad. High Voltage connection was supplied to all 9 pixels in a passive pixel structure (Figure 2). A semiconductor parameter analyzer measured the total current. The results indicate a familiar scaling with bias voltage and depleted depth, albeit at the very low current level due to thin depleted region (Figure 3).

For the capacitance measurements we biased all 9 pixels at 100 V. A capacitively coupled LCR meter stimulated the central pixel with respect to the neighbors and the substrate to determine the total capacitance. The values are also rather small (Figure 4 and Table 1), and the measurements at the level of 100 fF and below can be challenging. However, the measured values for the long pixels we are interested in are rather consistent with the TCAD simulations of the sensors (Table 1), ensuring that the chip design simulations have correct assumptions. In principle, one could lower the capacitance by using smaller area of the n-well (Figure 4), although this may limit the area for in-pixel analog electronics and affect post-irradiation performance.

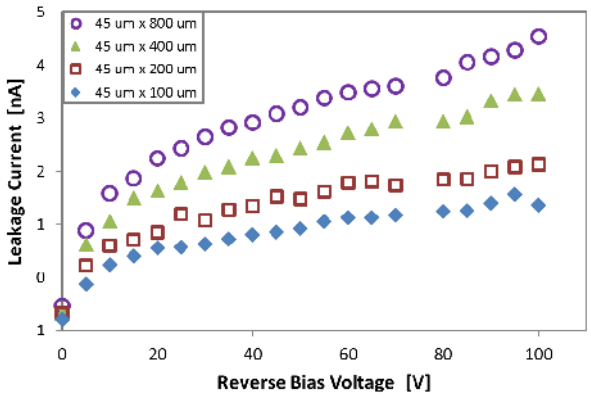

Figure 3. Leakage current on passive sensors as a function of bias voltage for different pixel lengths.

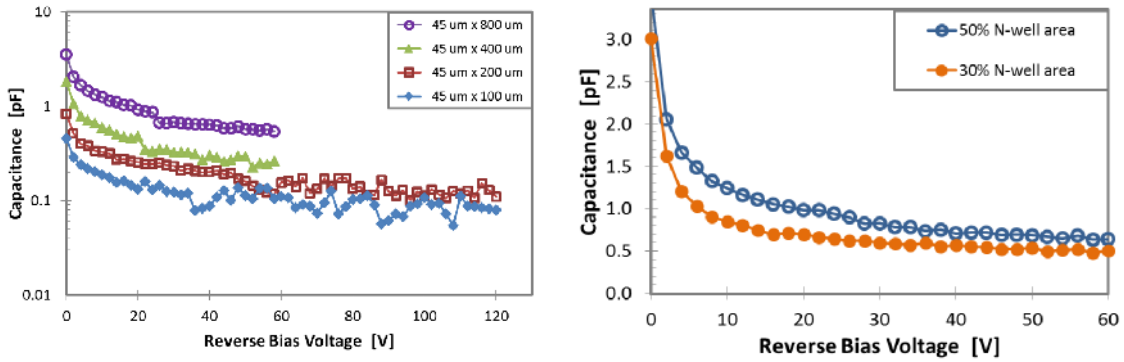

Figure 4. Left plot shows measurements of pixel capacitance with respect to the bulk and neighboring pixels as a function of bias voltage. Right plot shows measurements for the 800 mm long pixels in cases when n-well occupies 30% of the pixel area (filled circles) and 50% of the pixel area (open circles).

Table 1. Measured and simulated capacitance values for passive pixels at two bias voltage values.

Pixel length [μm]	Measured C(60V) [fF]	Simulated C(60V) [fF]	Measured C(120V) [fF]	Simulated C(120V)[fF]
100	~100	63	~70	56
200	~200	117	~170	105
400	250	227		202
800	450	445		397

The setup for the inter-pixel resistance measurement was similar to the one for IV characterization, except that different channels of parameter analyzer controlled the voltages for the central pixel and its neighbors. The central pixel was maintained at 99 V potential with respect to the substrate. The neighbor potential was varied between 98 V and 100 V while the current going to the central pixel was measured. The resistance was

derived differentially as R(inter-pixel) = dV(neighbors)/dI(central). The values obtained showed a rather high resistance in the range of 100s of GΩ (Figure 5). This is natural, since the top-side biasing is implemented in these devices with doped areas between the pixel n-wells, called "guard rings". The guard rings provide a strong isolation, similar to "p-stop" technique in conventional sensors [7]. A test structure without intentional guard ring still showed similarly high resistance indicating a presence of similar structure between the n-wells.

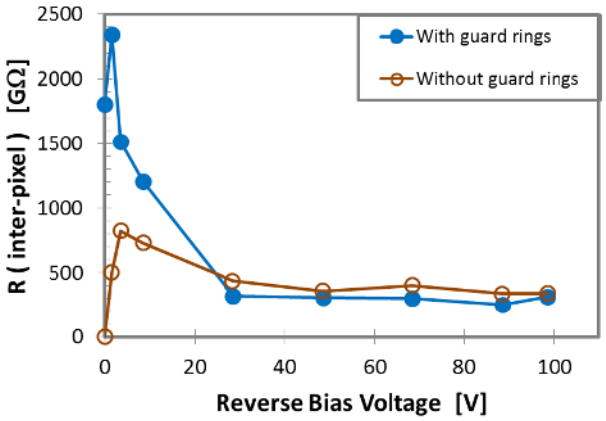

Figure 5. Inter-pixel resistance as a function of bias voltage. The graph with filled symbols is for the conventional design with "guard ring" between the pixels containing doped area for top-side biasing. The open symbols are for the pixel design with omitted guard ring.

Using the 120 V design rule assures that such voltage can be applied on vast majority of structures. A possibility to apply even higher voltage would increase the depleted region and therefore the signal collected from the sensor. Measurements in wider voltage range indicated that the safety margin may not be too high: there are signs of breakdown above 130 V (Figure 6). Furthermore, irradiated devices show a difference in currents measured on pixels with 30% and 50% diode area fraction after ionizing dose (Figure 7). The 30% area fraction pixels show signs of early soft breakdown during the measurements that increase their currents substantially. The 50% area fraction pixels did not have this phenomenon. We attribute this observation to the gain in the interface charge between the surface oxide and silicon. The extra charge increased in the peak electric fields near the surface, which was critical for the breakdown of 30% area fraction pixels due to higher curvature of the implant geometry. The post-irradiation performance difference constrains the size of the n-well one can have, therefore presenting limitations for the pixel capacitance and noise performance.

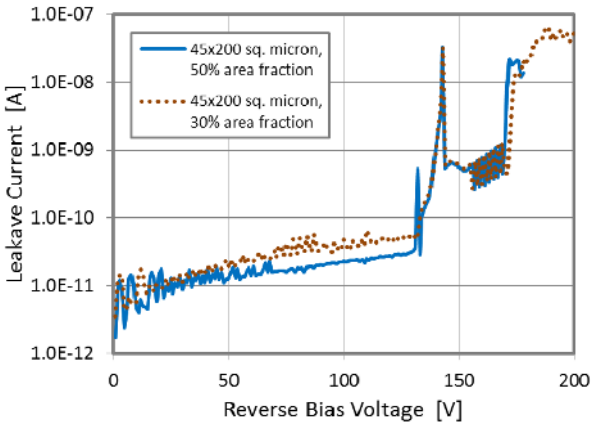

Figure 6. Current-voltage characteristics on passive test structures with 30% and 50% area fractions filled by n-well in the bias range exceeding the nominal 120 V design rule.

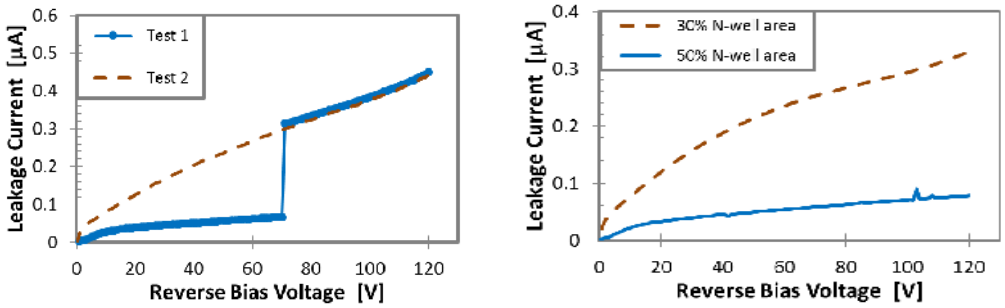

Figure 7. Repeated IV tests on passive pixel array with collecting n-well occupying 30% of the pixel area, which has been irradiated to 30 Mrad with gammas (left). A comparison on pixels 30% diode area fraction (dashed line) and 50% fraction (solid line) irradiated to 100 Mrad dose with gammas.

Another observation of the breakdown voltages was obtained after neutron irradiation (Figure 8). In this case the breakdown happens in the range of 130-150 V for all pixels with 50% diode area fraction, not very different from the pre-radiation measurement. We attribute this consistency to the top-side biasing geometry used in these devices, where the biasing voltage is supplied through the substrate contact on top. This geometry maintains the same distance between the collecting diodes and the implant supplying high-voltage potential along the surface after irradiation. This is in contrast to conventional backside-biased sensors (Figure 9) that have a sidewall surface between collecting diodes and biasing potential on the back. The sidewall, which is initially conductive, becomes resistive after irradiation. As the result it effectively lengthens the surface path between the diodes and the bias which leads to an increase in the breakdown voltage [10]. The pixels with 30% diode area fraction had higher breakdown voltages after the neutron irradiation. However, using this feature would be difficult in light of their susceptibility to the ionizing dose.

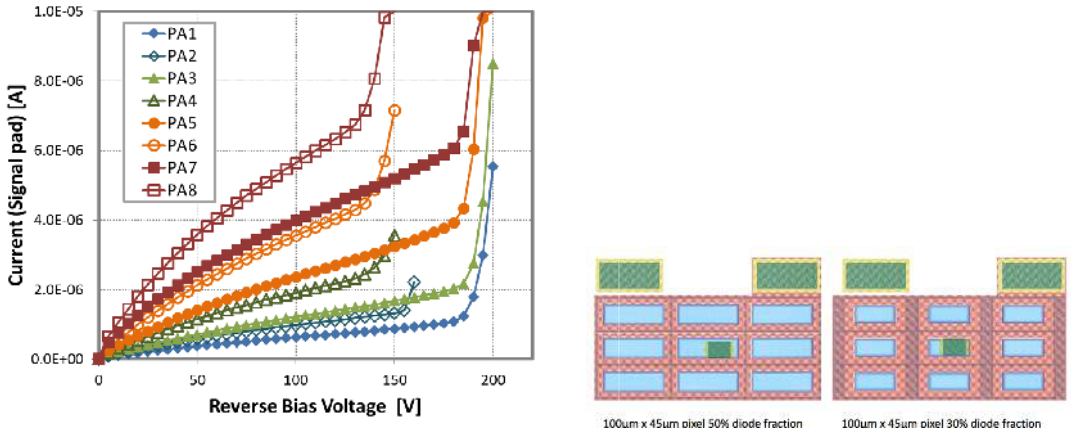

Figure 8. IV characteristics of test pixel arrays irradiated with $2x10^{15}$ neq/cm^2 neutron fluence (left) and the layout of arrays with different diode area fractions (right). Structures PA1, PA3, PA5, PA7 have 30% fraction, and structures PA2, PA4, PA6, PA8 have 50% fraction.

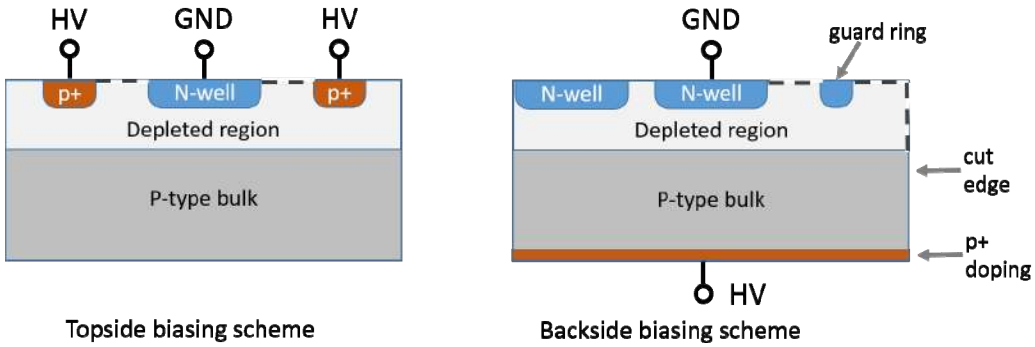

Figure 9. A sketch for top- and backside-biasing schemes. Surface path connecting collecting n-wells and the HV bias region is indicated with a dashed line.

b) Amplifiers

Performance of both stand-alone amplifiers and active pixels is described in Ref [11]. There is an observed evolution of amplifier noise with ionizing dose. The noise increases by at least a factor of 3 for the strip tracker dose of 60 Mrad compared to the pre-radiation value. The amplifier gain can be made stable with bias current tuning for some of the designs. Previous observations with HVStripV1 chip with Fe-55 source indicated S/N ratio of 13 before irradiation. The signal deposited in the sensor is comparable to the minimal value of 1500 electrons, indicating a need for more depletion to ameliorate the effect of noise increase. Further studies are under way to improve the characterization of active pixels. Figure 10 illustrates their response to Americium-241 source with 5.5 MeV energy deposition. Such a large signal causes amplifier saturation at ~0.7 V output. Studies with Sr-90 should yield a response close to a minimum ionizing particle level [12].

One of the important amplifier performance aspects for strip tracker is timing performance. Due to the strip readout architecture features, single bunch crossing

resolution of 25 ns is required. Data in [11] indicate that both timing jitter and time walk are consistent with this requirement for the expected signal range.

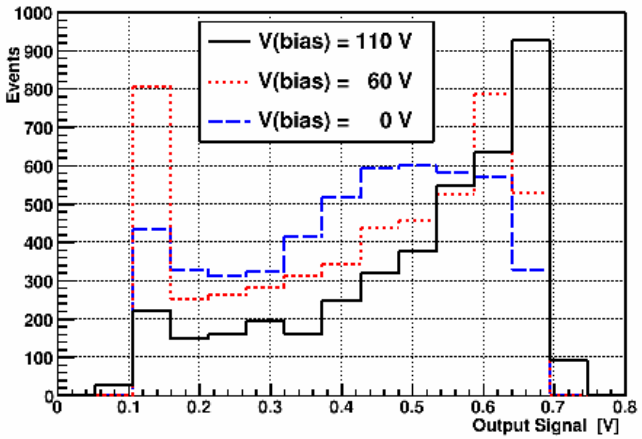

Figure 10. Active pixel response to Am-41 source on CHESS-1 chip. The peak value of the amplifier's output waveform is plotted.

4. Large-scale chip

The results of the 1st year investigation of HV-CMOS technology have been incorporated in an on-going design of a full-reticle chip, CHESS-2-AMS. It has several important goals aimed at definitive characterization of the technology:

- Prototyping of the readout architecture. Reading out a large pixel array with the single-bunch timing resolution to conform to strip tracker readout requirements is not trivial. The current assumption is the need for reading up to 8 hits from the area of 128 strips, each comprising 32 pixels. The block-diagram of the readout scheme is shown in Figure 11. Analog information from the active pixel array is digitized by comparators which transmit the hit information to hit encoding engine. The engine scans the available hits within 25 ns of bunch-crossing time and encodes at most 8 of them for transmission off the chip. The output is sent synchronously with the bunch crossing, with a fixed delay. No hand-shaking is involved. Instead, the output is always transmitted at 320 MHz to allow for up to 8 hits.
- Assessment of common mode noise phenomena and cross talk. The large chip may be afflicted with common mode noise which would modify the assessment of the signal to noise ratio obtained with the smaller test structure. Furthermore, the scheme of transferring the amplifier outputs to the chip periphery for hit processing may have some level of cross-talk that we need to characterize. The chip will contain several areas with comparator placement in pixel, and in the periphery to find the best solution.
- The submission is planning to use several substrate wafer resistivities higher than the default value to increase the sensor signal level.

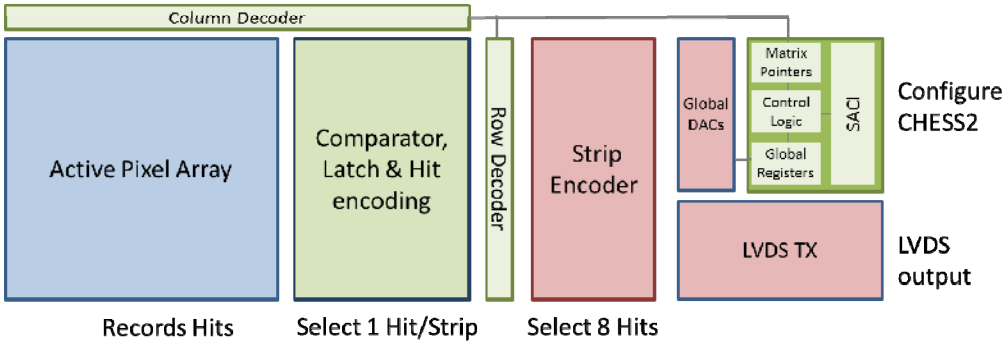

Figure 11. Block-diagram of CHESS-2-AMS chip design architecture[‡‡]. The reticle area is dominated by the Active Pixel Array part.

The issue of signal increase is not trivial. The charge collection study [8] indicated that the acceptor removal rate is a function of bulk doping. Empirical calculations based on the information known so far show an increase of minimal signal with initial resistivity (Figure 12). For resistivities above 80 Ωcm the minimal signal of about 4500 electrons is obtained at the full strip tracker fluence of $2x10^{15}$ neq/cm^2, when the effect of charge trapping dominates. The signal gain for higher resistivities is minimal.

There is also an adverse aspect of using high resistivity wafers, which may make using them with top-side biasing less attractive. TCAD simulations of the depleted region show that for 1000 Ωcm the field gradient is weaker and less uniform than for 80 Ωcm, even before irradiation (Figure 13).

A combination of these considerations indicates that the optimal resistivity values may be in the range of roughly 80-200 Ωcm.

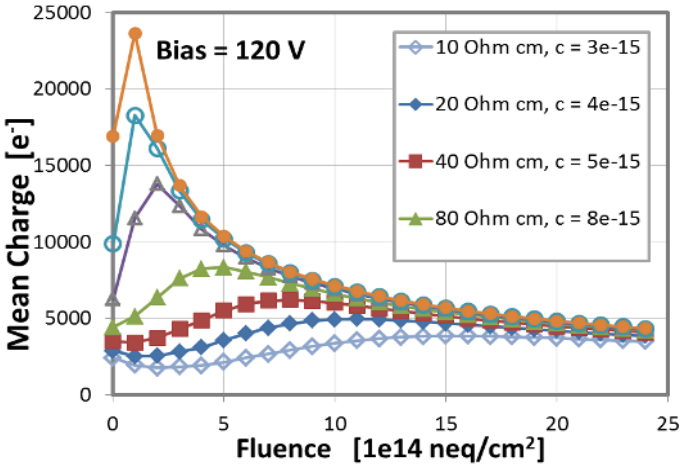

Figure 12. Empirical calculations of collected charge as a function of fluence for different initial bulk resistivities.

[‡‡] Here SACI stands for SLAC ASIC Control Interface.

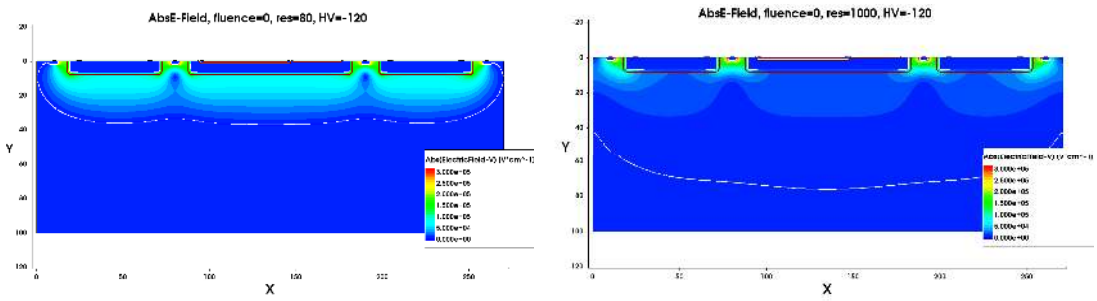

Figure 13. Electric field profiles with top side biasing for 80 Ωcm (left) and 1000 Ωcm (right) wafer resistivities. The white line indicates the depletion region boundary.

5. Conclusions

As a part of the plan to characterize HV/HR-CMOS technologies for ATLAS strip tracker, we produced and characterized several test devices. HV-CMOS results include assessments of leakage current, capacitance, and inter-pixel resistance. The current and capacitance are important aspects of the monolithic sensor design, especially for the relatively long pixels to be used in this application. They affect the signal-to-noise projections and analog design parameters.

The inter-pixel resistance is very high due to built-in process features. This ensures the channel isolation necessary for spatial resolution promised by the pixel layout.

There is a preference for collecting n-wells with 50% pixel area versus 30% pixel area, since the latter has a soft breakdown after ionizing dose. The breakdown voltages do not increase much beyond the foundry-guaranteed 120 V after neutron irradiation due to top-side biasing. As the result of these findings, we can rely on being able to bias the devices at 120 V when using n-wells with 50% pixel area. However, the method of boosting the signal level by applying even higher bias voltages post-radiation is not viable in this case.

Initial signal-to-noise characterization with Fe-55 source indicates the value of 13, which may be acceptable. However, the amplifier noise increases with radiation level by at least a factor of 3. The plan for the next (full-reticle) chip is to use higher bulk resistivities that may increase the signal by a similar factor according to empirical calculations. As the result, the high signal-to-noise value may be maintained. The chip will also feature a readout scheme compatible with strip tracker readout architecture, and it will allow characterization of common mode noise and cross talk.

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