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Investigation of Inversion Charge Characteristics and Inversion Charge Loss for InGaAs Negative-Capacitance Double-Gate FinFETs Considering Quantum Capacitance

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ABSTRACT This paper investigates the inversion charge characteristics and quantum-capacitance induced inversion charge loss for $In_{0.53}Ga_{0.47}As$ negative-capacitance FinFETs (NC-FinFETs) using theoretical calculation corroborated with numerical simulation. Our study indicates that, the boost of inversion charges due to negative capacitance increases with increasing remnant polarization P_r. In addition, the inversion-charge boosting for the $In_{0.53}Ga_{0.47}As$ device is significantly larger than that of the Si (110) device due to the step-like inversion capacitance characteristic stemming from the 2D density-of-states of the $In_{0.53}Ga_{0.47}As$ device. In other words, the quantum-capacitance induced inversion-charge loss for III-V channel can be mitigated in NCFETs.

INDEX TERMS Negative-capacitance FET (NCFET), quantum capacitance, FinFET structure, CMOS, InGaAs.

I. INTRODUCTION

With the progress of the nano-electronic circuit miniaturization, lowering power consumption becomes the important roadblock due to the fundamental thermal limit of subthreshold swing for CMOS technologies. Negative-capacitance field-effect transistor (NCFET) [1], especially NC-FinFET [2]–[5] has been considered as one of the most promising beyond-CMOS device candidates for future low-power applications due to its steep slope and similar current transport mechanism to MOSFET. In addition, based on IRDS [6], III-V materials such as $In_{0.53}Ga_{0.47}As$ are considered as attractive channel materials (for nFET) for future technology nodes due to their high electron mobility, and the ultra-thin-body InGaAs NCFET has been reported [7], [8]. However, the quantum capacitance stemming from the small electron effective mass and low density-of-states (DOS) for III-V materials [9] may reduce the intrinsic inversion capacitance (C_{inv}) and the inversion charges (Q_{inv}) which are crucial to drive current [10]–[13]. How might the negative-capacitance action affect the Q_{inv} loss for III-V devices has rarely been known and merits investigation. In this work, using theoretical calculation corroborated with TCAD numerical simulation, we investigate the impact of negative capacitance on the Q_{inv} characteristic and the quantum-capacitance induced Q_{inv} loss for $In_{0.53}Ga_{0.47}As$ and Si (110) NC-FinFETs.

This paper is organized as follows: In Section II, we present our methodology for constructing a quantum mechanical model in calculation of the inversion charge (Q_{inv}) for $In_{0.53}Ga_{0.47}As$ and Si (110) double-gate NC-FinFETs. By using our calculation together with TCAD numerical simulation, we investigate the Q_{inv} characteristics and quantum-capacitance induced Q_{inv} loss for $In_{0.53}Ga_{0.47}As$/Si NC-FinFETs in Section III. Finally, Section V draws the conclusion.

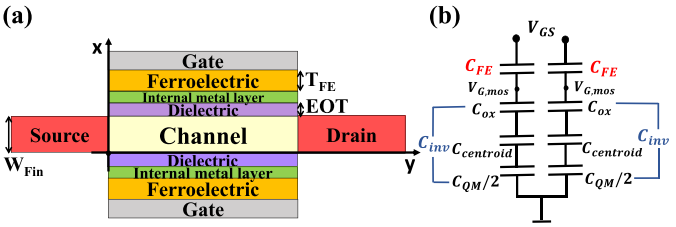

FIGURE 1. (a) Cross-sectional view of a double-gate NC-FinFET structure with the gate-dielectric of the baseline FinFET replaced by the ferroelectric/metal/gate-oxide layer. The doping concentrations of source/drain and channel (N_{ch}) are 6E19 cm^{-3} and 1E15 cm^{-3}, respectively. Abrupt junction is assumed. L_g is channel length. W_{Fin}, T_{FE} and EOT are thicknesses of channel, ferroelectric and equivalent oxide, respectively. (b) Equivalent capacitance network of the NC-FinFET. The C_{FE} and C_{inv} are the ferroelectric capacitance and the inversion capacitance, respectively.

II. METHODOLOGY

A. QUANTUM CAPACITANCE MODEL

Figure 1 (a) shows a schematic sketch of the double-gate NC-FinFET structure in this study. To accurately model the quantum-confinement effect along the fin-width (W_{Fin}) directions, the 2D Schrödinger equation can be expressed as:

$$-\frac{\hbar^2}{2m_x}\frac{\partial^2}{\partial x^2}\psi_j(x) + E_C(x)\psi_j(x) = E_j\psi_j(x) \tag{1}$$

where j is the principle quantum number for the electron quantization along the W_{Fin} directions, E_j the j-th eigen-energy, Ψ_j the corresponding wave-function and m_x the carrier quantization effective mass along the W_{Fin} direction.

To determine the inversion capacitance (C_{inv}), we calculate the gate charge of the double-gate FinFET ($Q_{G,mos}$) (i.e., the internal-gate charge of the NC-FinFET) for each internal-gate voltage ($V_{G,mos}$) based on [13] (see the Appendix). The C_{inv} can be determined by

$$C_{inv} = \frac{dQ_{G,mos}}{dV_{G,mos}} \tag{2}$$

Figure 2 shows that the normalized C_{inv} versus $V_{GT,mos}$ (gate-voltage overdrive of the baseline FinFET) characteristics calculated by our model are in good agreement with the TCAD numerical simulation [14] for $In_{0.53}Ga_{0.47}As$ and Si (110) double-gate FinFETs. It can be seen that the InGaAs-OI device exhibits lower C_{inv} than that of the SOI device. This is due to the quantum capacitance because the $In_{0.53}Ga_{0.47}As$ channel possesses a smaller quantization effective mass than that of Si. Fig. 2(a) also shows that the $In_{0.53}Ga_{0.47}As$ device possesses a step-like C_{inv} characteristic. This is a signature of the energy dependence of 2D DOS [Eqn. (9) in the Appendix].

B. QUANTUM Q_{INV} MODEL FOR NC-FINFET

The inversion charge (Q_{inv}) calculation for the NC-FinFET can be constructed by considering the 1D steady-state Landau-Khalatnikov (L-K) equation [17] for the voltage

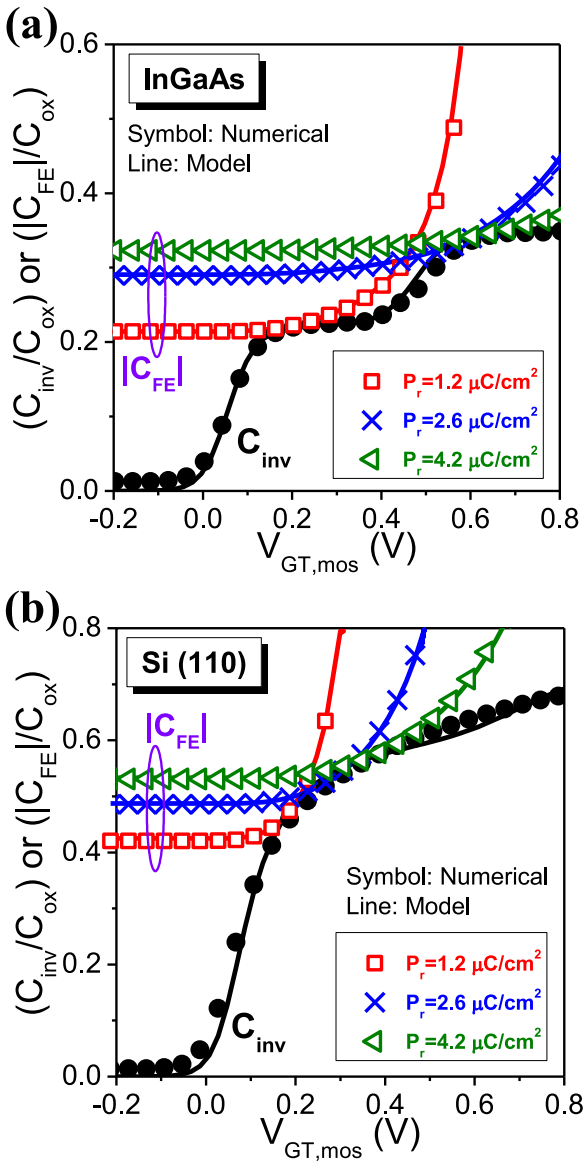

FIGURE 2. Numerically simulated and model-calculated capacitance matching with C_{inv} (normalized with the physical oxide capacitance C_{ox}) versus $V_{GT,mos}$ characteristics with various P_r for (a) $In_{0.53}Ga_{0.47}As$ and (b) Si (110) double-gate FinFET. A quantization effective mass m_x = 0.041m_0 [12] is used for the $In_{0.53}Ga_{0.47}As$ channel.

drop across the ferroelectric layer [see Fig. 1(a)]:

$$V_{FE} = \frac{3\sqrt{3}}{2}T_{FE}E_c\left[-\frac{Q_{G,mos}}{P_r} + \left(\frac{Q_{G,mos}}{P_r}\right)^3\right] \tag{3}$$

where E_c, P_r, and T_{FE} are the coercive field, remnant polarization and ferroelectric thickness, respectively. In Eqn. (3), it is assumed that the internal-gate charge, $Q_{G,mos}$, is approximately equal to the polarization inside the ferroelectric layer. For a given $V_{G,mos}$, $Q_{G,mos}$ can be determined and then the voltage across the ferroelectric, V_{FE}, can be calculated by Eqn. (3). Therefore, the corresponding gate voltage of the NC-FinFET can

be obtained:

$$V_G = V_{G,mos} + V_{FE} \tag{4}$$

From Eqn. (3) the ferroelectric negative capacitance ($C_{FE} = dQ_{G,mos}/dV_{FE}$) can be calculated by

$$\frac{1}{C_{FE}} = \frac{3\sqrt{3}}{2} T_{FE} E_c \left[-\frac{1}{P_r} + \frac{3Q_{G,mos}^2}{P_r^3} \right] \tag{5}$$

Fig. 2 shows that the calculated C_{FE} is fairly accurate, which also verifies the accuracy of $Q_{G,mos}$. The internal-gate charge $Q_{G,mos}$ can be approximated as the inversion charge (Q_{inv}) under strong inversion. Therefore, the quantum Q_{inv} model for the NC-FinFET can be constructed.

To obtain the TCAD numerical characteristics of the NC-FinFETs, we coupled the TCAD simulation [14] with the post-processed 1D steady–state L-K equation (Eqn. (3)). During the procedure, the inversion charge density at each bias point of the baseline FinFET were extracted from the TCAD simulation, which self-consistently solves coupled Poisson–Schrödinger equations. The V_{FE} corresponding to each bias and the inversion charge characteristics of the NC-FinFET can then be obtained by Eqn. (4).

The internal voltage amplification of the NC-FinFET, A_V, can be expressed as (see Fig. 1(b)):

$$A_V = \frac{\partial V_{G,mos}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{inv}} \tag{6}$$

Eqn. (6) indicates that larger A_V can be obtained as $|C_{FE}|$ is close to the C_{inv}. In this work, the T_{FE} is optimized under the constraint of non-hysteresis operation for each P_r (see Fig. 2).

In this work, based on the IRDS 2019 technology node [6], the channel thickness $W_{Fin} = 7$ nm and the equivalent oxide thickness EOT = 0.8 nm are used for the baseline FinFET. We investigate the NC-FinFETs with various P_r under $E_c = 1.4$ MV/cm [18].

III. RESULTS AND DISCUSSION

By using the quantum Q_{inv} model calculation corroborated with TCAD numerical simulation, we investigate the impact of negative-capacitance on the inversion charge (Q_{inv}) characteristics and the quantum-capacitance induced Q_{inv} loss for $In_{0.53}Ga_{0.47}As$ and Si (110) devices in this section. Fig. 3 shows the impact of negative-capacitance on the Q_{inv} versus V_{GT} (gate-voltage overdrive) for $In_{0.53}Ga_{0.47}As$ and Si (110) devices with various P_r. It can be seen that the Q_{inv} boosting mechanism for the NC-FinFET due to the gate-voltage amplification can be well captured by our model. Besides, after the action of negative capacitance, larger value of P_r (= 4.2 μC/cm^2) can achieve larger improvement of Q_{inv}. This can be explained by the capacitance matching as shown in Fig. 2. It shows that the curvature of $|C_{FE}|$ decreases with increasing P_r (due to the $3Q_{inv}^2/P_r^3$ term in Eqn. (5)), which extends the voltage range of $|C_{FE}| \approx C_{inv}$ and improves the A_V (and thus Q_{inv}) significantly.

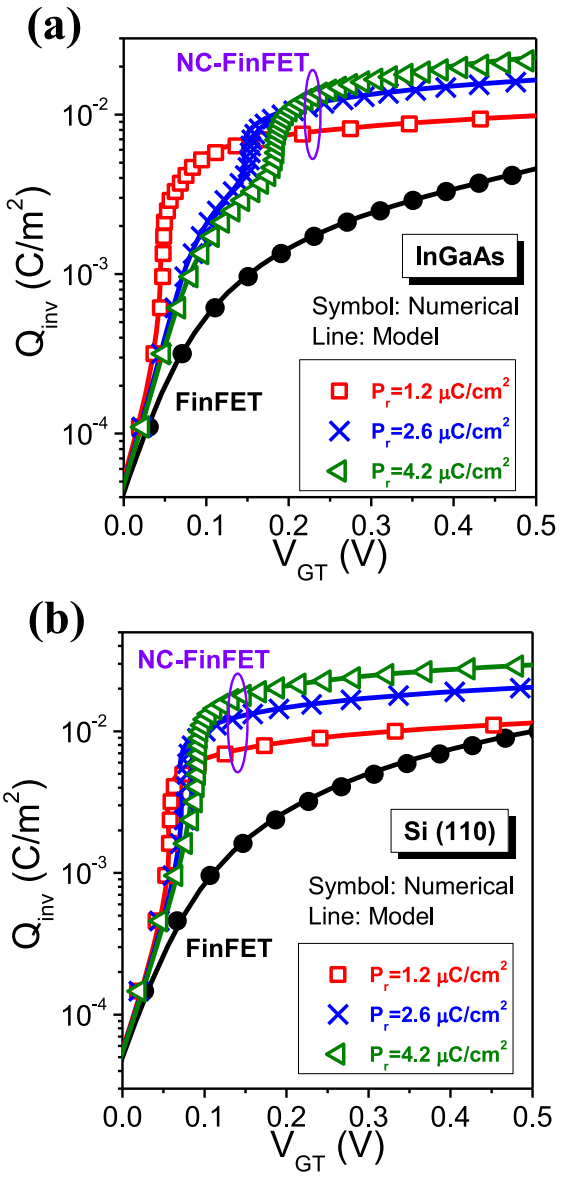

FIGURE 3. Impact of negative capacitance on the Q_{inv} - V_{GT} characteristics with various P_r for (a) $In_{0.53}Ga_{0.47}As$ and (b) Si (110) devices.

Figure 4 shows the negative-capacitance induced Q_{inv} improvement with various P_r for $In_{0.53}Ga_{0.47}As$ and Si (110) devices. The improvement due to the impact of negative-capacitance is defined as the Q_{inv} ratio of NC-FinFET to FinFET (i.e., $Q_{inv,NC}/Q_{inv,Fin}$). It can be seen that the $Q_{inv,NC}/Q_{inv,Fin}$ ratio increases with increasing P_r. Fig. 5 shows the S curve [19] with various P_r for the $In_{0.53}Ga_{0.47}As$ NC-FinFET. It can be seen that larger value of P_r possesses larger negative capacitance region, which means that the voltage amplification can be maintained over a larger voltage range and improves the Q_{inv} characteristics.

Figure 6 shows the impact of negative capacitance on the quantum-capacitance induced Q_{inv} loss at different V_{GT}. It can be seen that the $Q_{inv,Si}/Q_{inv,InGaAs}$ ratio for

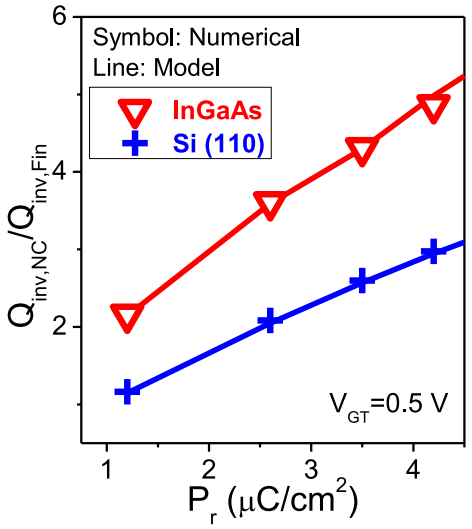

FIGURE 4. Impact of P_r on the negative-capacitance boosted Q_{inv} for $In_{0.53}Ga_{0.47}As$ and Si (110) devices.

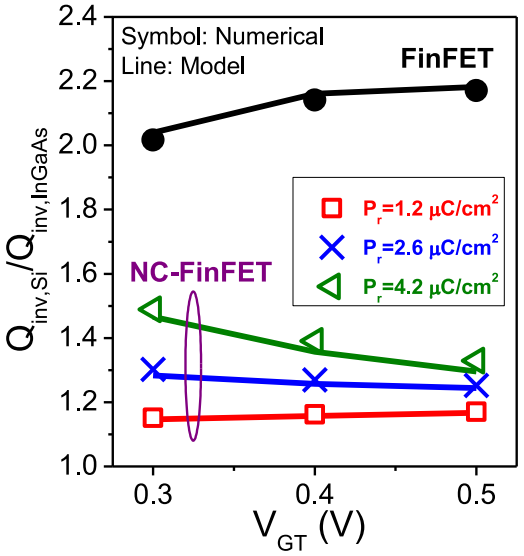

FIGURE 6. Impact of negative capacitance on the quantum-capacitance induced Q_{inv} loss with various P_r at different V_{GT}.

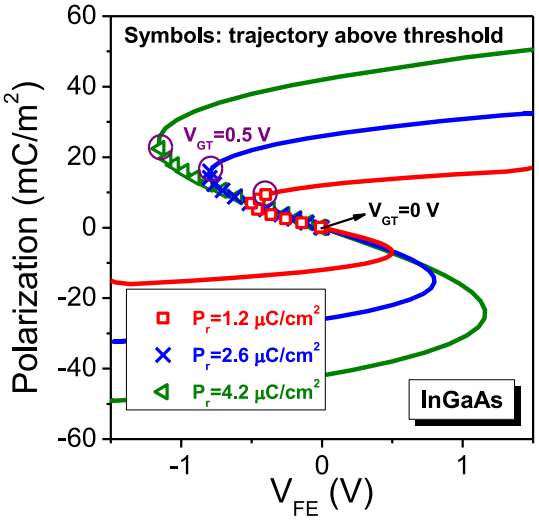

FIGURE 5. Impact of P_r on the S curve for the $In_{0.53}Ga_{0.47}As$ NC-FinFET.

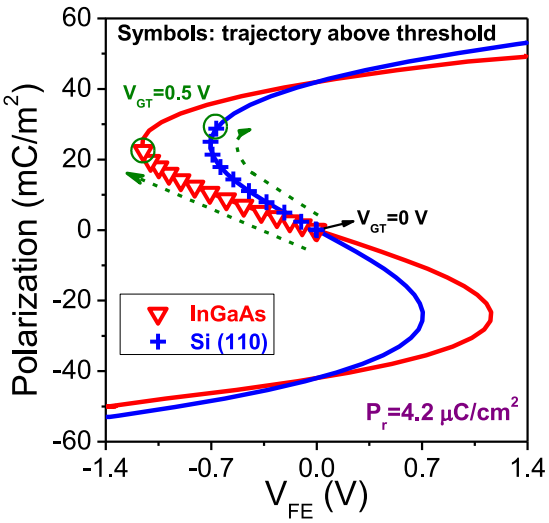

FIGURE 7. S-curve comparison for $In_{0.53}Ga_{0.47}As$ and Si (110) NC-FinFETs.

the NC-FinFET is significantly lower than that of the FinFET. This is because the Q_{inv} boosting for $In_{0.53}Ga_{0.47}As$ channel is significantly larger than that of the Si channel (Fig. 4), and the $In_{0.53}Ga_{0.47}As$ FinFET possesses a step-like C_{inv} characteristic which can provide a better capacitance matching over a larger gate-voltage range and higher A_V above threshold.

Figure 7 compares the S curve for $In_{0.53}Ga_{0.47}As$ and Si (110) NC-FinFETs with $P_r = 4.2$ μC/cm^2. It can be seen that $In_{0.53}Ga_{0.47}As$ device possesses larger negative-capacitance region and the slope of S curve is also smaller (i.e., $|C_{FE}|$ is closer to C_{inv}) than that of the Si device. In other words, the $In_{0.53}Ga_{0.47}As$ NC-FinFET can achieve higher A_V over larger gate-voltage range and results in larger Q_{inv} boost. In other words, the Q_{inv} loss due to quantum capacitance of the III-V device can be mitigated by the action of negative capacitance for NC-FinFETs. Fig. 6 indicates that the needed mobility gain of the FinFET to compensate for the quantum-capacitance induced Q_{inv} loss should be at least ~2.2×, while the needed mobility gain of the NC-FinFET can be reduced to ~1.4× (against the Si one) due to the impact of negative capacitance.

IV. CONCLUSION

Quantum capacitance for low-DOS III-V materials reduces the intrinsic inversion capacitance and the inversion charges, which is crucial to the drive current. We have investigated the inversion charge characteristics and quantum-capacitance induced inversion charge loss for $In_{0.53}Ga_{0.47}As$ NC-FinFETs by using theoretical calculation corroborated with TCAD numerical simulation. We have found that the step-like inversion capacitance characteristic stemming from

the energy dependence of 2D DOS plays a crucial role in capacitance matching. Our study indicates that, the inversion charge boosting due to the impact of negative capacitance increases with increasing remnant polarization P_r. Besides, the inversion charge improvement for the $In_{0.53}Ga_{0.47}As$ device is larger than that of the Si (110) device. The quantum-capacitance induced inversion charge loss can be mitigated from ~2.2× to ~1.4× for the $In_{0.53}Ga_{0.47}As$ NC-FinFET (against the Si counterpart) due to the boost of negative capacitance.

APPENDIX

The gate charge $Q_{G,mos}$ of a double gate FinFET under strong inversion can be expressed as:

$$\begin{aligned} Q_{\mathrm{G,mos}} &= 2C_{\mathrm{oxeff}}\left(V_{\mathrm{G,mos}} - V_{\mathrm{fb}} - \varphi_s\right) \\ &= Q_{\mathrm{inv}} + Q_{\mathrm{bulk}} = Q_{\mathrm{inv}} + qN_{\mathrm{ch}}W_{\mathrm{Fin}} \end{aligned} \tag{7}$$

where $V_{G,mos}$ is the internal-gate bias, V_{fb} the flat-band voltage, ϕ_s the potential at the carrier centroid, and N_{ch} the channel doping concentration. C_{oxeff} is the effective gate oxide capacitance, which has considered the impact of carrier centroids and can be calculated by [12], [13]:

$$C_{oxeff} = \frac{\epsilon_{ox}}{t_{ox} + 0.7\frac{\epsilon_{ox}W_{Fin}}{4\epsilon_{ch}}} \tag{8}$$

where ε_{ox} and ε_{ch} are the permittivity of the gate-dielectric and channel, respectively.

With 1D quantum confinement, the inversion electrons act like the 2D electron gas with the 2D DOS:

$$DOS_{2D}(E) = \sum_j \frac{m_{dos}}{\pi\hbar^2} \tag{9}$$

where m_{dos} is the DOS effective mass and $m_{dos} = m_x = 0.041m_0$ for isotropic $In_{0.53}Ga_{0.47}As$. The inversion charge can be calculated by [13], [15]:

$$\begin{aligned} Q_{inv} &= q\int_{E_j}^{\infty} DOS_{2D}(E)f_{FD}(E)dE \\ &= \sum_j \frac{kT}{q}C_{QM}ln\left[1 + exp\left(\frac{\varphi_s - \frac{E_j}{q} - \frac{E_g}{2q}}{V_T}\right)\right] \end{aligned} \tag{10}$$

where C_{QM} is quantum capacitance ($= q^2m_x/\pi\hbar^2$), $f_{FD}(E)$ is the Fermi–Dirac distribution function and E_g is the band-gap. E_j is the j-th eigen-energy and can be determined by the Eqn. (1) under the flat-well approximation [12], [16].

Therefore, for a given internal-gate voltage ($V_{G,mos}$), ϕ_s can be solved from the Eqn. (7) and Eqn. (10) by iteration. Then the internal-gate charge $Q_{G,mos}$ can be obtained (Eqn. (7)).

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