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Investigation of Self-Heating Effect on DC and RF Performances in AlGaN/GaN HEMTs on CVD-Diamond

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ABSTRACT Abstract-We have investigated the self-heating effect on DC and RF performances of identically fabricated AlGaN/GaN HEMTs on CVD-Diamond (GaN/Dia) and Si (GaN/Si) substrates. Self-heating induced device performances were extracted at different values drain bias voltage (V_D) and dissipated DC power density (P_D) in continuous wave (CW) operating condition. The effect of self-heating was observed much lesser in GaN/Dia HEMTs than GaN/Si HEMTs in terms of I_D, I_G, g_m, f_T and f_{max} reduction. Increased channel temperature caused by joule heating at high P_D reduces the 2-DEG carrier mobility in the channel of the device. This behaviour was also confirmed by TCAD simulation which showed ~3.9-times lower rising rate of maximum channel temperature and lowers thermal resistance (R_{th}) in GaN/Dia HEMTs than GaN/Si HEMTs. Small signal measurements and equivalent circuit parameter extraction were done to analyze the variation in performance of the devices. Our investigation reveals that the GaN/Dia HEMT is a promising candidate for high power density CW operation without significant reduction in electrical performance in a large drain bias range.

INDEX TERMS AlGaN/GaN, HEMT, CVD-diamond, self-heating, DC, RF and TCAD.

I. INTRODUCTION

AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising candidates for high power continuous wave (CW) operations in compact solid-state power amplifier (SSPA) modules which are ideal for civil avionics, communications, industrial, scientific, and medical applications. GaN HEMTs have the desirable intrinsic capacity of handling large current and power densities due to its unique material properties such as large band gap, high electron velocity and critical breakdown field [1]. However, thermal management, size reduction and long term reliable operation for GaN-based devices are some of the major challenges, especially when the device is operating at high drain bias voltage (e.g., V_D 28-48 V). High drain bias voltage causes a higher longitudinal electric field at the gate edge of the gate-drain region near the AlGaN/GaN interface. Under such condition, a large electric field exists at the gate edge near the 2-dimensional electron gas (2-DEG) of AlGaN/GaN interface [2]. The scattering of 2-DEG electrons with the generated phonons leads to large joule heating (self-heating) and increasing the lattice temperature locally (called hot spot) [3], [4]. Self-heating effect becomes more prominent when device size further reduces, mainly by lowering gate-drain spacing (L_{gd}), the gate to gate pitch (L_{gg}). Here, substrate plays an important medium for transporting the joule heat away from the hot spot region of the device. However, poor heat emission from conventional substrates (e.g., Si, Sapphire) further accelerates self-heating, which causes additional phonon scattering in the channel and degrades the 2-DEG effective carrier mobility (μ_{eff}). This eventually leads to degraded DC and RF performance with an increase in V_D.

To avoid self-heating effect, a superior thermal conductive material such as Diamond (10-20 W/cm-K) [5], has been employed as a substrate to dissipate the generated heat from the active region of the device. Researchers have also

reported AlGaN/GaN HEMTs on Diamond with dissipated DC power density ($P_D = V_D \times I_D$) of 22 W/mm (CW) [6], and 24 W/mm in pulse condition as well as 3.6-times higher RF power capability over GaN/SiC HEMTs [7]. These results show the strong manifestation of exploiting best transport properties of GaN HEMT by using Diamond as a substrate. However, the bias conditions effect on self-heating and transport properties in AlGaN/GaN HEMTs-on-Diamond have not been reported so far. Such work is inevitable for developing the electrical and thermal model of device as well as understanding the operating limit of GaN HEMTs for next-generation high power DC and RF application. In this work, we systematically investigated the self-heating effect on DC and RF performance with increasing the drain bias voltage and quantitatively analysed the results under increasing dissipated DC power density ($P_D = V_D \times I_D$). Results were also compared and analysed with identical GaN HEMTs fabricated on Si (111) (low thermal conductive substrate, ~1.5 W/cm.K). For a fair comparison of electrical performances, GaN HEMT on-Si was selected with similar 2-DEG property and identical device dimensions in this study. However, buffer thickness is higher in GaN/Si HEMT than GaN/Dia HEMT. Effect of this difference in channel temperature was also simulated.

II. DEVICE FABRICATION

Figure 1 shows the schematic cross-sectional diagram of (a) GaN/Dia HEMT and (b) GaN/Si HEMTs. GaN/Dia (GaN/Si) HEMT exhibited an average room temperature 2-DEG mobility (μ) of 1502 (1450) $cm^2V^{-1}s^{-1}$, sheet carrier density (n_s) (of 0.97×10^{13}(1.0×10^{13}) cm^{-2} and an average sheet resistance of 422 (430) ohm/sq. with a variation of ±3% over the full 4-inch wafer. The product of μ and n_s ($\mu \times n_s$) is almost the same for GaN/Si (1.450×10^{16} $V^{-1}.s^{-1}$) and GaN/Dia (1.457×10^{16} $V^{-1}.s^{-1}$). The device fabrication started with the mesa isolation using BCl_3/Cl_2 plasma. The ohmic contact was formed by depositing conventional Ti/Al/Ni/Au metal stacks followed by rapid thermal annealing at 825 °C for 30s in an N_2 atmosphere. Next, the Ni/Au (150/300 nm) gate metalization was formed using conventional lithography and e-beam evaporation followed by a lift-off process. Further, thick Ti/Au (50/1000 nm) metalization was done to withstand high power density during operation. The devices were then passivated with 120-nm-thick SiN using plasma-enhanced chemical vapor deposition (PECVD). In this study, we have used the device dimensions of $L_{sg}/W_g/L_g/L_{gd} = 2/(2 \times 100)/2/3\mu$m for both GaN/Si and GaN/Dia HEMTs. The DC and RF characterization were done on the device, in similar measurements condition, using Agilent B1505A semiconductor parameter analyzer and Keysight N5244A PNA-X network analyzer, respectively.

III. RESULTS AND DISCUSSIONS

Figure 2 (a) shows the DC I_D-V_D and of GaN/Dia and GaN/Si HEMTs with $L_g/W_g = 2/(2 \times 100)$ μm.

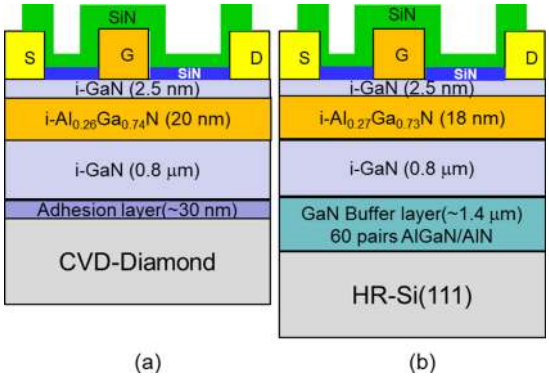

FIGURE 1. Cross-sectional schematic diagram of AlGaN/GaN HEMTs on (a) CVD-Diamond substrate (b) Si (111) substrate.

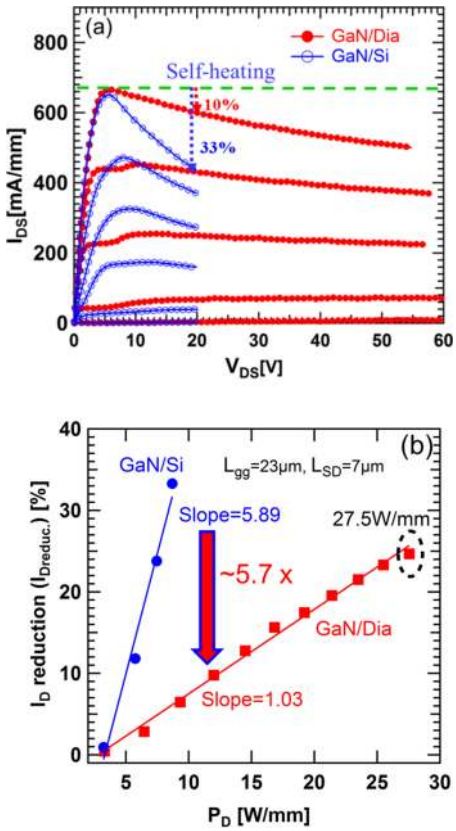

FIGURE 2. (a) I_{DS}-V_{DS}, (b) I_D reduction ($I_{Dreduc.}$) versus DC P_D of GaN/Dia and GaN/Si HEMTs. Device dimensions: $L_{sg}/W_g/L_g/L_{gd} = 2/(2 \times 100)/2/3$ with $L_{gg} = 23$ um.

GaN/Dia HEMTs were measured up to $V_D = 60$ V whereas GaN/Si HEMTs were measured up to $V_D = 20$ V at $V_G = +1$ V to avoid on-state device breakdown. The GaN/Si and GaN/Dia HEMTs exhibited maximum drain current density (I_{Dmax}) of 652 and 662 mA/mm respectively. As we can see in Figure 2(a), GaN/Si suffered a significant reduction of I_D beyond the maximum current density (I_{Dmax}) as compared to GaN/Dia. The I_D reduction rate at $V_g = +1$V was obtained as 15 mA/mm.V and 3.3 mA/mm.V for GaN/Si and GaN/Dia respectively.

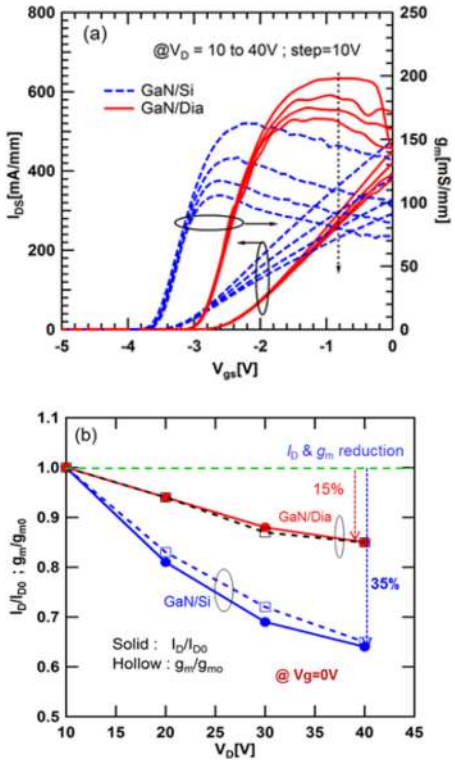

FIGURE 3. **(a) Transfer characteristics of GaN/Dia and GaN/Si HEMTs at different V_D (b) Normalized I_{dmax} and g_{mmax} reduction at different V_D.**

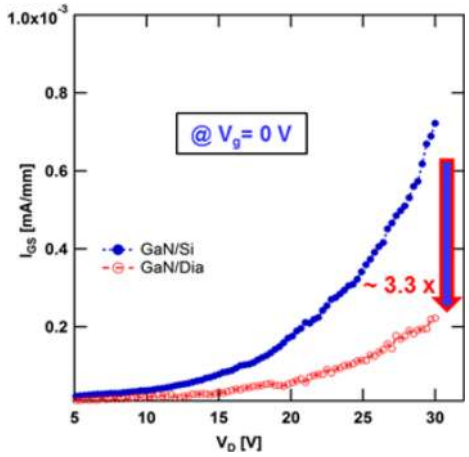

FIGURE 4. **Gate current characteristics of GaN/Dia and GaN/Si HEMTs with V_D at $V_G = 0$ V.**

The GaN/Dia HEMT shows a much smaller percentage of drain current reduction which is 10 % compared to the 33 % in GaN/Si HEMTs (see Fig. 2(a)). Our result of I_D reduction (17.7 % at $V_D = 55$ V, $V_g = 0$) was also compared with the reported value in GaN/SiC HEMTs ($\sim$ 27 %) [8], correlating to the much lower self-heating effect in our GaN/Dia HEMTs. Hence, it is evident that self-heating induced $I_{Dreduc.the}$ rate in GaN/Dia HEMTs is much lower than GaN/Si and GaN/SiC HEMTs. The dissipated DC power density (P_D) in GaN/Dia was calculated as 27.56 W/mm ($V_D = 55$ V) as compared to the 8.7 W/mm ($V_D = 20$ V) in GaN/Si. The $I_{Dreduc.}$ rate in GaN/Dia is $\sim$ 1 % / W.mm^{-1} as compared to 5.89% /W.mm^{-1} in GaN/Si HEMTs, which is $\sim$5.7-times lower rate of I_{Dreduc} in GaN/Dia as compared to GaN/Si (see Fig. 2(b)). It is worth to mention that GaN/Dia sustained a higher P_D of 27.56 W/mm even without on-state breakdown. Whereas GaN/Si was burnt around $\sim$9 W/mm of DC P_D, could be due to intense self-heating and increased channel temperature in GaN/Si. Such inherent characteristics make GaN/Dia transistor very suitable for high power CW operation.

In addition to I_{Dreduc}, maximum transconductance (g_{mmax}) and maximum drain current density (at $V_G = 0$ V) I_{Dreduc} were analyzed from the measured transfer characteristics. By limiting the V_G up to 0 V, we increased the CW V_D up to 40 V for GaN/Si and device was measured without observing catastrophic failure. The HEMTs exhibited peak extrinsic transconductance (g_{mmax}) of 162 and 199 mS/mm for GaN/Si and GaN Dia respectively at $V_D = 10$ V(See Fig. 3(a)). We can clearly observe that as V_D increases, the g_{mmax} decreases. Further analysis was done for the drain bias dependent I_{Dmax} (at $V_g = 0$ V, $V_D = 10 - 40$ V) andg_{mmax} reduction. The percentage of I_D reduction ($I_{Dreduc.}$) was calculated based on the formula: $I_{Dreduc.} = ((I_{Dmax} - I_{D-Vd})/I_{Dmax}) \times 100$. The I_{Dmax} is the maximum I_D value from transfer characteristics at $V_D = 10$ V and I_{D-vd} is taken as maximum I_D at a particular V_D for the calculation of $I_{Dreduc.}$. Similarly, the g_{mmax} reduction [$g_{mreduc.} = (g_{mmax} - g_{m-vd}) \times 100/g_{mmax}$] ($g_{mmax}$ is the maximum g_m value from transfer characteristics at $V_D = 10$ V and g_{m-vd} is taken as maximum g_m at a particular V_D for the calculation of $g_{mreduc.}$) was also calculated. The $g_{mreduc.}$ was found to be 15 % and 35 % at $V_D = 40$ V with the rate of 1.0 mS/mm.V^{-1} and 1.9 mS/mm.V^{-1} respectively for GaN/Dia and GaN/Si HEMTs (See Fig. 3(b)). Similar reduction in g_{mmax} and I_{Dmax} in GaN/Dia HEMT was observed which could be associated with mobility degradation. Lower g_{mmax} reduction of GaN/Dia also indicates a lower reduction of effective mobility (μ_{eff}) which was extracted further in this work. Lower $I_{Dreduc.}$ and$g_{mreduc.}$ in GaN/Dia HEMTs confirms the low self-heating effect in the device which is due to the efficient heat dissipation through the Diamond substrate. Therefore, GaN/Dia enables the device to operate at higher V_D without much compromise of current density and transconductance, which is key requirements for devices operating at higher CW power. In addition to the I_D and g_m, gate current was also measured on the same device with increasing V_D at $V_G = 0$ V.

Figure 4 shows the I_G versus V_D for both GaN/Si and GaN/Dia HEMTs. From Fig. 4, it is clear that I_G is increasing at a higher rate in GaN/Si than GaN/Dia under similar longitudinal electric field condition. However, I_g increase is more prominent at $V_D >\sim 15$ V. This increase of I_G could be due to the increased channel temperature at higher drain bias voltage. Increased gate current with temperature was reported in the literature which is due to temperature assisted

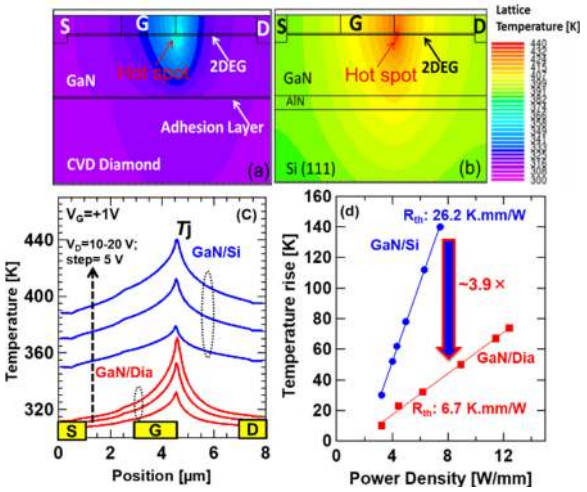

FIGURE 5. TCAD Simulated cross sectional thermal profile for (a) GaN/Dia, (b) GaN/Si at $V_D = 20$V, $V_G = +1$V, (c) device temperature profile across source-drain region for different $V_D = 10$, 15 and 20 V (d) ΔT_j versus P_D of GaN/Dia and GaN/Si HEMTs.

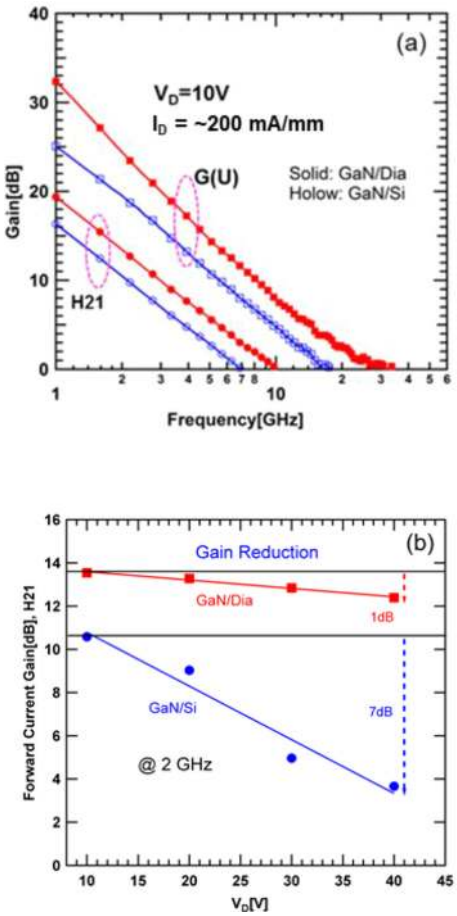

FIGURE 6. (a) Small-signal characteristics, (b) Current gain (H_{21}) of GaN/Dia and GaN/Si HEMTs for different V_D of a 2-μm gate GaN/Dia and GaN/Si HEMTs.

tunnelling [9], [10]. The rate of I_G increase in GaN/Dia is obtained ~3-times lower than GaN/Si. Lower rise of I_G with V_D implies higher gate stability and reliable device performance at high voltage operation of GaN/Dia.

In order to investigate the bias dependent temperature distribution in these devices, 2D TCAD simulation (SILVACO) was also performed using the GIGA module consistently with BLAZE [11]. The thermal boundary conditions can be expressed as

$$(J_{tot}.s) = \frac{1}{R_{th}}\left(T - T_{ref}\right)$$

where J_{tot} is the total energy flux, s is the unit external normal of the boundary, T_{ref} is the reference boundary condition of the thermo-contact in the simulation environment, and Rth is the material-dependent thermal resistance. In our simulation, the bottom of the devices is used as the reference thermo-contact at 300 K.

Fig. 5(a) and 5(b) shows the lattice temperature profile of the GaN/Dia and GaN/Si HEMTs, respectively. The highest temperature in the channel (Hot spot) is referred here as junction temperature (T_j). From the temperature scale, it is clear that GaN/Dia has much lower temperature as compared to GaN/Si HEMTs.

The obtained temperature profile across the device channel from source to drain clearly indicates (See Fig. 5(a)) that the GaN/Si HEMTs has T_j of 440 K, whereas it is 370 K in the GaN/Dia HEMTs. The observation of lower T_j of 70 K in GaN/Dia HEMTs means it can further operate at higher P_D. Fig. 5(c) shows the junction temperature rise (ΔT_j) of the device with P_D. From the figure, it is clear that the junction temperature rises more rapidly in GaN/Si HEMT (140 K) than GaN/Dia HEMT (36 K) at P_D (7 W/mm). A similar trend of temperature rise (ΔT_j) in GaN/Dia HEMTs was also observed by Pomeroy *et al.* [12]. Thermal resistance (R_{th}) values were calculated from the slope of the rise of junction temperature versus P_D for both GaN/Dia (6.7 K.mm/W) and GaN/Si (26.2 K.mm/W) HEMTs (See Fig. 5(d)). The extracted values of R_{th} were closely matched the reported values (~6.5 K.mm/W) for GaN/Dia HEMTs [13], and (24.6 K.mm/W) for GaN/Si HEMTs [14]. The GaN/Dia shows ~3.9-times lower R_{th} value than GaN/Si HEMTs. This is in good agreement with the reported results by Pomeroy *et al.* [15]. The R_{th} of GaN/Dia can further be minimized by optimizing the interface layer between GaN and CVD-Diamond [16].

We also performed the small-signal measurements on both the HEMTs from $V_D = 10-40$ V. Fig. 6 (a) shows the small-signal microwave characteristics of GaN/Dia and GaN/Si HEMTs. At $V_D = 10$V, the GaN/Dia and GaN/Si HEMTs exhibited a unity current gain cutoff frequency (f_T) of 10.2 GHz and 7.0 GHz and a maximum oscillation frequency (f_{max}) of 31.4 GHz and 18.2 GHz, respectively. The forward current gain (H_{21}) was deduced from measured S-parameters at different V_D. At 2 GHz, about 1.0 dB reduction of H_{21} was observed in GaN/Dia HEMT when compared to 7 dB reduction in GaN/Si HEMTs from $V_D = 10 - 40$ V, (See Fig. 6(b)).

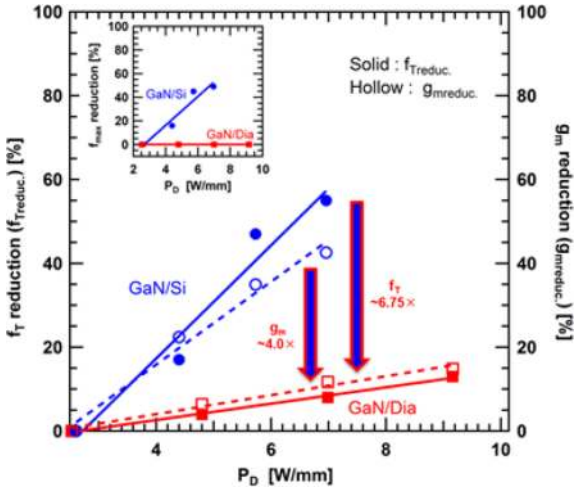

FIGURE 7. The f_T reduction ($f_{Treduc.}$) and gmmax reduction ($g_{mreduc.}$) versus P_D of GaN/Dia and GaN/Si HEMTs. Inset: f_{max} reduction ($f_{maxreduc.}$) versus P_D for GaN/Dia and GaN/Si HEMTs.

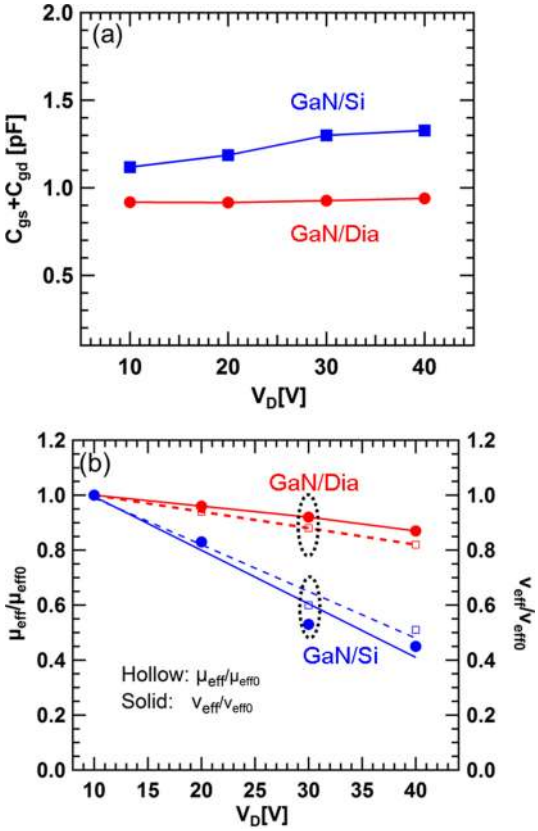

FIGURE 8. (a) Extracted gate capacitance from measured small-signal characteristics and (b) normalized effective carrier mobility and effective carrier velocity versus drain bias characteristics V_D of a 2-μm gate GaN/Dia and GaN/Si HEMTs.

Almost constant small signal gain for $V_D = 10-40$ V in GaN/Dia offers a better choice for developing high-power high-frequency amplifier required for a large range of drain bias operation. The f_T and f_{max} were also evaluated for different V_D from 10 - 40V, the I_d was fixed ~200 mA/mm where both the devices exhibited maximum g_m., for GaN/Dia and GaN/Si respectively as f_T was obtained highest at these gate bias voltage. The f_T reduction ($f_{Treduc.}$) was calculated using the formula $f_{Treduc.} = (f_{Tmax} - f_{T-vd}) \times 100/f_{Tmax}$ (f_{Tmax} is maximum f_T value measured at $V_D = 10$ V and f_{T-vd} is the f_T obtained at different V_D). Fig. 7 shows the $f_{Treduc.}$ and$g_{mreduc.}$ versus P_D for both GaN/Dia and GaN/Si HEMTs. At 7 W/mm, GaN/Dia HEMTs exhibited only 8.2 % of $f_{Treduc.}$ whereas GaN/Si HEMTs exhibited much higher $f_{Treduc.}$ of 55%. This f_T ($f_T = g_m/2pi(C_{gs} + C_{gd})$) reduction is predominantly due to the g_m reduction (42%) in GaN/Si devices. The additional reduction of 13% in f_T could be attributed to the slight increase of $C_{gs} + C_{gd}$, as was observed for GaN on Si devices. It is also clear that the GaN/Dia HEMTs has ~6.75-times lower $f_{Treduc.}$ rate with P_D as compared to GaN/Si HEMTs. It is also clear that GaN/Si HEMTs has larger $f_{Treduc.}$ than $g_{mreduc.}$ at higher V_D whereas GaN/Dia HEMTs has an almost similar rate of $f_{Treduc.}$ and $g_{mreduc.}$ The reduction of f_{max} with increasing V_D was also calculated using the formula; ($f_{maxreduc.} = (f_{max(max)} - f_{max-vd}) \times 100/f_{Tmax}$). Where $f_{max(max)}$ is the f_{max} obtained at $V_D = 10$ V and f_{max-vd} is f_{max} obtained at a particular V_D. The inset of Fig. 7 shows the $f_{maxreduc}$ for both GaN/Si and GaN/Dia HEMTs. The $f_{maxreduc.}$ was obtained to be 49 % in the GaN/Si HEMTs while no significant reduction was observed in GaN/Dia HEMTs.

To confirm this, small-signal equivalent circuit parameters were extracted, from measured S-parameter at different V_D, following the proposed model in the literature [17]. We observed that the intrinsic parameters, mainly g_m intrinsic (g_{mo}), C_{gs} and C_{gd} were affected more significantly at high V_D which is due to increased junction temperature in the device. Extrinsic parameters have relatively less effect in small-signal performance in our device. It could be due to alower rise of temperature in the parasitic area of the device than hot spot region (See Fig. 5 (a,b)). However, a small increase in drain resistance (R_d) was also observed at higher V_D. Similar behaviour of extrinsic parameters with temperature has been reported in the published work [18]. The extracted C_g ($C_{gs} + C_{gd}$) at different V_D was shown in Figure 8(a). A small increase of C_g (~3 %) was observed in GaN/Dia as compared to ~16 % increase in GaN/Si. Large reduction of f_T in GaN/Si is due to the reduction of g_m and increase of C_g as f_T ($f_T \alpha (1/C_g)$). Higher increase of C_{gs} in GaN/Si could be linked to the large junction temperature (T_j) at higher V_D (See Fig. 5(c)). The increase of C_{gs} with temperature in AlGaN/GaN HEMTs have also been reported by Cuerdo *et al.* [19]. Which could be related to changes occurred in SiN passivate and AlGaN permittivities [19], [20].

We observed a decreasing trend of C_{gd} with V_D. Similar trend of C_{gd} was reported in other published works [21], [22]. Which could be due to the extension of the depletion region towards the drain side with an increase of

V_D [22]. The reduction of C_{gd} can help to improve the f_{max} at higher V_D [23]. Further, effective carrier mobility (μ_{eff}) was estimated from the extracted g_{mo} which is associated with the device channel and can be expressed as $g_{mo} = (\mu_{eff} C_{gs} \times W/L)(V_G - V_{TH}))$, where W is the gate width (200 μm) and L is the gate length (2 μm), V_{TH} is the threshold voltage of device. Both μ_{eff} and v_{eff} (effective carrier velocity) were also calculated from the extracted small-signal equivalent circuit parameters for both GaN/Si and GaN/Dia. The normalized μ_{eff} and v_{eff} versus V_D were plotted for both the HEMTs (See Fig. 8(b)). Around 55 % reduction of μ_{eff} was observed in GaN/Si as compared to 18% in the case of GaN/Dia. Comparatively higher reduction of μ_{eff} in GaN/Si occurred due to increased T_j at higher V_D. Extracted effective 2-DEG mobility with temperature in GaN HEMT has shown a similar trend in the reported literature [24]. These results show that GaN/Dia HEMTs suffers $\sim$ 3-times lower rate of μ_{eff} reduction which is due to the lower rise of junction temperature at increased V_D.

IV. CONCLUSION

In conclusion, we have quantitatively investigated the self-heating effect on DC and RF performances of identically fabricated AlGaN/GaN HEMTs on CVD-Diamond and Si substrates. Self-heating induced device performances were extracted at different values of dissipated DC power density (P_D) in continuous wave (CW) operating condition. The GaN/Dia HEMTs exhibited $\sim$5.7-times lower rate of $I_{Dreduc.}$ than GaN/Si HEMTs. This behaviour was also confirmed by 2D device simulation which showed $\sim$3.9-times lower rate of increase in junction temperature and lowers thermal resistance (R_{th}) in GaN/Dia HEMTs in comparison with GaN/Si HEMTs. The $f_{Treduc.}$ rate was $\sim$6.75-times lower in the case of GaN/Dia than GaN/Si HEMTs whereas no significant reduction of f_{max} was observed in GaN/Dia HEMTs. Comparatively lower reduction rate ($\sim$3-times) of μ_{eff} and v_{eff} in GaN/Dia made its performance less degraded ($\sim$15%) as compared to ($\sim$50%) GaN/Si. These results show that GaN/Dia HEMTs can be operated even at higher V_D as well as at higher P_D which are paramount features for developing compact high power SSPAs for CW application.

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REFERENCES

[1] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.
[2] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, Aug. 2001.
[3] V. O. Turin and A. A. Balandin, "Performance degradation of GaN field-effect transistors due to thermal boundary resistance at GaN/substrate interface," *Electron. Lett.*, vol. 40, no. 1, pp. 81–83, 2004.
[4] J. Kuzmik, R. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, "Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1496–1498, Aug. 2002.
[5] G. D. Via *et al.*, "Wafer−scale GaN HEMT performance enhancement by diamond substrate integration," *physica Status Solidi (c)*, vol. 11, nos. 3–4, pp. 871–874, 2014.
[6] D. C. Dumka, T. M. Chou, F. Faili, D. Francis, and F. Ejeckam, "AlGaN/GaN HEMTs on diamond substrate with over 7W/mm output power density at 10 GHz," *Electron. Lett.*, vol. 49, no. 20, pp. 1298–1299, 2013.
[7] P.-C. Chao *et al.*, "Low-temperature bonded GaN-on-diamond HEMTs with 11 W/mm output power at 10 GHz," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3658–3664, Nov. 2015.
[8] K. Takagi *et al.*, "Ku-band AlGaN/GaN-HEMT with over 30% of PAE," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, 2009, pp. 457–460.
[9] A. P. Zhang *et al.*, "Temperature dependence and current transport mechanisms in AlGaN Schottky rectifiers," *Appl. Phys. Lett.*, vol. 76, pp. 3816–3818, 2000.
[10] S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "Temperature dependence of gate–leakage current in AlGaN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 82, no. 18, pp. 3110–3112, 2003.
[11] *ATLAS User's Manual Device Simulation Software*, Silvaco, Santa Clara, CA, USA, 2010.
[12] J. W. Pomeroy, M. Bernardoni, D. C. Dumka, D. M. Fanning, and M. Kuball, "Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping," *Appl. Phys. Lett.*, vol. 104, no. 8, 2014, Art. no. 083513.
[13] S. Martin-Horcajo, A. Wang, M.-F. Romero, M. J. Tadjer, and F. Calle, "Simple and accurate method to estimate channel temperature and thermal resistance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4105–4111, Dec. 2013.
[14] S. Arulkumaran *et al.*, "Temperature dependent microwave performance of AlGaN/GaN high-electron-mobility transistors on high-resistivity silicon substrate," *Thin Solid Films*, vol. 515, no. 10, pp. 4517–4521, 2007.
[15] J. Pomeroy *et al.*, "Achieving the best thermal performance for GaN-on-diamond," in *Proc. IEEE Compd. Semicond. Integr. Circuit Symp. (CSICS)*, Monterey, CA, USA, 2013, pp. 1–4.
[16] H. Sun *et al.*, "Reducing GaN-on-diamond interfacial thermal resistance for high power transistor applications," *Appl. Phys. Lett.*, vol. 106, no. 11, 2015, Art. no. 111906.
[17] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-36, no. 7, pp. 1151–1159, Jul. 1988.
[18] M. A. Alim, A. A. Rezazadeh, and C. Gaquiere, "Thermal characterization of DC and small-signal parameters of 150 nm and 250 nm gate-length AlGaN/GaN HEMTs grown on a SiC substrate," *Semicond. Sci. Technol.*, vol. 30, no. 12, 2015, Art. no. 125005.
[19] R. Cuerdo *et al.*, "High-temperature microwave performance of submicron AlGaN/GaN HEMTs on SiC," *IEEE Electron Device Lett.*, vol. 30, no. 8, pp. 808–810, Aug. 2009.
[20] R. Aggarwal, A. Agrawal, M. Gupta, and R. S. Gupta, "Investigation of temperature dependent microwave performance of AlGaN/GaN MISHFETs for high power wireless applications," in *Proc. IEEE Int. Conf. Recent Adv. Microw. Theory Appl.*, Jaipur, India, 2008, pp. 66–68.
[21] B. Green, K. Moore, D. Hill, M. C. Debaca, J. Schultz, B. Noori, M. Bokatius, "Gallium nitride RF technology advances and applications," *Edicon-China*, 2014.
[22] Z. H. Liu *et al.*, "Comprehensive study on the bias-dependent equivalent-circuit elements affected by PECVD SiN passivation in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 473–479, Feb. 2011.
[23] W. Chong, H. Yun-Long, Z. Xue-Feng, M. Xiao-Hua, Z. Jin-Cheng, and H. Yue, "AlGaN/GaN high-electron-mobility transistors with transparent gates by Al-doped ZnO," *Chinese Phys. B*, vol. 22, no. 6, 2013, Art. no. 068503.
[24] R. Menozzi *et al.*, "Temperature-dependent characterization of AlGaN/GaN HEMTs: Thermal and source/drain resistances," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 255–264, Jun. 2008.