Investigation of Silicon Nanowire Gate-All-Around Junctionless Transistors Built on a Bulk Substrate

Dong-Il Moon, Sung-Jin Choi, Juan Pablo Duarte, and Yang-Kyu Choi

***Abstract*— A silicon nanowire (Si-NW) with a gate-all-around (GAA) structure is implemented on a bulk wafer for a junctionless (JL) field-effect transistor (FET). A suspended Si-NW from the bulk-Si is realized using a deep reactive ion etching (RIE) process. The RIE process is iteratively applied to make multiply stacked Si-NWs, which can increase the on-state current when amplified with the number of iterations or enable integration of 3-D stacked Flash memory. The fabricated JL FETs exhibit excellent electrostatic control with the aid of the GAA and junction-free structure. The influence on device characteristics according to the channel dimensions and additional doping at the source and drain extension are studied for various geometric structures of the Si-NW.**

***Index Terms*— Bosch process, bulk MOSFET, corner effect, deep reactive ion etching (RIE), extension doping, gate-all-around (GAA), junctionless (JL) transistor, short-channel effects (SCEs), vertically stacked silicon nanowire (Si-NW).**

I. Introduction

A SILICON nanowire (Si-NW) field-effect transistor (FET) without junctions has recently been proposed as an alternative to the conventional junction-embedded FET that contains a p-n junction at both the source and drain (S/D) [1], [2]. By virtue of its junction-free nature, the junctionless (JL) FET has potential advantages compared to the conventional FET such as reduced fabrication complexity due to a low thermal budget and elimination of the requirement of a shallow and abrupt junction, improved immunity against short-channel effects (SCEs), and less stringent demand to reduce the gate dielectric thickness [1]–[5]. Nevertheless, one of the challenging issues pertaining to the JL FET stems from contradictory demands: a narrow channel for the fully depleted (FD) body to turn off in conjunction with a high-doping concentration. The former is crucial for off-state characteristics, and the latter is important for the on-state current and reduction of the parasitic resistance to the greatest extent possible in S/D extensions. Note that the aforementioned issues can result in an unwanted partially depleted region in the channel. On the one hand, the JL FET was initially demonstrated on a silicon-on-insulator (SOI) substrate, because the thickness of the channel (T_{ch}) on a SOI substrate is readily scaled down. However, this adversely increases the fabrication cost and leads to noncompatibility with standard CMOS technology implemented on a bulk substrate. To overcome these issues, JL FETs have been proposed on a bulk silicon substrate [6]–[8]. Among 3-D device structures, a gate-all-around (GAA) transistor assisted by excellent electrostatic controllability is considered to be an ultimately scaled device. The GAA is especially attractive for the JL FET from a structural point of view, because it can alleviate the strict requirement of reducing T_{ch}, which is indispensable to ensure that the inherently heavily doped channel is FD. Therefore, the GAA JL FET built on a silicon bulk substrate is a timely and important development. In this aspect, a recently proposed method for the formation of a Si-NW on the bulk substrate, known as the Bosch process, can be utilized to fabricate a JL FET with a GAA structure [9]–[11]. On the other hand, in the GAA structure, a narrow Si-NW serves as a channel. Accordingly, the shape of the Si-NW is important, because the JL FET has variability issues [12]. In the JL FET, the parasitic series resistance that arises from the relatively low-doping concentration (approximately 10^{19} cm^{-3}) at the S/D can be problematic compared to a conventional junction-embedded transistor. Additional doping at the S/D extension can reduce the parasitic resistance and thus enhance the on-state current [4]. However, a detailed study that takes into account the Si-NW geometry and extra doping at the S/D extension has not yet been reported.

In this paper, a GAA JL FET composed of a Si-NW formed by a one-step dry etching route is demonstrated on a bulk substrate. The proposed fabrication method can also be used for multiply stacked 3-D Si-NW devices. Typical electrostatic properties of n-type JL transistors are presented. The effects that arise from various channel dimensions, the shape of the Si-NW, and extra doping at the S/D extension are also investigated.

II. Device Fabrication

A schematic illustration of the one-step dry etching route used to form the Si-NW and an obtained result are shown in Fig. 1. In this paper, for the heavily doped S/D and channel, a bulk region was initially doped with arsenic at a dose of 3×10^{14} cm^{-2}. Afterwards, the suspended Si-NW, which

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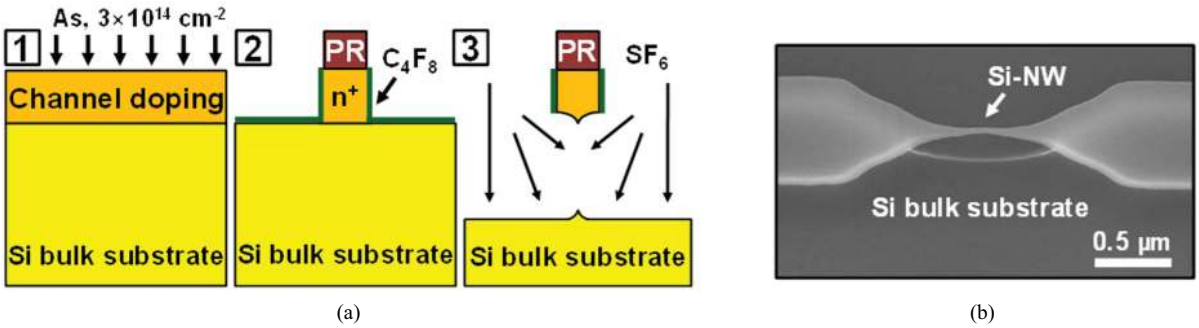
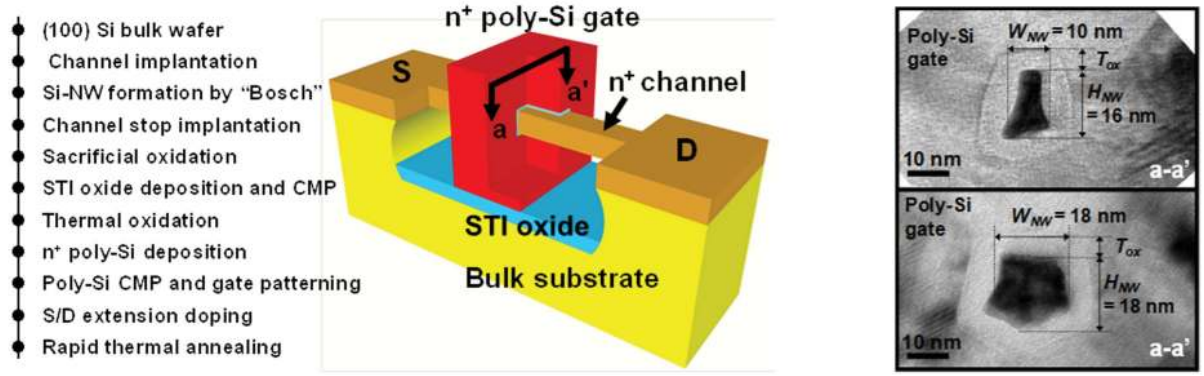


(a) (b)

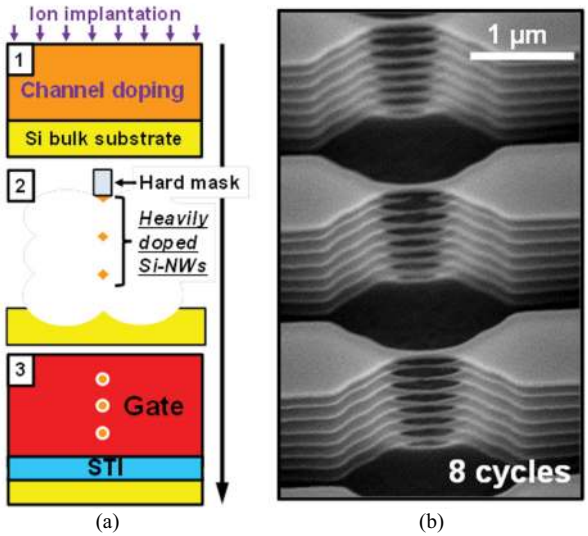
Fig. 1. (a) Schematic representation of the formation of the heavily doped Si-NW on a bulk substrate by the Bosch process. The sidewall of the patterned Si-NW on a bulk substrate is passivated by the *in situ* generated CF_4-based polymer during the RIE process. (b) Tilted SEM image of the fabricated Si-NW on a bulk substrate.



(a) (b)

Fig. 2. (a) Process flow and a schematic of the proposed JL FET built on a bulk substrate. The JL FET has homogeneous doping polarity and a uniform doping concentration along the S/D, but the S/D extension of the control device is additionally doped by arsenic with a dose of 5×10^{15} cm^{-2}. (b) Cross-sectional TEM images along the a-a' direction of the fabricated Si-NW GAA JL FET.

is separated from the bulk substrate, was formed by a deep reactive ion etching (RIE) process, i.e., the Bosch process [11]. It should be noted that the underside of the patterned bulk Si-NW was completely etched out after the one-step etching route without additional processes used in previous reports [9], [10]. Moreover, the cross-sectional geometric shape of the Si-NW can be accurately and independently controlled by anisotropic etching, which accompanies in situ sidewall passivation in the same etching chamber. Isotropic etching was subsequently applied for complete separation of the Si-NW from the bulk substrate while the in situ sidewall passivation layer protected the exposed sidewalls of the Si-NW from being etched laterally. The process flow and a schematic representation of the GAA JL FET are shown in Fig. 2(a). After the formation of the heavily doped Si-NW, the bulk substrate was doped with boron at a dose of 10^{14} cm^{-2} to block leakage paths among adjacent FETs. For proper operation of the JL FET, the diameter of the Si-NW was reduced by sacrificial oxidation. Afterward, the bottom part of the Si-NW was partially filled with an oxide for device isolation. Thermal oxidation with a thickness (T_{ox}) of 5 nm was performed for the gate oxide, and n^+ in situ doped polysilicon was deposited and sequentially patterned for the gate electrode. To evaluate the additional doping effect at the S/D extension, arsenic implantation at a dose of 5×10^{15} cm^{-2} was carried out. Transmission electron microscopy (TEM) images



(a) (b)

Fig. 3. (a) Schematics of the process flow for a vertically and 3-D stacked Si-NW JL FET in the cross-sectional view. (b) SEM image after 8 cycles of the deep RIE process, which enables the formation and separation of each Si-NW. The number of etching cycles is equal to that of the stacked Si-NW.

of the fabricated devices are shown in Fig. 2(b). The cross-sectional area of the Si-NWs with different widths (W_{NW}) and heights (H_{NW}) ranges from 10 nm (W_{NW}) by 16 nm (H_{NW})

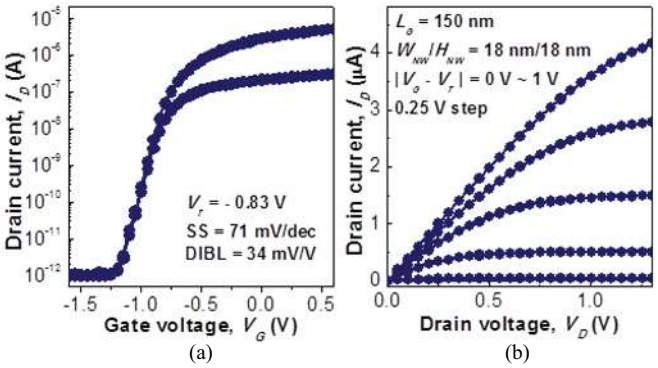


Fig. 4. Measured (a) $I_D - V_G$ and (b) $I_D - V_D$ characteristics of the GAA JL FET with a W_{NW} value of 18 nm, a H_{NW} value of 18 nm, a L_G value of 150 nm, and an n^+ poly-silicon gate.

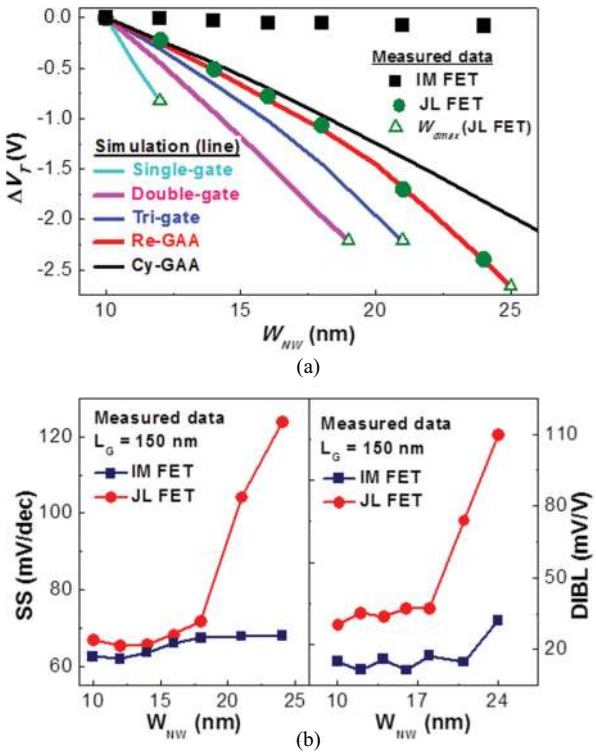


Fig. 5. (a) V_T roll-off characteristic of the JL and IM FETs according to the channel dimensions and the shape of different gate structures. V_T at a W_{NW} value of 10 nm is used as a reference value in each structure. (b) SS and DIBL according to W_{NW} in the fabricated GAA JL and IM FETs.

to 24 nm (W_{NW}) by 20 nm (H_{NW}), and the gate length (L_G) ranges from 30 to 150 nm.

Interestingly, the proposed one-step etching route can be extended to a vertically and 3-D stacked Si-NW GAA JL FET using multiple cycles of the deep RIE process. Conceptual schematics of the fabrication process for a multiple stacked JL FET and a tilted scanning electron microscopy (SEM) image of vertically stacked eight-layer Si-NWs are depicted in Fig. 3(a) and (b), respectively. It should be noted that as a proof-of-concept, vertically stacked Si-NWs on a bulk substrate are realized by an iterative plasma etching route without the epitaxial growth of multiple sacrificial SiGe and structural Si layers [13], [14]. Moreover, in the conventional junction-embedded FET, the formation of the junction and its doping for the S/D become difficult when the number of stacked layers increases. However, in the JL FET, the doping process for the S/D and the channel can be applied before the formation of the vertically stacked Si-NWs; the complexity of the device fabrication process is thereby significantly reduced. The proposed JL FET with vertically stacked Si-NWs thus provides a solution for high-performance transistors and 3-D stacked Flash memory applications.

III. Results and Discussion

Typical transfer and output characteristics for an n-type JL FET are shown in Fig. 4. The threshold voltages (V_T) of the fabricated devices were not optimized due to the use of n^+ poly-silicon as a gate electrode. The off-state current (I_{off}) does not originate from the heavily doped Si-NW but stems from the leakage paths through the bulk region [11]. The on-state current (I_{on}), however, mainly flows through the Si-NW. The normalized I_{on} by the perimeter is 50.8 μA/μm at $V_G - V_T = 1$ V and $V_D = 1$ V. Although the leakage current flows through the bulk region, the ON/OFF current ratio within a V_G range of 1 V is larger than 10^6. High mobility in a conventional junction-embedded FET composed of a GAA and an undoped Si-NW has been reported [15], but the degree of mobility in the fabricated GAA JL FET can be degraded owing to impurity scattering that arises from heavy doping concentration in the Si-NW channel. The estimated electron mobility is 70 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ at a flatband voltage [2]. A JL FET built on a bulk substrate shows feasible device characteristics with a drain-induced barrier lowering (DIBL) value of ~35 mV/V and a subthreshold slope (SS) of ~70 mV/dec due to the GAA and JL structure.

The W_{NW} dependence of V_T, SS, and DIBL in the fabricated GAA JL and inversion-mode (IM) FETs are compared in Fig. 5. The IM FETs were fabricated at the same time by the same processes with the JL FETs except the channel doping concentration (N_{ch}). It was 2×10^{15} cm^{-3} by boron and 1.5×10^{19} cm^{-3} by arsenic, respectively for the IM and JL FETs. Further information can be found in [11]. Fabricated devices with a L_G value of 150 nm were assessed to exclude the SCEs. In this paper, W_{NW} varies more significantly than H_{NW} because W_{NW} is delineated by photo-lithography for various widths and H_{NW} is uniformly determined by the Bosch etching time in a wafer. Therefore, W_{NW} is considered as a dominant factor affecting the device characteristics. As can be clearly seen in Fig. 5, there are two distinctive trends for the V_T roll-off, SS, and DIBL according to the W_{NW}. In the case of IM FETs, the aforementioned device parameters are not significantly affected by W_{NW}. In contrast, they are sensitively changed by W_{NW} because their N_{ch} is very high. In the JL FETs, large fluctuation of the device parameters originating from the various widths would be unavoidable; therefore, structural optimization should be required or narrow width should be sustained as long as a high N_{ch} is used for the JL FETs. For better understanding of ΔV_T in particular, numerical simulations for n-type JL FETs were performed to

analyze the geometrical effects of the channel on ΔV_T [16], and the results are plotted in Fig. 5(a). The parameters used in the simulation are as follows: an aspect ratio ($H_{\mathrm{NW}}/W_{\mathrm{NW}}$) of 1 for a rectangular GAA (Re-GAA) and a tri-gate structure, N_{ch} of 1.5×10^{19} cm^{-3}, a T_{ox} value of 5 nm, and an n$^+$ poly-silicon gate. Note that ΔV_T with respect to ΔW_{NW} is changed according to the geometric structure of the gate. Among the different device structures, a cylindrical GAA (Cy-GAA) JL FET shows the smallest ΔV_T due to its superior electrostatic nature. Projected from these results, the device variability originating from the process variations such as fluctuations of W_{NW} and N_{ch} can be minimized by the GAA structure [12]. The measured V_T roll-off is in good agreement with the simulation results in the rectangular GAA (Re-GAA) structure due to the geometric similarity, i.e., four corners in a trapezoidal shape of the fabricated Si-NW. Below a W_{NW} value of 20 nm, the ΔV_T according to ΔW_{NW} in the fabricated device was approximately 133 mV/nm. In this range, the values of SS and DIBL were not greatly affected by W_{NW}. The transfer characteristic, which depends on the amount of depletion charges in the Si-NW, thus shifts in parallel. This reveals that the aforementioned Si-NW channel can be considered as a FD body. However, above a W_{NW} value of 20 nm, V_T rapidly decreases, and the values of SS and DIBL also increase. Note that the maximum calculated depletion width (W_{dmax}) based on the depletion approximation is approximately 25 nm for a N_{ch} value of 1.5×10^{19} cm^{-3} in the Re-GAA device. Although W_{NW} was smaller than W_{dmax}, the device characteristics were significantly degraded. These results can be explained by the concentration of the majority carriers under the FD condition. The electron and hole concentrations (N_e and N_h) in the FD body of the n-channel JL FET are plotted in Fig. 6. In contrast to a conventional IM FET, the inversion process, i.e., the creation of holes, is enabled when the JL FET is turned off. Because inverted holes preferentially stay near the surface, they do not block the flow of electrons through the center of the body. Thus, the off-state behavior ($V_G \leq V_T$) of the JL FET is quite different from that of a conventional IM FET. When the body of the JL FET is partially depleted due to the heavily doped channel, the device is not properly turned off. Although the body of the JL FET is FD, the device characteristics are significantly degraded according to the pre-existing N_e in the channel. When W_{NW} becomes wider and closer to W_{dmax}, a high N_e in the channel remains even under the FD condition. That is, the body potential is not effectively controlled by V_G and becomes more sensitive to V_D. Therefore, the device characteristics, specifically the values of I_{off}, DIBL, and SS, are degraded. It should be noted that the device degradation arising from the remaining N_e is more severe in the Re-GAA, which has four corners, compared to Cy-GAA [17]. Due to the corner effect, there is no significant suppression of N_e by V_G. Moreover, the corner effect tends to be severe as N_{ch} increases. Consequently, in contrast to a conventional IM transistor, the channel dimensions and the shape of the heavily doped Si-NW in a JL FET should be carefully designed.

Comparisons of the L_G dependences on V_T, SS, and DIBL as extracted from the fabricated GAA JL FETs with and without S/D extension doping are shown in Fig. 7. The reference JL FET has a uniform doping concentration along the source, channel, and drain, but the S/D extension of its control device was additionally doped with arsenic at a dose of 5×10^{15} cm^{-2}. It should be noted that the SCEs are more severe in a device with an additionally doped S/D than in a device with no additional doping. These results are analyzed by numerical simulations with a double-gate structure, an N_{ch} value of 1.5×10^{19} cm^{-3}, additional S/D doping of 10^{20} cm^{-3}, a T_{ox} value of 1 nm, a L_G value of 50 nm, a T_{ch} value of 5 nm, and an n$^+$ poly-silicon gate [16]. The simulation results also indicate that the additional S/D doping degrades the characteristics of the V_T-roll off, SS, and DIBL even when the on-state current is enhanced by the reduction of the series resistance in the S/D, as shown in Fig. 8(a). When the S/D extension is additionally doped and its doping concentration is therefore higher than the channel, the potential of the S/D extension cannot easily be controlled by V_G. That is, the length of the depleted S/D extension is reduced in the off-state. To verify this, a simulated energy band diagram at a V_G value of -0.8 V and a V_D value of 0.05 V is depicted in Fig. 8(b). It can clearly be seen that the effective L_G is shortened by the additional S/D doping. Accordingly, the channel potential is also not effectively controlled by V_G, and the JL device with additional S/D doping suffers more SCEs. In the same manner as done for the IM FET, the introduction of a proper length of the underlap between the gate and the additionally doped S/D extension can suppress degradation of the device characteristics with less decrement of the on-state current. There are two reasons for the aforementioned improvements. The first is that the effective L_G is modulated

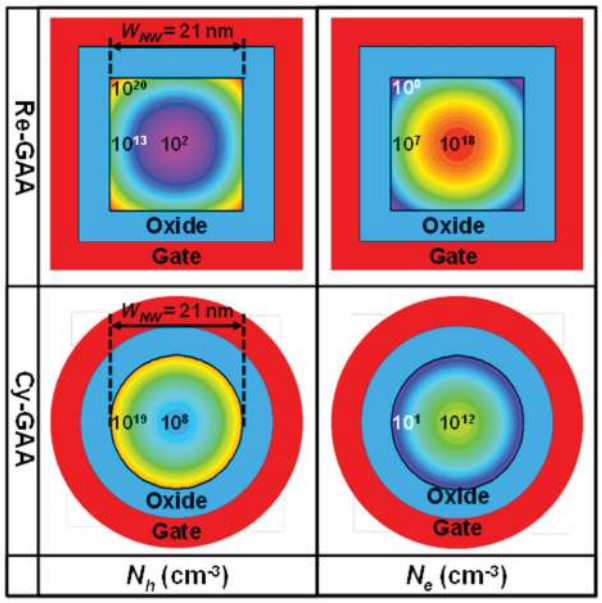


Fig. 6. Simulated N_e and N_h in the body of n-type JL FETs with a W_{NW} value of 21 nm and a V_G value of -2.6 V. Both channels are considered to be FD; however, N_e at the center of the body is still high in the Re-GAA. In contrast to Cy-GAA, a large buildup of electron density at the corner of the channel is observed when the center of the body begins to be depleted. Because most of the incremental charges are taken up by holes, there is no significant decrease of N_e according to V_G.

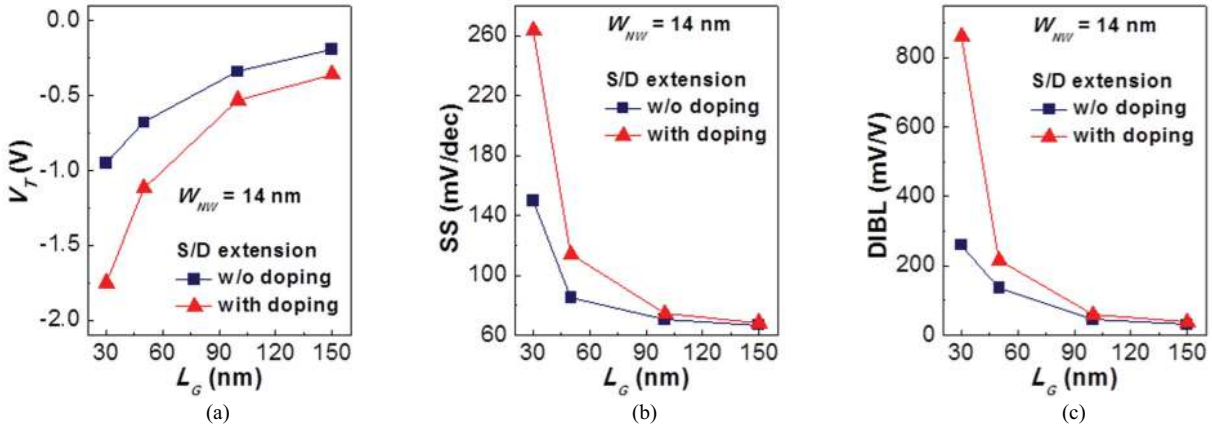


Fig. 7. (a) V_T, (b) SS, and (c) DIBL versus various values of L_G of the fabricated Si-NW GAA JL FETs. The channel controllability by the gate is worsened by the additional S/D doping.

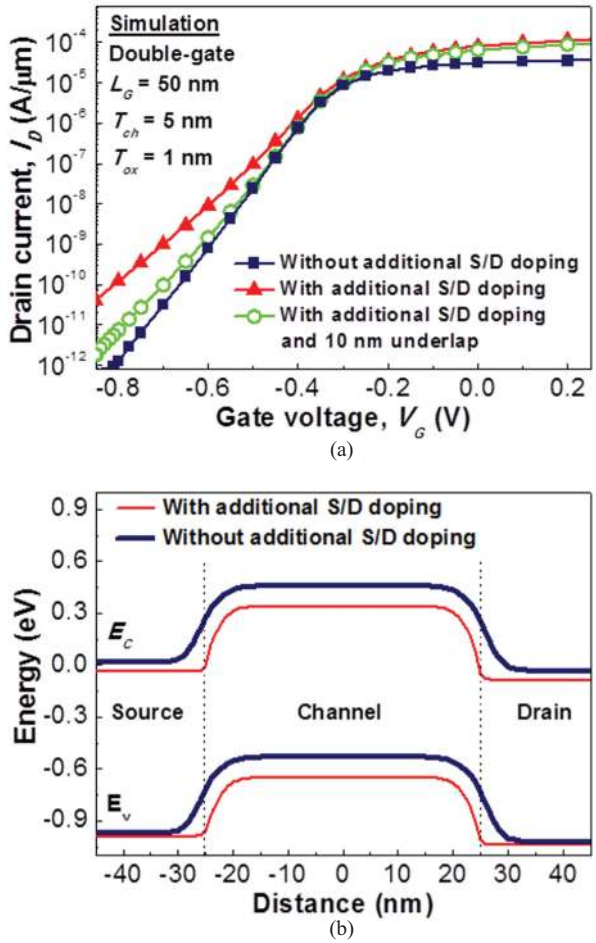


Fig. 8. (a) Simulated transfer curves of double-gate JL FETs with consideration of the additional S/D doping. The characteristics of the JL FET are degraded by the additional S/D doping; however, these are improved by the introduction of a 10-nm underlap. (b) Energy band diagram of two different JL FETs. The JL FET without additional S/D doping shows a longer effective channel length than that with additional S/D doping.

in the range of the underlap by the fringing field from the gate sidewall, i.e., the effective L_G is shortened in the on-state mode and the effective L_G is increased in the off-state mode. The second is that the parasitic resistance of the S/D extension is relatively decreased. It was also reported that high-k spacers could improve the electrostatics of the JL FETs [18]. Therefore, additional S/D doping with high-k spacers can boost the performance of the JL FET in terms of the on/off current ratio, DIBL, and SS.

IV. Conclusion

A JL FET composed of a Si-NW was integrated on a bulk substrate. The Si-NW was fabricated using a one-step plasma etching route, which demands neither a silicon-on-insulator substrate nor epitaxial growth of a sacrificial SiGe and a structural Si layer. Therefore, the JL FET can be fabricated by low-cost and CMOS-compatible processes. In order to suppress the short-channel effects (SCEs), a GAA structure that completely wraps the Si-NW was employed. The proposed devices showed excellent characteristics with the aid of the GAA and junction-free nature. The variability of the threshold voltage due to fluctuation of the channel dimension was reduced by increasing the number of gate electrodes coming into contact with each channel surface in multiple-gate devices. However, it was found that a high concentration of pre-existing majority carriers in the fully-depleted Si-NW channel led to worsened SCEs even in the GAA structure owing to the corner effect. Also, the degree of channel controllability by the gate was significantly affected by additional S/D doping due to the shortened effective gate length, and an optimization strategy pertaining to this was described. Although the JL FET can have better short-channel immunity than the IM FET, the JL FET should be carefully designed than the IM FET. Consequently, structural optimization of the JL FET is further required for the next generation technology node. As a perspective of the proposed device structure, the demonstrated fabrication process can be applicable to vertically and 3-D stacked Si-NW JL devices.

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