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# Investigation of Source/Drain Recess Engineering and Its Impacts on FinFET and GAA Nanosheet FET at 5 nm Node

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**Abstract:** Impacts of source/drain (S/D) recess engineering on the device performance of both the gate-all-around (GAA) nanosheet (NS) field-effect transistor (FET) and FinFET have been comprehensively studied at 5 nm node technology. TCAD simulation results show that the device off-leakage, including subthreshold leakage through the channel ($I_{sub}$) and punch-through leakage ($I_{PT}$) in the sub-channel, is strongly related to the S/D recess process. Firstly, device electrical characteristics such as current density distributions, On/Off-state current ($I_{on}$, $I_{off}$), subthreshold swing (SS), RC delay, and gate capacitance ($C_{gg}$) are investigated quantitatively for DC/AC performance evaluation and comparison according to S/D lateral recess depth ($L_{rcs}$) variations. For both device types, larger $L_{rcs}$ will result in a shorter effective channel length ($L_{eff}$), so that the $I_{on}$ and $I_{off}$ simultaneously increase. At the constant $I_{off}$, the $L_{rcs}$ can be optimized to enhance the device's drivability by ~3% and improve the device's RC delay by ~1.5% due to a larger $C_{gg}$ as a penalty. Secondly, S/D over recess depth ($H_{rcs}$) in the vertical direction severely affects the punch-through leakage in the Sub-Fin or bottom parasitic channel region. The NSFET exhibits less $I_{off}$ sensitivity provided that it can be well controlled under 12 nm since the bottom parasitic channel is still gated. Furthermore, with both $H_{rcs}$ and $L_{rcs}$ accounted for in the device fabrication, the NSFET still shows better control of the off-leakage in the intrinsic and bottom parasitic channel regions and ~37% leakage reduction compared with FinFETs, which would be critical to enable further scaling and the low standby power application. Finally, the S/D recess engineering strategy has been given: a certain lateral recess could be optimized to obtain the best drive current and RC delay, while the vertical over-recess should be in tight management to keep the static power dissipation as low as possible.

**Keywords:** 5 nm node technology; gate-all-around (GAA); nanosheet (NS) FET; FinFET; source/drain recess



**Citation:** Wang, D.; Sun, X.; Liu, T.; Chen, K.; Yang, J.; Wu, C.; Xu, M.; Zhang, W. Investigation of Source/Drain Recess Engineering and Its Impacts on FinFET and GAA Nanosheet FET at 5 nm Node. *Electronics* **2023**, *12*, 770. https://doi.org/10.3390/electronics12030770

Academic Editor: Frédérique Ducroquet

Received: 13 January 2023
Revised: 31 January 2023
Accepted: 1 February 2023
Published: 3 February 2023



## 1. Introduction

FinFETs have become the mainstream logic devices for system-on-chip (SoC) applications since they were adopted by the industry at the 22 nm node [1–3]. However, to meet the chip power-performance-area (PPA) demands at aggressively scaled sub-7 nm nodes while maintaining decent gate controllability, higher and higher Fin aspect ratios (AR) are utilized with limited Fin pitch, bringing up great challenges in both device fabrication and performance aspects [4,5]. In this case, gate-all-around (GAA) nanosheet (NS) FETs have been recognized as a most promising candidate for beyond 7 nm node applications owing to their superior electrostatics and improved layout efficiency [6,7]. Moreover, the NS width design flexibility is also conducive to standard cell optimization in extremely scaled nodes [8,9].

In aggressively scaled transistors, process variations in the fabrication flow are inevitable and have significant impacts on the obtained device characteristics [10–13]. In

particular, the source/drain (S/D) recess process is one of the most crucial factor in the scaled Fin and GAA FETs fabrication. The lateral S/D recess distance into the channel ($L_{rcs}$) directly determines the effective channel length ($L_{eff}$), which is most important for gate electrostatic control and S/D extension region parasitic resistance [14–16]. While the S/D vertical excess recess depth ($H_{rcs}$) is strongly related to the bottom leakage path in both FinFETs and GAA NS FETs, which is one of the biggest challenges in extremely scaled devices [17]. Different kinds of technologies, such as anti-punch-through (APT) implantation, silicon on insulator (SOI), partial/full bottom dielectric isolation (BDI), and the narrow sub-Fin technique, have been proposed to suppress or totally cut off this leakage path [18–21]. Furthermore, several S/D design studies includingS/D confinement, trimming and doping concentration have also been addressed [22–24]. The device architecture of GAA FETs differs from that of FinFETs, so understanding the S/D recess impacts on the different leakage mechanisms along with Fin and NS FETs' performance comparison is essential for figuring out the optimal targets and most important process parameters [25].

In this paper, the effects of the S/D recess process are quantitatively investigated and benchmarked for Fin and NS FETs at the 5 nm node dimensions. In the actual fabrication flow, the device inevitably deviates from the ideal structure, and its impacts can be rapidly and conveniently captured with the help of technology-computer-aided (TCAD). Physical models are calibrated to the experimental data of TSMC's 7 nm node FinFET and then utilized to investigate the impacts of the S/D recess process of interest. The S/D recess process is decoupled into recess volumes in 2 separate directions that are perpendicular to each other. $L_{rcs}$ directly determines the $L_{eff}$ and significantly affects various electrical characteristics in the ultra-scaled transistors. In addition to the intrinsic channel investigation, the sub-Fin or bottom parasitic channel region, where the gate control is weak and punch-through can easily occur is another key factor affecting the device switch characteristics. $H_{rcs}$, which is closely related to off-state energy band changes in this region, is also studied. The simulation results show that the sensitivity of off-state current ($I_{off}$) in NS FETs to this process variations is superior. Devices of Fin and NS FETs with both $L_{rcs}$ and $H_{rcs}$ are constructed in TCAD. The off-state analysis is conducted through the $I_{off}$ breakdown into 2 main leakage components, which are subthreshold leakage through the channel ($I_{sub}$) and punch-through leakage ($I_{PT}$) in the sub-channel. Finally, we gave a conclusion regarding the S/D recess engineering in Fin and GAA NS FETs.

## 2. Device Structure and Simulation Methodology

3D schematics of the ideal 2-fin FinFET and 3-stacked NS FET structures are shown in Figure 1, with the lateral S/D recess distance $L_{rcs}$ and the vertical S/D recess depth $H_{rcs}$ labeled, respectively. Key device parameters of the studied Fin and NS FETs are summarized in Table 1 based on 5 nm node ground rules [26]. The gate length ($L_g$) of 18 nm, the spacer thickness ($L_{sp0}$) of 5 nm, and the contact gate pitch (CPP) of 51 nm are adopted. To ensure the same layout density, the active footprint of Fin and NS FETs is kept the same, namely the baseline GAA FET with 36 nm wide NS. The channel doping concentration is $10^{15}/cm^3$ to avoid undesired carrier mobility degradation and the random doping fluctuation (RDF) [27]. In-situ and uniform doping S/D epitaxy was performed with $2 \times 10^{20}/cm^3$ of phosphorus doping concentration for n-type MOS. The doping concentration of punch-through stopper (PTS) layer below the channel is $2 \times 10^{18}/cm^3$ to suppress the sub-Fin leakage [28]. As for the electrical characteristic simulations, the operating voltage (Vdd) is equal to 0.7 V, and the parasitic contact resistivity is fixed to $10^{-9}$ ohm·cm$^2$ [29].

3D process simulations of Fin and NS FETs have been conducted using Sentaurus TCAD tools with advanced physical models [30]. A self-consistent calculation was achieved based on the drift-diffusion (DD) transport equation combined with the Poisson and carrier continuity equations. The bandgap narrowing effect dependent on the doping concentration was implemented by the Slotboom model in all the semiconductor regions [31]. Thinlayer and inversion and accumulation layer (IAL) mobility models were utilized, ac-

counting for the impurity, phonon, surface roughness, and thin-layer-related scattering. Density-gradient (DG) based quantum correction models were included. Moreover, an auto-orientation framework was applied to take the surface orientation dependency of the carrier mobility and quantum correction into account. Ballistic mobility and high-field saturation models, Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling (BTBT) models were also included. The vital quantization effects, including quantum confinement and quantum tunneling, have been well implemented and considered in the TCAD simulation. By applying DG-based potential-like correction to the carrier density calculation formula, the carrier concentration deviates from the classical DD model and captures much quantum-mechanical behavior inside 3D device [32,33]. The BTBT tunneling current cannot be neglected if the electric field exceeds $7 \times 10^5$ V/cm [34]. The Hurkx model is established based on the local variables and is conducive to numerical calculations. And these physical models have been utilized and validated in [13,23,35].

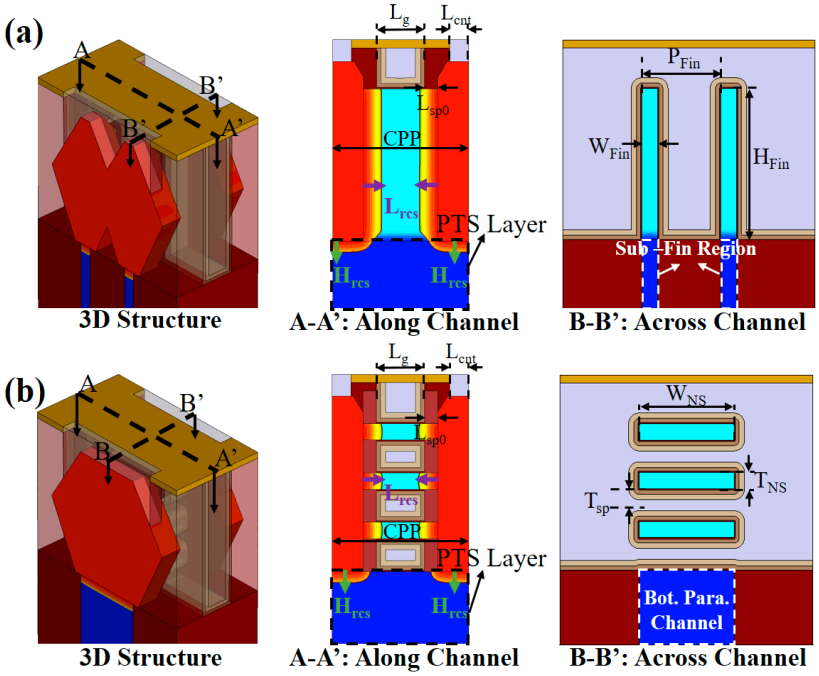


**Figure 1.** 3D schematic view of the ideal device structure and 2D cross-sections across and along the channel of (**a**) FinFET and (**b**) NSFET with the same footprint.

**Table 1.** Key Device Parameters for 5 nm Node Fin and NS FETs.

| | Parameters | Value |
|---|---|---|
| Both | Contact gate pitch (CPP) | 51 nm |
| | Gate length ($L_g$) | 18 nm |
| | Spacer length ($L_{sp0}$) | 5 nm |
| | Contact length ($L_{cnt}$) | 14 nm |
| | S/D doping ($N_{sd}$) | $2 \times 10^{20}$ cm$^{-3}$ |
| | Channel Doping ($N_{ch}$) | $1 \times 10^{15}$ cm$^{-3}$ |
| | Punch-Through Stop Doping ($N_{PTS}$) | $2 \times 10^{18}$ cm$^{-3}$ |
| Fin | Number of Fin | 2 |
| | Fin width ($W_{Fin}$) | 6 nm |
| | Fin height ($H_{Fin}$) | 56 nm |
| | Fin pitch ($P_{Fin}$) | 30 nm |
| GAA | Number of Nanosheet | 3 |
| | NS width ($W_{NS}$) | 36 nm |
| | NS Thickness ($T_{NS}$) | 6 nm |
| | NS Spacing ($T_{sp}$) | 12 nm |

The physical model parameters have been delicately calibrated with the TSMC 7 nm node FinFET silicon data, as shown in Figure 2 [36]. The calibration process is performed as follows. The default physical model parameters are included in the material parameter file supplied by Synopsys, while some key process and physical model parameters are manually tuned within a reasonable range. Firstly, in the subthreshold regime, the doping profile is changed so that the TCAD simulation results can be well fitted to the experimental silicon data. As shown in Figure 2, the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are consistent with [36], which are ~64 mV/dec and ~30 mV/V, respectively. Furthermore, the ballistic coefficient and surface roughness scattering factor are tweaked to fit the Ids in the linear regime. The peak internal carrier saturation velocity of such scaling devices exceeds the conventional saturation velocity. In spite of this, the saturation velocity is increased from ~$1.0 \times 10^7$ cm/s to ~$3.0 \times 10^7$ cm/s in order to match the device on-state current. The final adjustment of saturation velocity is basically consistent with that reported in [35].

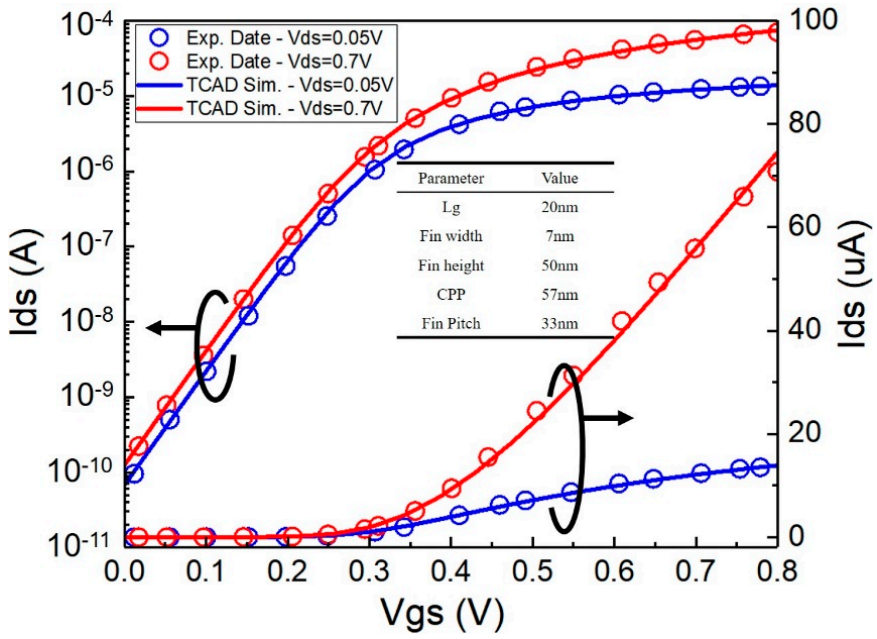


**Figure 2.** Physical model parameters calibrated to the mature 7 nm node Si-FinFET experimental data. Inset: Key geometry parameters of the fit device, of which the related parameters in the TCAD simulation is the same as [36].

The transistor dimensions of the 5 nm technology node are not essentially different from those of the 7 nm node. Besides, the main transport surface orientation is changed from (110) of FinFET to (100) of NSFET. It has been well accounted for in the TCAD simulation through the auto-orientation framework based on the nearest interface. Therefore, the calibrated physical models can well apply to the 5 nm-node device electrical characterization in this work. As a matter of fact, with the continuous technology upgrading following Moore's Law, the conventional pitch scaling has greatly slowed down and basically reached its limitation. This can be attributed to many reasons, such as lithography limitations, manufacturing costs, process variations, and stability. Instead, the chip performance boost becomes more reliable with the Design Technology Co-Optimization (DTCO) methodology to achieve equivalent scaling. Various techniques, including complementary FET (CFET), contact over active region (COAG), single diffusion break (SDB), buried power rail (BPR), and back-side power distribution network (BS-PDN), have been proposed [3,37,38]. They are mainly concerned with the improvement of power, performance, area and cost (PPAC) of the whole SoC design. Therefore, the physical models only need to be slightly tweaked

for further scaling of the device on the condition that the related process parameters and device geometry are given correctly.

## 3. Results and Discussion

### *3.1. $L_{rcs}$ Impacts on Device Performance*

Figure 3 shows the transfer characteristics of both Fin and NS FETs with varied $L_{rcs}$. Low power (LP, $I_{off}$ = 0.1 nA) design is assumed for the work function (WF) modulation of Fin and NS FETs with ideal structures [23].

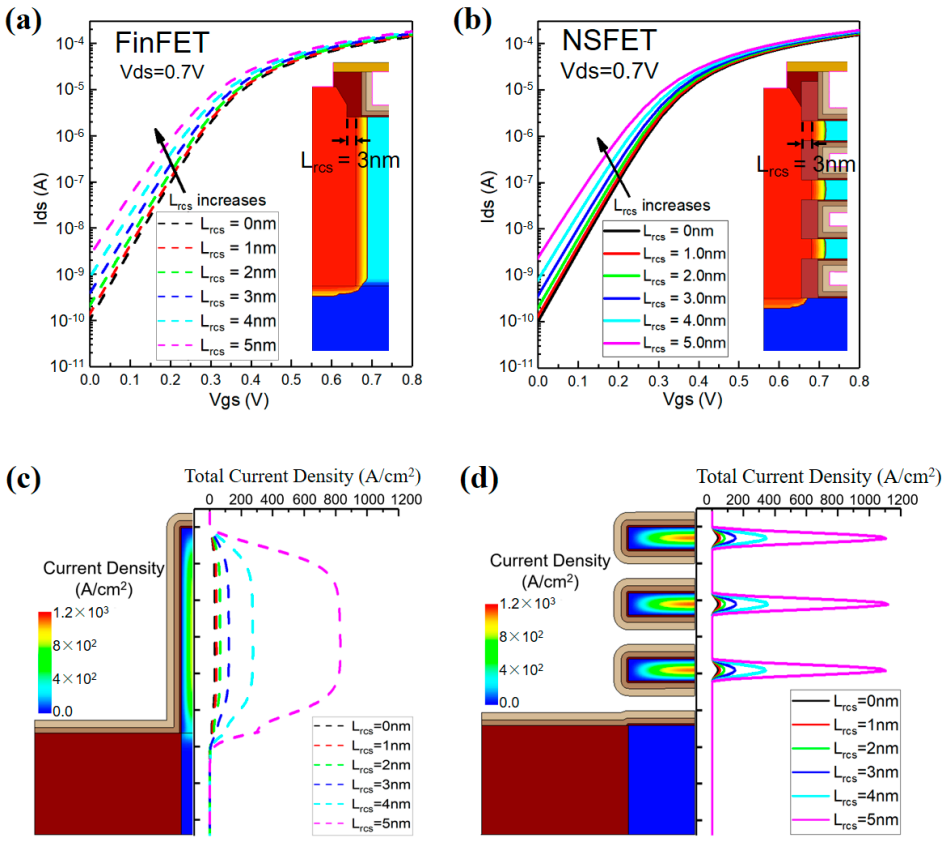


**Figure 3.** Id-Vg curves @ Vds = 0.7 V of (**a**) FinFET and (**b**) NSFET. Inset: Fin and NS FET devices with 3 nm $L_{rcs}$. Leakage current density profiles (Vgs = 0 V and Vds = 0.7 V) of (**c**) FinFET and (**d**) NSFET at 5 nm $L_{rcs}$.

The upper limit of $L_{rcs}$ is 5 nm, which is not larger than the spacer length in order to avoid channel damage. As the $L_{rcs}$ increases, its impacts on both device types are almost the same, as shown in Figure 3a,b. While the on-state current ($I_{on}$) is elevated by additional $L_{rcs}$, the subthreshold characteristics such as the $I_{off}$ and SS deteriorate owing to the short channel effect (SCE). The $I_{off}$ of devices with $L_{rcs}$ = 5.0 nm is more than 10 times larger than that of the ideal Fin and NS FETs. The device leakage current density profiles at 5 nm $L_{rcs}$ are shown in Figure 3c,d, respectively. The higher current density peak value of the NSFET is compensated by its smaller cross-section and bottom parasitic channel leakage, so that the overall $I_{off}$ is still slightly smaller, as shown in Figure 4a. Furthermore, most of the off-state current resides in the intrinsic channel region, which indicates that the $I_{sub}$ dominates.

The key device characteristics, including the $I_{on}$, $I_{off}$, SS, and on-off ratio, extracted from the Id-Vg curves are shown in Figure 4. $I_{on}$ increases linearly as the epitaxial S/D region is brought closer to the channel with the exponential increase in the $I_{off,}$ whose increment is much more significant than $I_{on}$ with increasing $L_{rcs}$. Compared with the FinFET, about 10% $I_{on}$ improvement of the NSFET is obtained at the same footprint. It can

be attributed to the fact that the effective width ($W_{eff}$) of an NSFET with a 36 nm NS is 252 nm larger than that of a FinFET, which is 236 nm. The $W_{eff}$ of different device structures is calculated as shown in the following equations:

$$W_{eff.Fin} = (2 \times H_{Fin} + W_{Fin}) \times Fin\ Number \quad (1)$$

$$W_{eff.NS} = 2 \times (W_{NS} + T_{NS}) \times NS\ Number \quad (2)$$

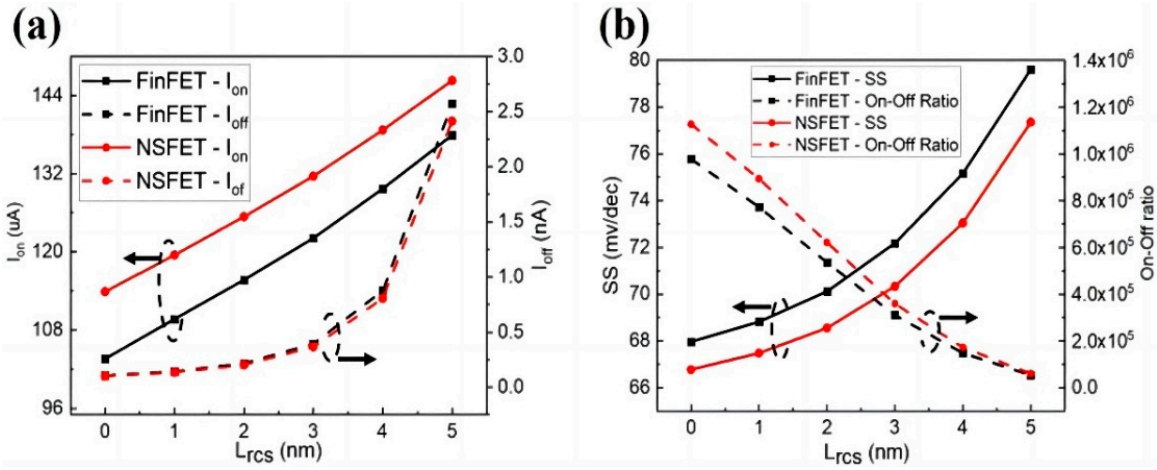


**Figure 4.** Trends of DC characteristics by $L_{rcs}$ variations (**a**) $I_{on}$ and $I_{off}$, (**b**) SS and On-Off ratio.

On the other hand, the electron transportation of NSFET is mainly implemented in the (100) orientation, in which the electron mobility is higher than that of the (110) surface orientation of FinFET [39]. The $I_{off}$ trends with varied $L_{rcs}$ are almost the same for Fin and NS FETs, but the superior electrostatics of the NSFET is beneficial in suppressing the $I_{sub}$. This result is consistent with the trends of SS shown in Figure 4b, which is a critical indicator of gate controllability. SS and on-off ratio simultaneously degrade with shorter effective gate lengths resulting from the larger $L_{rcs}$. In the meanwhile, better current drivability and effective suppression of the leakage current both contribute to the better on-off ratio of the NSFET.

Apart from DC behaviors, the AC performance also needs to be rigorously evaluated with the capacitance components taken into consideration. Firstly, LP design by WF tuning is considered so that the static power dissipation ($P_{static}$) is kept unchanged for different device structures. As shown in Figure 5a, the $I_{on}$ at constant the $I_{off}$ shows differences from the absolute values shown in Figure 4a, of which the larger $L_{rcs}$ also leads to more severe $I_{off}$. $L_{rcs}$ can be optimized to reduce the S/D extension region parasitic resistance with a reasonable gate controllability maintained so that the $I_{on}$ is slightly boosted by ~3%. However, this DC gain brought by $L_{rcs}$ will vanish if it is longer than 3 nm. The reason is that in this range, the deteriorative subthreshold characteristics will require a higher threshold voltage ($V_{th}$) to meet the needs of the LP design, and the on-state current will be negatively affected due to the overdrive voltage decrease ($V_{od}$). The trade-off between SCE immunity and device drivability should be carefully considered for device design and optimization.

Figure 5b shows the intrinsic and main parasitic capacitance components in the NSFET, of which the $C_{ov,ISP}$ between S/D and metal gate region is a specific element compared with the FinFET [8,10]. As the S/D is closer to each other through S/D lateral recess, the total gate capacitance ($C_{gg}$), including the parasitic components such as inner fringing ($C_{if}$), outer fringing ($C_{of}$) and overlap ($C_{ov}$) capacitances, increases, as shown in Figure 5c. The intrinsic device RC delay is taken to evaluate the device AC performance and is defined as follows:

$$RC\ Delay = \frac{V_{dd} \times C_{gg}}{I_{on}} \quad (3)$$

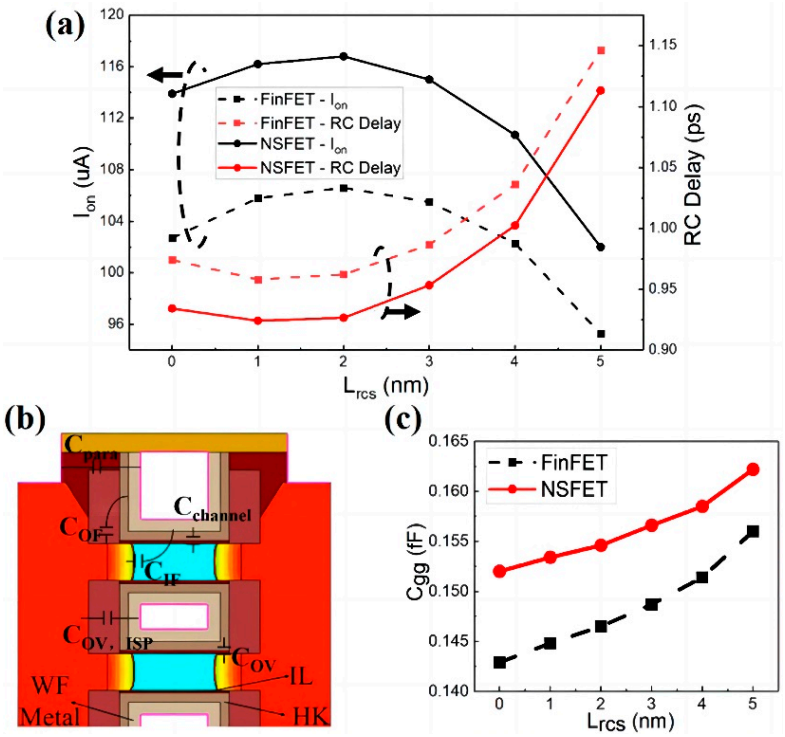


**Figure 5.** (**a**) $I_{on}$ and RC Delay comparison at fixed $I_{off}$ with varied $L_{rcs}$ (**b**) Schematic of intrinsic and parasitic gate capacitance components distribution in NSFET (**c**) $C_{gg}$ trends by varying $L_{rcs}$ for Fin and NS FETs.

As shown in Figure 5a, the NS FET RC delay improvement over the FinFET is reduced to ~4.5% due to the larger parasitic capacitances. For both device types, the AC performance gain is adversely affected by increased Cgg, and the best RC delay improvement is reduced to ~1.5% with the optimal $L_{rcs}$ shifted to the smaller value. The potential optimization of DC/AC performance at the constant $I_{off}$ can be achieved through the careful control of S/D lateral recess, but this improvement is limited due to the extremely scaled device dimensions of the 5 nm node. When $L_{rcs}$ exceeds 3 nm, the gate control is more vulnerable, and the device performance will degrade rapidly.

### *3.2. $H_{rcs}$ Impacts on Device Performance*

Furthermore, the impacts of the vertical S/D over recess variation have also been studied. The S/D region is heavily doped to minimize the parasitic resistance so that the depletion region mainly extends into the substrate. The extremely short $L_g$ length of 18 nm leads to the significant proximity of the drain-substrate and the source-substrate depletion regions. Combining the factor that the drain is biased at $V_{dd}$ in the off state, which will further widen the drain-substrate depletion region, the punch-through leakage path can be easily formed where the gate control is weak. Its increase will degrade the static power dissipation and the switching characteristics and should be suppressed as low as possible. Therefore, its impacts on the leakage current of Fin and NS FETs need to be quantitatively examined. Figure 6a,b shows the transfer characteristic curves for various $H_{rcs}$. The $I_{off}$ enormously increases when $H_{rcs}$ exceeds 10 nm for both Fin and NS FETs.

If the vertical S/D recess is within good control, such as $H_{rcs}$ = 0 nm, the subthreshold leakage through the channel dominates, as shown in Figure 3c,d. Due to higher PTS doping and a larger punch-through distance, the leakage through the sub-Fin or bottom parasitic channel is negligible. However, as shown in Figure 6c,d, when the $H_{rcs}$ deviates from the ideal value ($H_{rcs}$ = 0 nm), in addition to the subthreshold leakage by the channel, the $I_{PT}$ in the region far from the gate control will come into effect and increase rapidly while the leakage current in the channel region is barely affected. As $H_{rcs}$ increases, more S/D

dopants will undesirably diffuse in the sub-Fin or bottom parasitic channel region, leading to easier punch-through formation. The leakage path gets wider, and the peak current density is also increasing as its position shifts away from the surface.

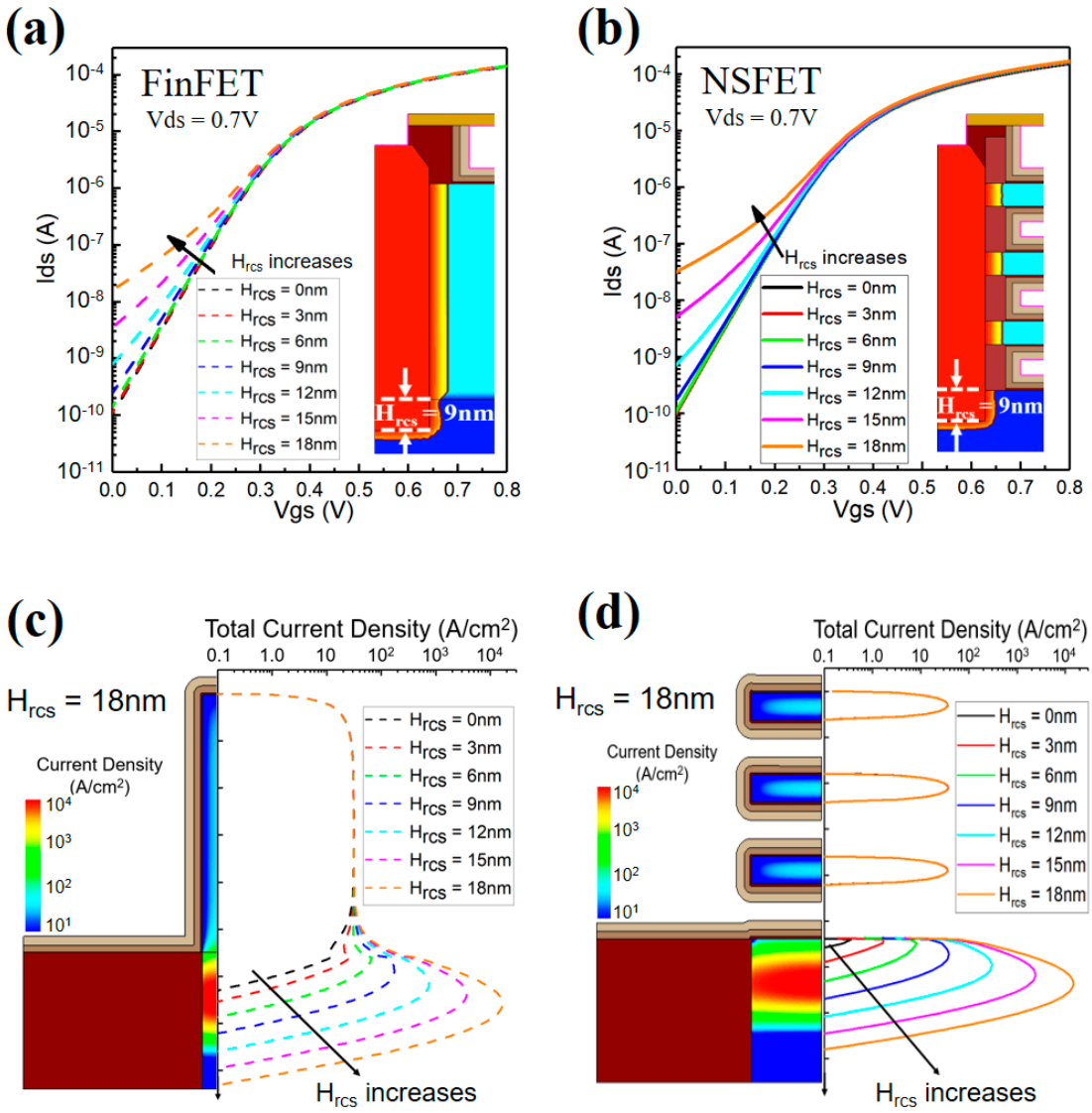


**Figure 6.** (**a**) Id-Vg curves @ Vds = 0.7V with various $H_{rcs}$ from 0 nm to 18 nm for (**a**) Fin and (**b**) NS FETs. Leakage current density contour plots at $H_{rcs}$ = 18 nm and its variation along Fin height direction of (**c**) Fin and (**d**) NS FETs.

The $I_{off}$ of various devices is extracted and presented in Figure 7. The $I_{off}$ of the NSFET is slightly smaller than that of the FinFET when $H_{rcs}$ is relatively small. However, it will soon outperform the FinFET due to the wider bottom parasitic channel. As shown in Figure 7, the additional bottom gate still has more controllability than the FinFET over the region where punch-through leakage is formed. Therefore, when the $H_{rcs}$ is relatively small, the increase in its punch-through current is not as sensitive as the FinFET. However, the $I_{off}$ of the NSFET will eventually exceed that of the FinFET as $H_{rcs}$ increases because of the wider leakage path.

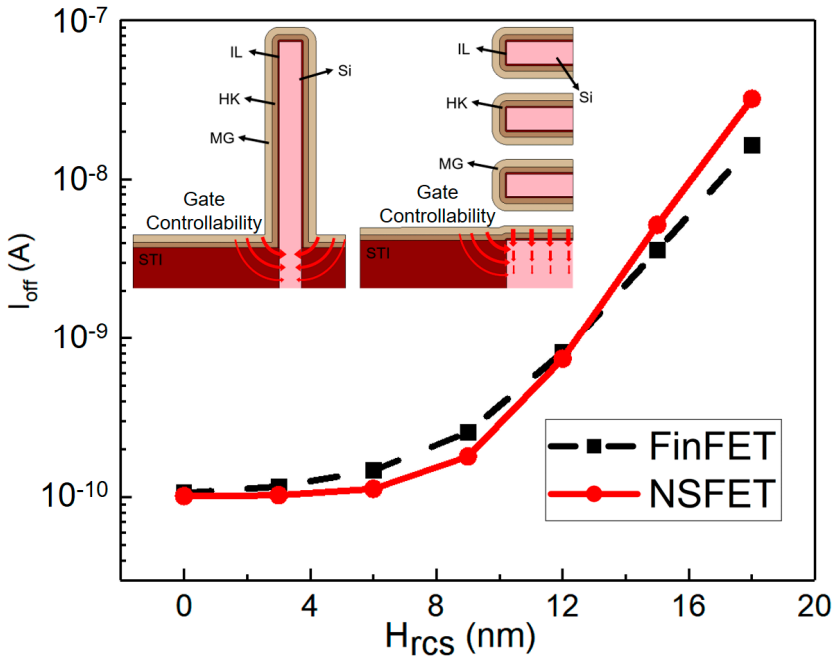


**Figure 7.** $I_{off}$ of Fin and NS FETs as a function of $H_{rcs}$. Inset: Gate controllability demonstration of sub-Fin region and bottom parasitic channel.

As shown in this Figure 8a, the electron barrier in the parasitic channel of NSFET is higher than that of FinFET due to the additional electrostatic control from the bottom gate electrode. The position of 0 nm corresponds to the center of the channel. Therefore, the source-to-drain leakage current of NSFET is 23% less than that of FinFET for 6 nm $H_{rcs}$. However, with the continuous increase in the $H_{rcs}$, the leakage path shifts away from the top of the STI, as shown in Figure 6c,d. In the meantime, more phosphorus inevitably diffuses into the Sub-Fin and the bottom parasitic channel region. This will make the effective substrate doping concentration ($N_{A,eff}$) drop due to the doping compensation effect. The threshold voltage for these regions will decrease along with $N_{A,eff}$ reduction and bring about upsurge of the leakage current. The electron barriers of both devices decrease, as shown in Figure 8b, which indicates that these regions are easier to be affected by the S/D and the larger $I_{off}$. Even though the electron barriers of Fin and NS FETs are almost the same at 18 nm $H_{rcs}$, the wider NS will take dominance over the additional bottom gate control effect and result in a larger device $I_{off}$ for the NSFET, as shown in Figure 7. This will reduce the device's On-Off ratio more than 2 order and deteriorate the device switch characteristics.

### *3.3. S/D Recess Overall Impacts*

The $I_{off}$ of Fin and NS FETs breaks down into 2 main components: the $I_{sub}$ in the channel region and the $I_{PT}$ in the sub-Fin or bottom parasitic channel region, as shown in Figure 9. 2 nm $L_{rcs}$ and 10 nm $H_{rcs}$ are assumed for S/D over recess in both directions. The 10 nm $H_{rcs}$ is consistent with the values provided in ref. [20], which considers the process nonuniformity and variations. As mentioned above, the ideal Fin and NS FETs are designed to satisfy the LP requirement. In this case, the $I_{sub}$ takes up the most part, of which the portion is larger than 97%, while $I_{PT}$ is almost negligible. However, with lateral and vertical over recess happening in the device fabrication flow, both the $I_{sub}$ and $I_{PT}$ increase. Especially, the $I_{PT}$ becomes comparable to or even larger than the $I_{sub}$ for the devices with 2 nm $L_{rcs}$ and 10 nm $H_{rcs}$. In this case, the $I_{sub}$ and $I_{PT}$ of the NSFET are less than those of the FinFET but are still under good control due to its superior gate electrostatics and additional gate control over the bottom parasitic channel region. With the above mentioned two main leakage components taken into consideration, the device overall leakage $I_{off}$

of NSFET is 37% less than that of FinFET. GAA's superior leakage control capability is essential for its deployment in the mobile SoC of smartphones, in which scenario the low standby power design must be well addressed.

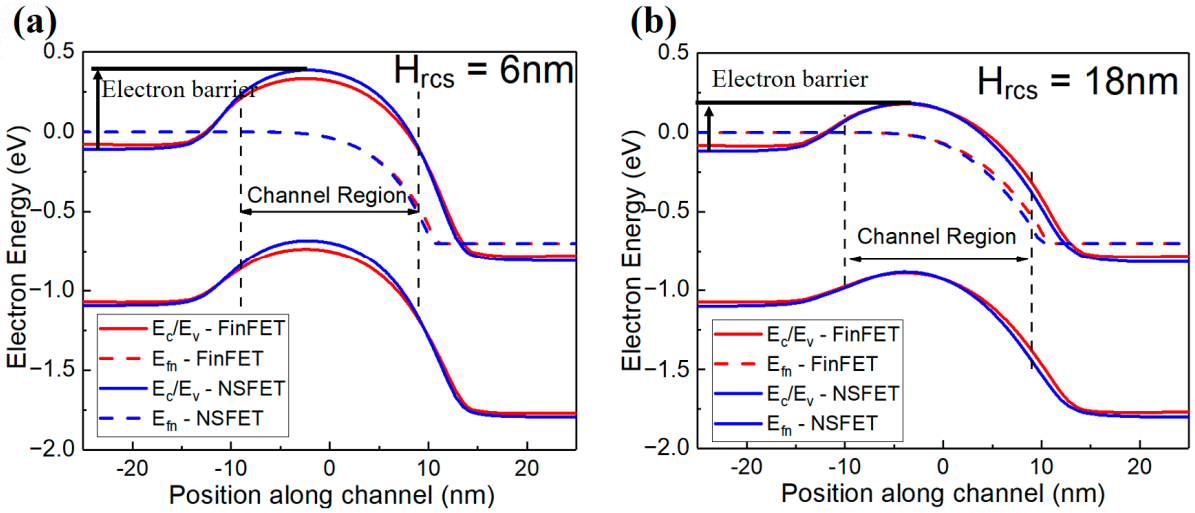


**Figure 8.** Off-state electron energy band distribution along the channel direction at (**a**) 3 nm (1/2 × 6 nm) and (**b**) 9 nm (1/2 × 18 nm) below the shallow trench isolation (STI) respectively.

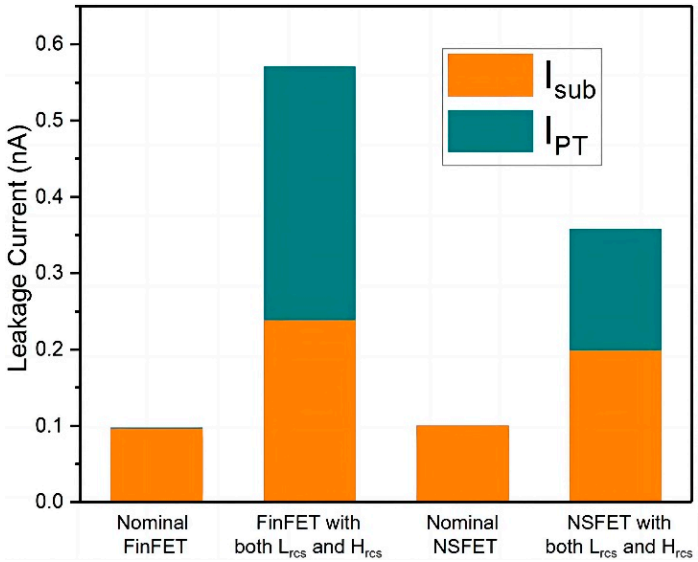


**Figure 9.** Shows that the $I_{on}$ and its main components of Fin and NS FETs with various structures.

## 4. Conclusions

In this article, the DC and AC performances of FinFETs and GAA NSFETs with various S/D recess shapes are comprehensively investigated and compared using fully calibrated 3D TCAD simulations based on the 5 nm node dimensions. Device off-leakage is strongly related to the S/D lateral and vertical recesses. In terms of $L_{rcs}$, its increase will lead to a shorter $L_{eff}$. This parameter, as a critical device parameter, can be optimized through $L_{rcs}$ to achieve the best trade-off between SCE immunity and device drive capability for both Fin and GAA FETs. The simulation results show that the $I_{on}$ can be enhanced by about ~3% while the RC delay, an important AC performance indicator, can be improved by ~1.5%. As for the 5 nm node dimensions, the electrostatic integrity is at risk, and the 18 nm Lg is approaching the scaling limitation. Therefore, it is more difficult to further reduce the $L_{eff}$ while keeping the SCE within an acceptable range. As a result, the DC and AC performance improvement is relatively small even at the optimal $L_{rcs}$. Regarding the vertical S/D recess,

the $I_{off}$ of the NSFET is not as sensitive as that of the FinFET due to the additional bottom gate control when $H_{rcs}$ can be well controlled under 12 nm. Beyond this range, the nature of the wider bottom parasitic channel of GAA NS FETs will come into dominance and exceed the leakage of FinFETs. With the presence of both $L_{rcs}$ and $H_{rcs}$, the off-state current, including the $I_{sub}$ and $I_{PT,}$ of the NSFET is still under good control and exhibits 37% less $I_{off}$ than the FinFET. And the NSFET shows more robustness to the process variations, which is a critical factor in the next scaling node. Therefore, GAA NSFETs would provide better device performance and yield at the 5 nm technology node and beyond.

**Author Contributions:** Conceptualization, D.W.; methodology, D.W., T.L., K.C. and C.W.; investigation, D.W., X.S. and J.Y.; writing—original draft preparation, D.W.; writing—review and editing, T.L., C.W. and M.X.; supervision, W.Z. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research received no external funding.

**Data Availability Statement:** The data and code are available from the corresponding authors upon reasonable request.

**Acknowledgments:** This work is sponsored by the platform for the development of next-generation integration circuit technology.

**Conflicts of Interest:** The authors declare no conflict of interest.

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