



Investigation of Transformer Winding Architectures for High Voltage (2.5 kV) Capacitor Charging and Discharging Applications

Thummala, Prasanth; Schneider, Henrik; Zhang, Zhe; Andersen, Michael A. E.

Published in:

IEEE Transactions on Power Electronics

Link to article, DOI:

[10.1109/TPEL.2015.2491638](https://doi.org/10.1109/TPEL.2015.2491638)

Publication date:

2016

Document Version

Peer reviewed version

[Link back to DTU Orbit](#)

Citation (APA):

Thummala, P., Schneider, H., Zhang, Z., & Andersen, M. A. E. (2016). Investigation of Transformer Winding Architectures for High Voltage (2.5 kV) Capacitor Charging and Discharging Applications. *IEEE Transactions on Power Electronics*, 31(8), 5786 - 5796. <https://doi.org/10.1109/TPEL.2015.2491638>

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

Investigation of Transformer Winding Architectures for High Voltage (2.5 kV) Capacitor Charging and Discharging Applications

Prasanth Thummala[§], *Member, IEEE*, Henrik Schneider^{*}, *Member, IEEE*, Zhe Zhang^{*}, *Member, IEEE*, and Michael A. E. Andersen^{*}, *Member, IEEE*

Abstract—Transformer parasitics such as leakage inductance and self-capacitance are rarely calculated in advance during the design phase, because of the complexity and huge analytical error margins caused by practical winding implementation issues. Thus, choosing one transformer architecture over another for a given design is usually based on experience, or a trial and error approach. This paper presents analytical expressions for calculating leakage inductance, self-capacitance and ac resistance in transformer winding architectures (TWAs), ranging from the common non-interleaved primary/secondary winding architecture, to an interleaved, sectionalized, and bank wound architecture. The calculated results are evaluated experimentally, and through finite element (FEM) simulations, for a RM8 transformer with a turns ratio of 10. The four TWAs such as, non-interleaved and non-sectioned, non-interleaved and sectioned, interleaved and non-sectioned, and interleaved and sectioned, for an EF25 transformer with a turns ratio of 20, are investigated and practically implemented. The best TWA for a RM8 transformer in a high-voltage (HV) bidirectional flyback converter, used to drive an electro active polymer based incremental actuator, is identified based on the losses caused by the transformer parasitics. For an EF25 transformer, the best TWA is chosen according to whether electromagnetic interference (EMI) due to the transformer interwinding capacitance, is a major problem or not.

Index Terms— switch-mode power converters, high voltage dc-dc converters, energy efficiency, actuator, transformer parasitics, transformer winding architectures, high voltage transformer

I. INTRODUCTION

DIELECTRIC electro active polymer (DEAP) is an emerging smart material that has experienced significant development and has gained increasing attention over the last decade [1]-[5]. DEAP, when used as actuators, has the potential to be an effective replacement for many conventional actuators due to its unique properties such as, large elastic strain (5-100%), light weight (7 times lighter than steel and copper), high

Manuscript received 24th July 2015; revised 7th September 2015; and accepted 10th October 2015. A part of this paper was presented and selected as an outstanding presentation at the 29th Annual Applied Power Electronics Conference, Fort Worth, TX, USA, March 2014.

[§]The author is with Electrical Machines and Drives Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Engineering Drive 1, Singapore 117580 (e-mail: prasanth.iitkgp@gmail.com).

^{*}The authors are with Electronics Group, Department of Electrical Engineering, Technical University of Denmark, Kongens Lyngby, 2800 Denmark. (e-mail: hensc@elektro.dtu.dk; zz@elektro.dtu.dk; ma@elektro.dtu.dk).

flexibility (100,000 times less stiff than steel), low noise operation, and low power consumption. However, a compact high voltage driver is required to charge and discharge the DEAP from 0 V to 2500 V DC supplied from a 24 V battery. The DEAP actuator applications [6]-[9] require bidirectional high voltage (HV) converters, to charge and discharge the actuators, and to increase the life time of the source, by transferring part of the energy to it. The flyback converter topology is suitable for low power (< 150 W), and high voltage capacitor charging applications, as it can be made very compact with a low number of components [10].

The flyback transformer is the most critical component in the HV driver performance. In Fig. 1, the schematic of the HV flyback converter including the equivalent model of the HV transformer is provided. The high output voltage requirement demands a high turns ratio for the transformer, which calls for a large number of secondary turns. This may lead to a high self-capacitance C_s (in Fig. 1) of the secondary HV winding, resulting in the severe capacitive switching loss, and undesirable, resonating current spikes in the leading edge of the current waveform, which could lead to false triggering of the current limit during the turn-on process [11]. The problem of high self-capacitance in the HV flyback, led early designers in this research area to automatically choose zero current switching (ZCS) primary operation, which gives zero voltage switching (ZVS) in the secondary. Leakage inductance plays a critical role in the HV switched-mode power supply design. The stored energy due to the leakage inductance L_{lkp} or L_{lks} (in Fig. 1) of the HV transformer may cause undesirable voltage spikes in the primary and secondary MOSFETs during the charge and discharge processes, respectively, which lead to the use of

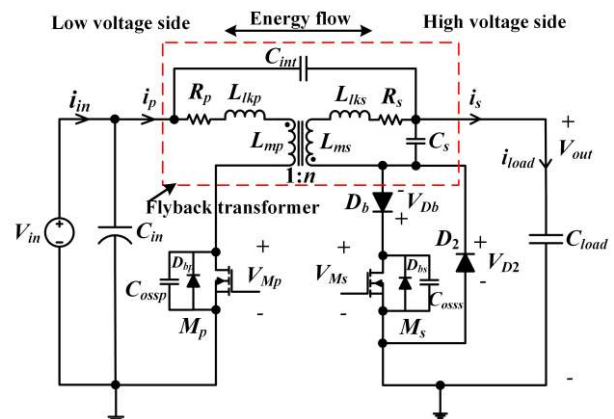


Fig. 1. Schematic of the HV bidirectional flyback converter [7].

active or passive snubber circuits in the converter. Consequently, the leakage inductance creates EMI problems, increases switching losses and reduces energy efficiency. With active snubbers high energy efficiency can be achieved, at the expense of higher cost and added control complexity, whereas the passive snubbers result in switching loss due to the leakage inductance. The ac resistance is also an important parameter to consider, since the ac conduction loss is caused by the high frequency skin and proximity effects, in a flyback converter operating in boundary conduction mode (BCM) or in discontinuous conduction mode (DCM). In order to limit the maximum temperature rise across the transformer, it is necessary to minimize the conduction loss due to the transformer winding resistances. The losses due to the transformer parasitics in the HV flyback converter are explained in [7]. The interwinding capacitance between primary and secondary windings C_{int} (in Fig. 1) of the flyback transformer gives an indication of how much common mode noise can be allowed. The interwinding capacitance couples the primary and secondary voltages, greatly reducing the high-frequency ac isolation, and leading to common-mode currents and conducted EMI. In medical applications common-mode noise is especially critical and for some applications, it is necessary to design the HV transformers with lower interwinding capacitances.

Accurate estimation of the transformer parasitics, and their associated losses are required, to evaluate different transformer winding architectures (TWAs), from which the best TWA can be selected, to achieve high energy efficiency. Extensive research has been done for calculating the leakage inductance in conventional transformers [12]-[19]. The capacitance calculation methods have been proposed for inductors, power, planar, and high voltage transformers in [20]-[28]. In [29], [30], the equations for ac resistance calculation are provided. In this paper, the equations to calculate the self-capacitance, leakage inductance and ac resistance for several TWAs are provided.

The influence of transformer parasitics for a low power HV flyback converter has been discussed in [7]. This paper investigates a number of TWAs, to provide a deep insight into transformer design, and its impact on the total loss contribution in a HV bidirectional flyback converter. Two different transformers (with RM8 and EF25 cores), with turns ratios 10 and 20, respectively, are investigated, and practically implemented. The paper is organized as follows: following the introduction, Section II describes the TWAs. Sections III, IV and V provide the calculations of self-capacitance, leakage inductance and ac resistance for different TWAs, respectively. In Section VI, the calculated transformer parasitics are evaluated via FEA simulation using ANSOFT Maxwell. Section VII compares the calculated, simulated, and measured transformer parasitics, for seven different implementations of a RM8 transformer. Section VIII provides the measured transformer parameters, for four different implementations of an EF25 transformer, followed by the conclusions in Section IX.

II. TRANSFORMER WINDING ARCHITECTURES (TWAs)

This paper investigates the four known winding schemes (A, B, C and D) as shown in Fig. 2 [12], [27], [28]. Winding scheme

A is the most simple to implement since the next layer starts where the previous layer ended. In winding scheme B, the next layer starts just above the starting point of the previous layer. Winding scheme C split the winding into a number of sections, and each section is individually wounded like winding scheme B. In winding scheme D (bank or progressive winding), the turns progress in a vertical back angled way, where the turns are built on the top of previous turns. It seems like winding scheme D achieves as many angled sections as there are turns in a layer, without the penalty of reducing the fill factor, due to the thickness of the section walls of a sectioned bobbin. The bank winding scheme minimizes the voltage difference between adjacent turns (less inter-turn capacitive energy storage). Another advantage is that, winding scheme D can be easily interleaved, which is not the case for winding scheme C, since it is hard to add section walls in-between windings. The difference in self-capacitance due to the winding schemes is severe [27], [28], because the voltage potentials between the adjacent turns in the winding, and the end-to-end winding voltages are changed.

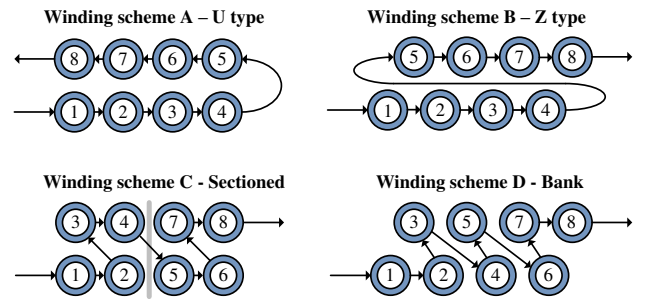


Fig. 2. An overview of different winding schemes: A – U type; B – Z type; C – Sectioned; D – Bank.

Several winding buildups (S/P, S/P/S, and S/P/S/P/S/P/S; where S and P are the secondary and primary windings, respectively) are investigated - see Fig. 3. Based on these configurations, seven HV transformer winding architectures (W_1 - W_7) are derived and the winding information is summarized in Table I. In order to simplify the implementation of the windings a low turns ratio of 10 is selected. The TWAs W_1 - W_6 are wound with 10 primary turns and 100 secondary turns. The TWA W_7 is only implemented with 9 primary turns, due to the nature of the winding architecture. Winding scheme A is employed for the primary winding of all architectures. Moreover, all winding space of the bobbin is utilized to improve the fill factor and to reduce the winding resistance. Equal space allocation for primary (50%) and secondary (50%) winding is adopted for this investigation, thus the primary winding is wound with a number of parallel wires.

III. SELF-CAPACITANCE

High voltage transformers tend to have a large number of turns in the HV side, which introduces a non-negligible parasitic self-capacitance. It is important to predict the self-capacitance in the design phase in order to avoid severe switching loss, and other problems. The winding self-capacitance is a parameter representing the electric field energy stored in the winding and is considered as a shunt lumped

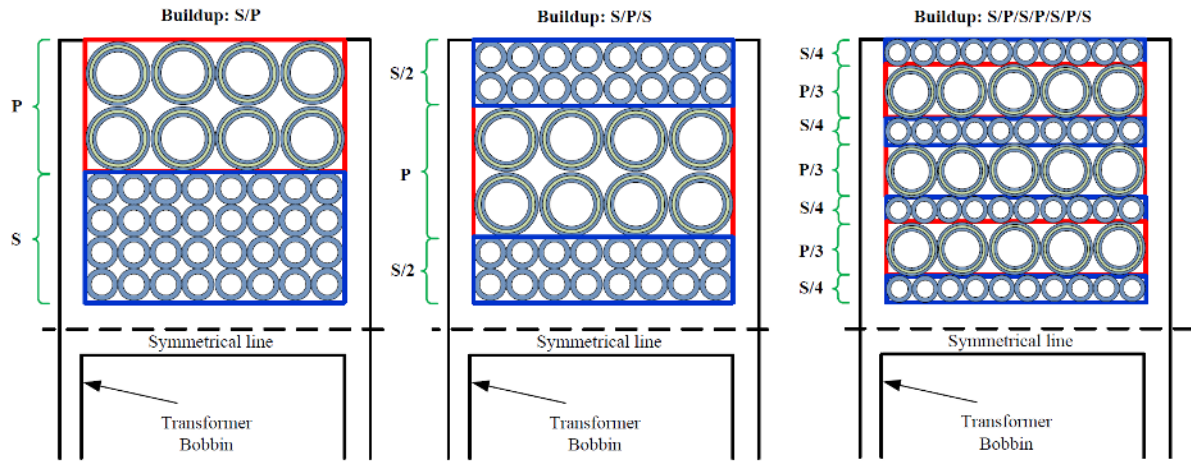


Fig. 3. An overview of different winding builds or arrangements (The figure is purely illustrative and the number of primary and secondary turns are different from the practical values).

TABLE I
HIGH VOLTAGE TRANSFORMER ARCHITECTURES

Design	Winding buildup	Secondary winding		Primary winding Parameters
		Scheme	Parameters	
W ₁	S/P	A	$N_s = 100$	$N_p = 10$ $*d_{ip} = 0.7$ mm $*d_{op} = 0.8$ mm $n_{ip} = 2$ $n_{parp} = 2$
W ₂	S/P	B	$d_{is} = 0.3$ mm	
W ₃	S/P	C	$d_{os} = 0.32$ mm	
W ₄	S/P	D	$p_{TT} = 0.355$ mm	
W ₅	S/P/S	B	$p_{LL} = 0.34$ mm	
W ₆	S/P/S	D	$n_{is} = 4$ $n_{pars} = 1$	
W ₇	S/P/S/P/S /P/S	B	Core / Material used: RM8 / N41	$N_p = 9$ $*d_{ip} = 0.48$ mm $*d_{op} = 0.5$ mm $n_{ip} = 3$ $n_{parp} = 5$

Parameters interpretation

N_s / N_p - number of secondary / primary turns;
 n_{is} / n_{ip} - number of secondary / primary winding layers;
 n_{pars} / n_{parp} - number of secondary / primary parallel windings;
 d_{is} / d_{os} - inner / outer diameter of secondary winding;
 d_{ip} / d_{op} - inner / outer diameter of primary winding;
 p_{TT} / p_{LL} - turn-to-turn / layer-to-layer pitch of secondary winding;
 *In the practical transformer implementation triple insulated (TEX) windings are not used for the primary due to the non-availability of the wires;

element in most cases [12], [27]. Due to large number of turns per layer, the effect of the turn-to-turn capacitance can be neglected, and the main contribution to the self-capacitance comes from the layer-to-layer capacitance, which can be calculated based on the simple parallel-plate or cylindrical capacitor model [12], [27], [28].

The self-capacitance in the transformer windings can be calculated using the electro static energy stored in the volume between the conductors, and is given by

$$E_{Electric} = \frac{1}{2} \iiint_{Vol} \epsilon E^2 dv = \frac{1}{2} C_S U_W^2 \quad (1)$$

where ϵ is the equivalent dielectric constant of the winding, E is the electric field strength, C_S is the self-capacitance, and U_W is the total voltage across the winding.

Two parallel plate capacitors with a linear potential distribution and a cylindrical capacitor model are shown in Figs. 4a) and 4b), respectively. The energy stored in two adjacent conductive layers [12] with a linear potential distribution, shown in Fig. 4a), is given by

$$E_{Stored} = \frac{C_l}{6} (U_S^2 + U_S U_T + U_T^2) \quad (2)$$

where U_S and U_T are the potential difference between the two surfaces at the bottom and top respectively. C_l is the capacitance between the two surfaces, and is considered as a parallel plate capacitance and is given by

$$C_l = \epsilon_r \epsilon_0 \frac{h \cdot w}{d_{eff}} \quad (3)$$

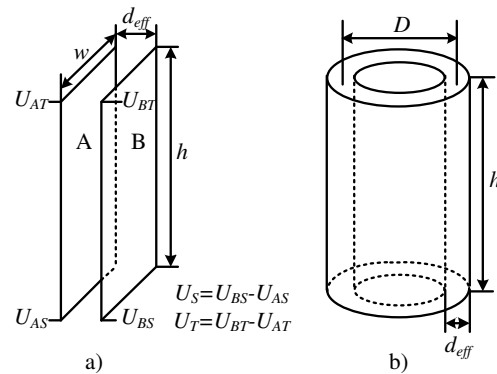


Fig. 4. a) Two parallel plates with a linear potential distribution, b) Cylindrical capacitor model.

where ϵ_0 is the vacuum permittivity and is 8.854×10^{-12} F/m, ϵ_r is the relative permittivity of the dielectric material. The parameters h, w represents the dimensions of the plate, and d_{eff}

is the effective distance between two layers (which needs to be calculated for each TWA) and is given by

$$d_{eff} = p_{LL} - 1.15d_{is} + 0.26p_{TT} \quad (4)$$

where p_{LL} , d_{is} and p_{TT} are the layer to layer pitch, inner diameter, and turn to turn pitch, of the secondary winding, respectively. According to the methods given in [12], the expressions for calculating the self-capacitance for all above mentioned TWAs have been derived and are summarized in Table II. Normally, the cylindrical shape, shown in Fig. 4b), is desired for most winding layers due to the simple winding technique as well as the short mean turn length [27]. If the distance between two layers is much less than the mean diameter for the two layers, the cylindrical capacitor can be considered to be a parallel plate capacitor and (3) can be employed to calculate the capacitance by replacing w with πD (see Fig. 4b)).

TABLE II
SELF-CAPACITANCE EXPRESSIONS FOR DIFFERENT TWAS

TWA	Self-capacitance expression
W ₁	$4 \frac{(n_{is} - 1) C_l}{n_{is}^2} \frac{C_l}{3}; C_l = \epsilon_r \epsilon_0 \frac{b_w l_{w1}}{d_{eff1}}; l_{w1} = \pi(D_i + n_{is} d_{is} + (n_{is} - 1) h_{is})$
W ₂	$4 \frac{(n_{is} - 1) C_l}{n_{is}^2} \frac{C_l}{4}; C_l = \epsilon_r \epsilon_0 \frac{b_w l_{w1}}{d_{eff1}}; b_w = (T_{is} - 1) p_{TT} + d_{os}$
W ₃	$\frac{4(n_{is} - 1) C_l}{q_1 n_{is}^2} \frac{C_l}{3}; C_l = \epsilon_r \epsilon_0 \frac{q_1 l_{w1}}{d_{eff1}}$
W ₄	$\epsilon_r \epsilon_0 \frac{p_{TT} l_{w1}}{d_{eff2}} \frac{L}{b_w}; L = (n_{is} - 1) p_{LL} + d_{os}$ [21]
W ₅	$\frac{\epsilon_r \epsilon_0 b_w}{n_{is}^2} \left[\frac{l_{w2}}{d_{eff3}} + \frac{l_{w3}}{d_{eff3}} + \frac{l_{w4}}{d_{eff3} + n_{ip} d_p + (n_{ip} - 1) h_{ip}} \right]$
W ₆	$\epsilon_r \epsilon_0 \left[\frac{p_{TT} (l_{w2} + l_{w3}) L_1}{d_{eff4}} + \frac{p_{TT2} l_{w4} L_2}{d_{eff4} + n_{ip} d_p + (n_{ip} - 1) h_{ip} b_w} \right];$ $L_1 = \left(\frac{n_{is} - 1}{2} \right) p_{LL} + d_{os}; p_{TT2} = n_{ip} h_p + (n_{ip} - 1) h_{ip} + d_{os};$ $L_2 = p_{TT2} + d_{os}$
W ₇	$\frac{\epsilon_r \epsilon_0 b_w}{n_{is}^2} \left[\frac{l_{w5} + l_{w6} + l_{w7}}{d_{eff5}} \right]$

Parameters interpretation

ϵ_0 / ϵ_r - relative permittivity of vacuum / dielectric material, and $\epsilon_r = 4$;
 b_w - the width of the layer;
 T_{is} is turns per layer of secondary winding;
 D_i - inner diameter of the bobbin;
 $d_{eff1,2,3,4,5}$ - effective thickness of dielectric between two layers [12] [27] for different TWAs;
 l_{w1} - mean length turn for the TWAs W₁, W₂, W₃ and W₄;
 $l_{w2} / l_{w3} / l_{w4}$ - mean length turn between most inner two secondary (S₁, S₂) / most outer two secondary (S₃, S₄) / most outer secondary and the most inner secondary (S₂, S₃), layers for W₅ [S₁-S₂-P-S₃-S₄] and W₆ [S₁-S₂-P-S₃-S₄];
 $l_{w5} / l_{w6} / l_{w7}$ - mean length turn between most inner two secondary (S₁, S₂) / middle two secondary (S₂, S₃) / most outer two secondary (S₃, S₄) layers for W₇ [S₁-P₁-S₂-P₂-S₃-P₃-S₄];
 q_1 - number of sections for the TWA W₃ and $q_1 = 4$;
 For remaining variables definitions refer to Tables I and III;

IV. LEAKAGE INDUCTANCE

The leakage inductance in a transformer is calculated using the energy stored in the magnetic field [12]. The total leakage energy stored in the magnetic field is given by

$$E_{Magnetic} = \frac{1}{2} \iiint_{Vol} \mu_0 H^2 dv = \frac{1}{2} L_k I_p^2 \quad (5)$$

where H is the magnetic field strength which is proportional to the number of ampere turns linked by the flux path, L_k is the leakage inductance, and I_p is the peak current in the winding. The fundamental principles used to calculate the leakage inductance are thoroughly investigated in [12], [14], [18] and [19]. Based on those methods, the equations for calculating the leakage inductances at low frequency, for TWAs W₁-W₇ have been derived, and are summarized in Table III [11]. The magneto motive force (MMF) distributions for all TWAs are provided in Fig. 5. The MMFs in each primary and secondary layers of a non-interleaved structure (Fig. 5a) are $T_{ip} I_p$ and $T_{is} I_s$, respectively.

TABLE III
LEAKAGE INDUCTANCE REFERRED TO PRIMARY EXPRESSIONS FOR DIFFERENT TWAS

TWA	Leakage inductance expression
W ₁ , W ₂ , W ₃ , W ₄	$\mu_0 l_w N_p^2 \left[\frac{1}{b_w} \left(\frac{n_{ip} h_p}{3} + \frac{(2n_{ip} - 1)(n_{ip} - 1)}{6} \left(\frac{h_{ip}}{n_{ip}} \right) + h_i \right) + \frac{1}{b_{w2}} \left(\frac{n_{is} h_s}{3} + \frac{(2n_{is} - 1)(n_{is} - 1)}{6} \left(\frac{h_{is}}{n_{is}} \right) \right) \right]$
W ₅ , W ₆	$\frac{\mu_0 l_w N_p^2}{b_w} \left[\frac{n_{is1}^3 + n_{is2}^3}{3(n_{is1} + n_{is2})^3} (n_{ip} h_p + (n_{is1} + n_{is2}) h_s) + \frac{n_{is1}^2 + n_{is2}^2}{(n_{is1} + n_{is2})^2} h_i + \left\{ \frac{n_{is1} (n_{is1} - 1)(2n_{is1} - 1) + n_{is2} (n_{is2} - 1)(2n_{is2} - 1)}{6(n_{is1} + n_{is2})^2} \right\} h_{is} + \left\{ \frac{(n_{ip} - 1) \left(\frac{n_{is1} n_{ip}}{n_{is1} + n_{is2}} \right)^2 + n_{ip} (n_{ip} - 1)(2n_{ip} - 1)}{6} \right\} \frac{h_p}{n_{ip}^2} + \left\{ \frac{n_{is1}^2 n_{ip} (n_{ip} - 1)}{n_{is1} + n_{is2}} \right\} \right]$
W ₇	$\mu_0 \frac{l_w}{b_w} N_p^2 \left[\frac{3h_p + 4h_s}{72} + \frac{7}{36} h_i \right]$

Parameters interpretation

μ_0 - permeability of free air;
 l_w - mean length turn (MLT) of the winding;
 b_w - width of the layer;
 b_{w2} - width of the layer excluding the combined width of the sections walls for TWA W₃, $b_{w2} < b_w$;
 For W₁, W₂ and W₄, $b_w = b_{w2}$;
 $h_p = d_{op}$ and $h_s = d_{os}$;
 $h_{ip} / h_{is} / h_i$ - insulation thickness between primary-to-primary layer / secondary-to-secondary layer / primary-to-secondary layer;
 For W₅ and W₆, n_{is1} and n_{is2} are the number of secondary layers at the top and bottom of a primary winding respectively, having n_{ip} primary layers;
 In Fig. 5c), $n_{is1}=2$ and $n_{is2}=2$;
 For remaining variables definitions refer to Tables I and II.

V. AC RESISTANCE

The ac resistance is calculated using equations commonly found in the literature [10], [13], [29]-[30]. The dc resistance of the primary/secondary winding can be calculated by

$$R_{DC} = \frac{\rho l_w N}{A n_{par}}, \quad A = \frac{\pi d_i^2}{4} \quad (6)$$

where ρ is the resistivity of copper at room temperature ($\rho=17.24 \text{ n}\Omega/\text{m}$ at $20 \text{ }^\circ\text{C}$), N is the total number of primary/secondary turns, l_w is the mean length turn of the winding, n_{par} is the number of parallel wires, A is the cross sectional area of the winding, and d_i is the inner diameter of the winding excluding the insulation thickness.

The ac resistance per layer of a given winding is given by [30], [36]

$$R_{AC,layer} = R_{DC,layer} Q \left\{ \begin{array}{l} (2m^2 - 2m + 1) \frac{\sinh(2Q) + \sin(2Q)}{\cosh(2Q) - \cos(2Q)} - \\ 4(m^2 - m) \frac{\cos(Q) \sinh(Q) - \sin(Q) \cosh(Q)}{\cosh(2Q) + \cos(2Q)} \end{array} \right\} \quad (7)$$

The derivation for (7) is provided in Appendix A. In (7), $R_{DC,layer}$ is the dc resistance per layer of a given winding. The variable m represents the effective number of layers and is given by [10]

$$m = \frac{F(h)}{F(h) - F(0)} \quad (8)$$

where $F(0)$ and $F(h)$ are the magneto motive forces (MMFs) at the start and end of each layer, respectively. The variable Q is the effective layer thickness normalized with the skin depth, and is given by

$$Q = \frac{\text{layer thickness}}{\text{penetration depth}} = \frac{\frac{\pi^{3.5}}{4} d_i \sqrt{\frac{d_o T_l}{b_w}}}{\sqrt{\frac{\rho}{\pi \mu_0 f}}} \quad (9)$$

where d_i is the bare wire diameter, d_o is the overall wire diameter including insulation, T_l is the turns per layer of the given winding, and f is the switching frequency.

Assume the variables $\Delta_1, \Delta_2, \Delta_3,$ and Δ_4 are assigned as given below,

$$\begin{aligned} \Delta_1 &= \frac{\sinh(2Q) + \sin(2Q)}{\cosh(2Q) - \cos(2Q)}; \quad \Delta_3 = \frac{\sinh(Q) + \sin(Q)}{\cosh(Q) - \cos(Q)}; \\ \Delta_2 &= \frac{\cos(Q) \sinh(Q) - \sin(Q) \cosh(Q)}{\cosh(2Q) + \cos(2Q)}; \quad \Delta_4 = \frac{\sinh(Q) - \sin(Q)}{\cosh(Q) + \cos(Q)}; \end{aligned} \quad (10)$$

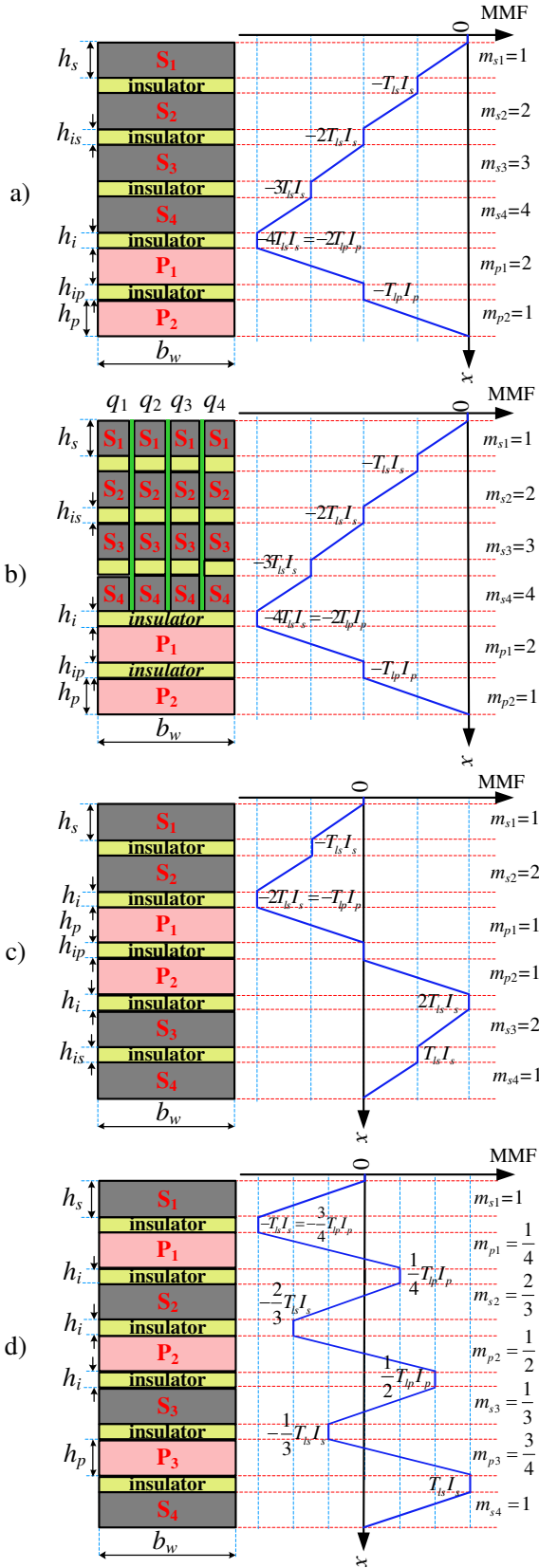


Fig. 5. Analytical MMF distribution for, a) non-interleaved structure (S/P - W₁, W₂, W₄), b) non-interleaved structure (S/P - W₃), c) interleaved structure (S/S/P/P/S - W₅, W₆), d) fully interleaved structure (S/P/S/P/S/P/S - W₇).

The variable Δ_1 in terms of Δ_3 and Δ_4 , and Δ_2 and Δ_4 is given by [30]

$$\Delta_1 = \frac{1}{2}(\Delta_3 + \Delta_4), \quad \Delta_2 = (2\Delta_2 + \Delta_4) \quad (11)$$

Using (10), (11) in (7), the simplified ac resistance per layer is

$$R_{AC,layer} = R_{DC,layer} Q \left\{ \Delta_1 + 2(m^2 - m)\Delta_4 \right\} \quad (12)$$

$$R_{AC,layer} = R_{DC,layer} \frac{Q}{2} \left\{ \Delta_3 + (2m-1)^2 \Delta_4 \right\} \quad (13)$$

The total ac resistance of M layers for the non-interleaved TWAs W_1 - W_4 is given by

$$\begin{aligned} R_{AC,total} &= R_{DC,layer} Q \left[\sum_{m=1}^M \left\{ \Delta_1 + 2(m^2 - m)\Delta_4 \right\} \right] \\ &= (R_{DC,layer} M) Q \left[\Delta_1 + \frac{2}{3}(M^2 - 1)\Delta_4 \right] \\ &= R_{DC,total} Q \left[\Delta_1 + \frac{2}{3}(M^2 - 1)\Delta_4 \right] \end{aligned} \quad (14)$$

where $R_{DC,total}$ is the total dc resistance of M layers.

To calculate the ac resistance per layer for the interleaved TWAs W_5 - W_7 , (12) or (13) needs to be calculated with the corresponding value of m for each layer. The total ac resistance is the sum of all ac resistances in each layer. The total ac resistance referred to the primary is given by

$$R_{AC} = R_{AC,total,P} + \frac{R_{AC,total,S}}{n^2} \quad (15)$$

where n is the transformer turns ratio, $R_{AC,total,P}$ and $R_{AC,total,S}$ are the total ac resistance of primary and secondary windings, respectively.

In a flyback converter, the primary and secondary currents are 180° out of phase; hence, the conventional equations [29], [30] cannot be used to calculate the ac resistance. The calculation of the total winding loss in a flyback converter [31], [32] using the magneto motive force (MMF) analysis is described in [7].

VI. FINITE ELEMENT ANALYSIS

Different winding architectures (W_1 - W_7) are simulated in Ansoft Maxwell to extract the values of the leakage inductances, self-capacitances and ac resistances. In Fig. 6, the electrostatic energy between the windings is shown for winding schemes B and D. It is noted that the energy density is high between layer to layer, and low between turn to turn as expected in winding scheme B, as shown in Fig. 6(a). In winding scheme D, there is a less electrostatic energy between the layers as shown in Fig. 6(b), and thus it has a lower self-capacitance.

Figure 7 shows a close-up of the magneto static energy of the three investigated winding buildups. The leakage flux runs approximately vertically through the windings, and the magneto static energy is highest in the space between the primary and secondary windings. The heavy interleaved buildup (S/P/S/P/S/P/S) has a very low magneto static energy, and thus it will have a very low leakage inductance. The non-interleaved, interleaved, and fully interleaved simulation results are provided in Figs. 7(a), 7(b), and 7(c), respectively. In the non-interleaved buildup, more magneto static energy is stored, between the primary and secondary windings, compared to the interleaved and fully interleaved buildups. Hence, the non-interleaved buildup will have very high leakage inductance.

The ac resistance at 100 kHz is also simulated for the three winding buildups. A standard mesh which is very fine compared to the skin depth is used to simulate the eddy effects in the winding. A close up plot of the mesh is shown in Fig. 8(a). The diameter of the secondary winding is 0.3 mm and the skin depth at 100 kHz is approximately 0.2 mm. It is noted that the dimensions of the mesh is much lower than the diameter of the winding, and the skin depth at 100 kHz. In Figs. 8(b)-8(d), a close up of the current density for the three winding buildups is shown. It is noted that the current density in the non-interleaved buildup is much higher compared to the others, and thus the ac resistance will also be higher.

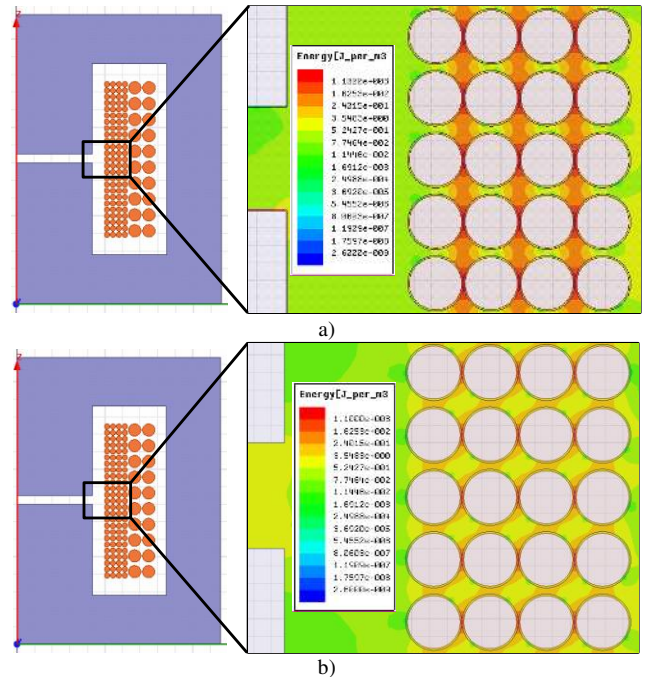


Fig. 6. Plots from simulation of self-capacitance: a) Energy distribution for winding scheme B; b) Energy distribution for winding scheme D.

VII. EXPERIMENTAL RESULTS

The measurement setup with 5 of the RM8 transformer prototypes is shown in Fig. 9. The measurement of the transformer parasitics is carried out by the frequency response analyzer PSM1735. The simulated, calculated and measured values [6] of the self-capacitance (measured using the resonance frequency of the impedance plot), leakage

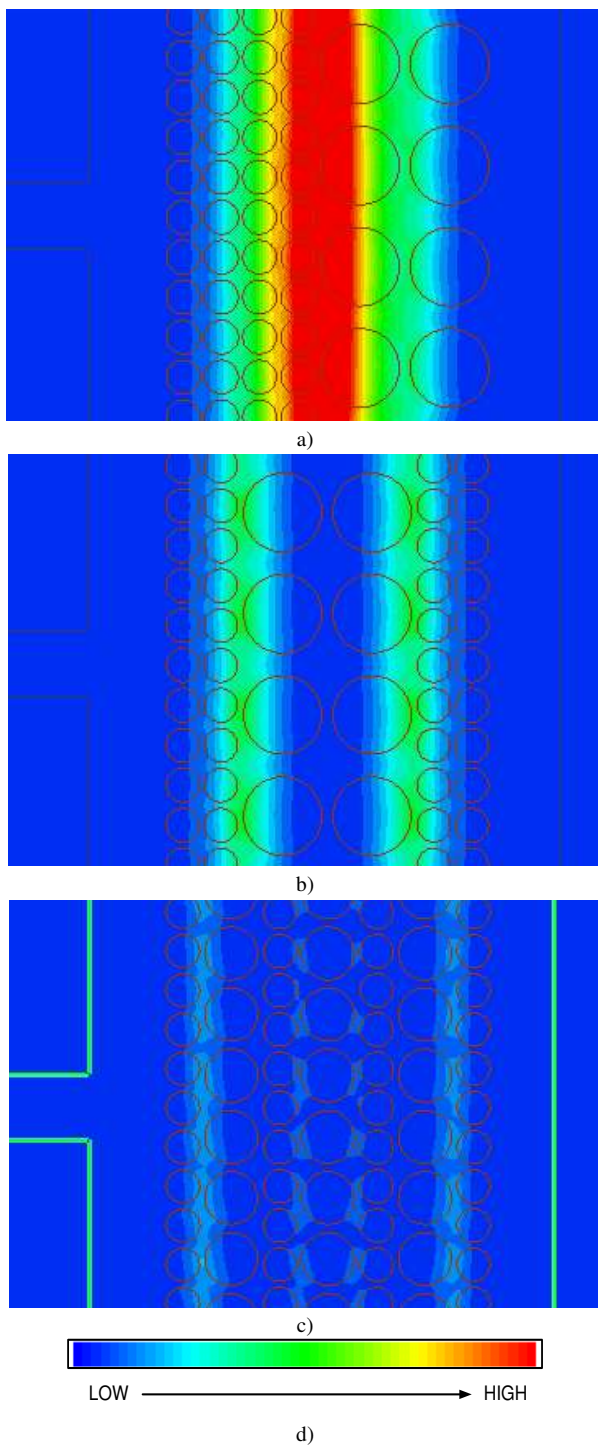


Fig. 7. Plots from simulation of leakage inductance: a) P/S. b) S/P/S. c) S/P/S/P/S/P/S. d) Density color bar.

inductance (measured at 10 kHz frequency) and ac resistance (measured at 100 kHz frequency) for the 7 TWAs are shown in the Tables IV, V and VI, respectively. From those tables, it is clear that the measured, calculated and simulated transformer parameters for most of the TWAs closely matches. However, the differences in winding parameters such as an average layer to layer distance and mean length turn may cause errors around $\pm 20\%$, in cases where the implementation complexity of the TWAs is high.

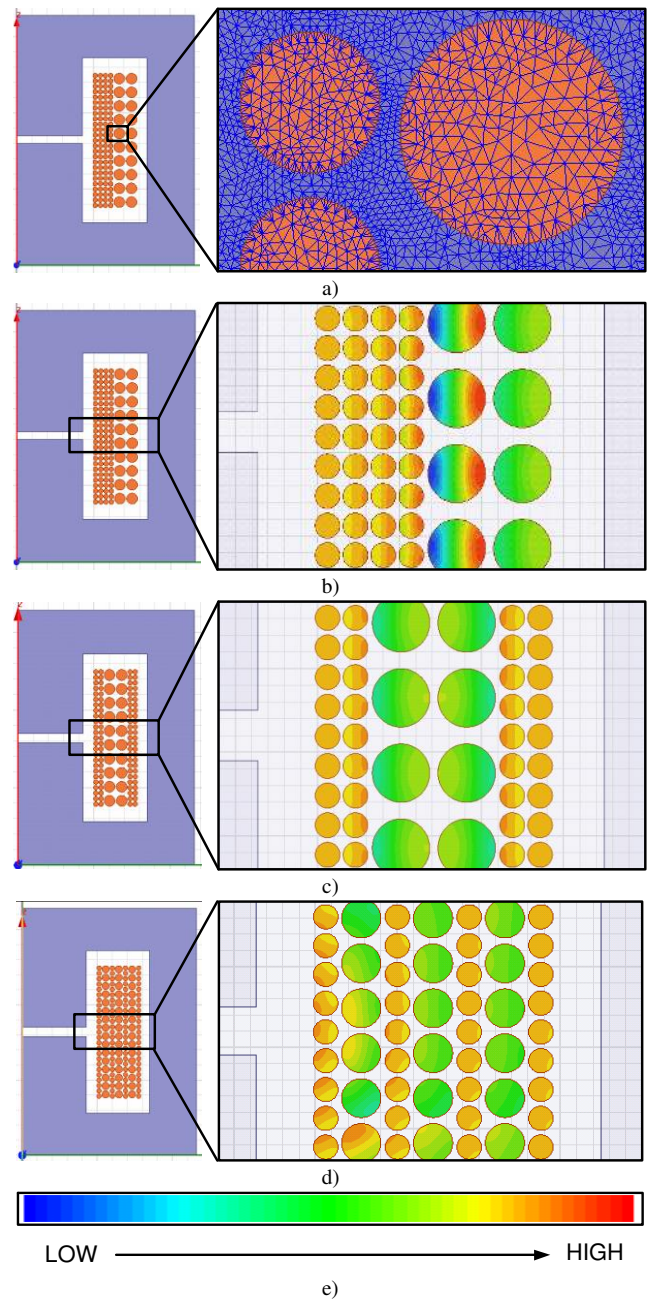


Fig. 8. Plots from the simulations of AC resistance: a) Default mesh; b) Current density of W₁-W₄; c) Current density of W₅-W₆; d) Current density of W₇; e) Density color bar.

There are some discrepancies between the simulations, calculations, and measurements of the self-capacitance and leakage inductance of W₃, W₅, W₆, and W₇. In self-capacitance calculations, a small change in the mean length turn (MLT) l_w of the winding and effective distance d_{eff} between two secondary layers, and the effective permittivity of the dielectric material ϵ_r significantly changes the self-capacitance value. When two dielectrics of different ϵ_r are connected, the equivalent ϵ_r value changes. In leakage inductance calculations, a small difference in the mean length turn (MLT) of the winding, and the effective window width b_w , considerably changes the leakage inductance value.

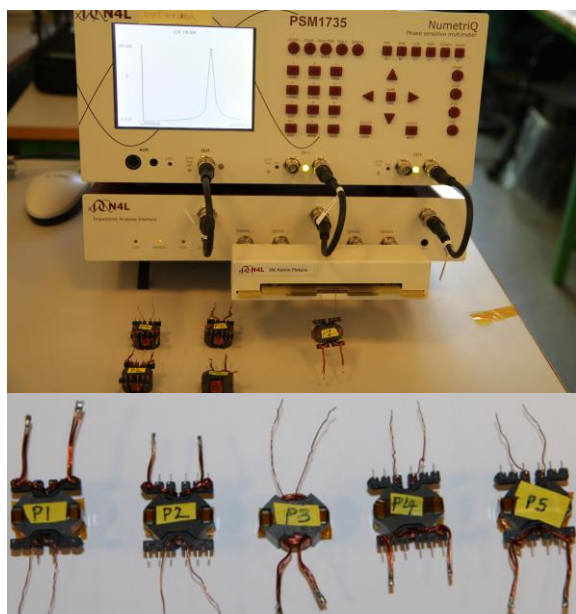


Figure 9. Measurement setup and five transformer prototypes with RM8 core.

TABLE IV
SELF-CAPACITANCE OF SECONDARY HV WINDING

TWA	Buildup	Winding scheme	Sim. (pF)	Calc. (pF)	Meas. (pF)
W ₁	S/P	A	33	32	28
W ₂	S/P	B	25	24	26
W ₃	S/P	C	2.4	2	4.2
W ₄	S/P	D	1.9	1	1.3
W ₅	S/P/S	B	10	20	22
W ₆	S/P/S	D	3.3	2.1	6
W ₇	S/P/S/P/S/P/S	B	5	3.6	15

TABLE V
LEAKAGE INDUCTANCE REFERRED TO PRIMARY

TWA	Buildup	Winding scheme	Sim. (nH)	Calc. (nH)	Meas. (nH)
W ₁	S/P	A	526	590	550
W ₂	S/P	B			520
W ₃	S/P	C			725
W ₄	S/P	D			580
W ₅	S/P/S	B	150	152	181
W ₆	S/P/S	D			208
W ₇	S/P/S/P/S/P/S	B	30	22	74

For TWA W₃ (non-interleaved and sectioned), the discrepancy between the calculation and measurement of the self-capacitance, is due to a small increase in the MLT, and a

TABLE VI
AC RESISTANCE REFERRED TO PRIMARY AT 100 KHZ

TWA	Buildup	Winding scheme	Sim. (mΩ)	Calc. (mΩ)	Meas. (mΩ)
W ₁	S/P	A	102	110	130
W ₂	S/P	B			127
W ₃	S/P	C			135
W ₄	S/P	D			84
W ₅	S/P/S	B	35	37	39
W ₆	S/P/S	D			42
W ₇	S/P/S/P/S/P/S	B	23	18	22

small reduction in effective distance d_{eff} , when the winding is practically implemented. Similarly, the discrepancy in the leakage inductance for TWA W₃, is due to a decrease in the value of the effective window width, due to the sectioned bobbin. For TWA W₅ (interleaved and Z-type), the difference between the simulation and calculation (or measurement) of the self-capacitance could be due to a change in the value of effective permittivity ϵ_r , which might not be considered during the Maxwell simulations of that particular TWA.

The TWA W₆ (interleaved and bank wound) was extremely difficult to implement in the laboratory. The difference between the calculation and measurement of the self-capacitance is due to an increase in the MLT (due to interleaving), when the winding is practically implemented. Similarly, the discrepancy in the leakage inductance for TWA W₆, could be due to an increase in the MLT of the winding. For TWA W₇ (fully interleaved) the discrepancies between the calculation and measurement of the self-capacitance and leakage inductances are due to an increase in the MLT of the winding, due to heavy interleaving.

A plot of the loss distribution of the energy losses caused by the transformer parasitics, in a bidirectional flyback converter, used for charging and discharging an incremental DEAP actuator [6] is shown in Fig. 10. The winding loss calculation for the flyback transformer is different from that of normal transformer, since the primary and secondary currents are out of phase, in [7] the winding loss is calculated for a flyback transformer with a non-interleaved structure. The same method can be used for the interleaved structures as well.

The calculated transformer parasitics values are used for calculating all losses, in order to provide a fair and useful comparison of the losses. The following specifications are used to calculate the losses in the bidirectional flyback converter [33]: input voltage: 24 V, output voltage: 1500 V, load capacitance: 200 nF, switching frequency during the charging and discharging process: 20-200 kHz, and 26 kHz, respectively, and primary peak current during charge and discharge processes: 2.12 A. The primary magnetizing inductance: 35 μ H. From Fig. 10, it is clear that W₆ has the lowest loss among all TWAs followed by W₄, W₇ and W₃. Thus, the structure W₆ is highly recommended for high voltage capacitor charging application. In the leakage inductance calculations, the high

frequency effects are not considered, because 200 kHz is still a low frequency, and the skin effect will not affect the leakage inductance below 200 kHz.

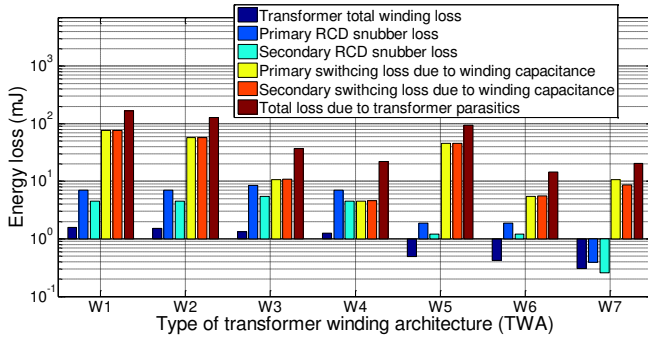


Figure 10. Energy loss distribution of the losses caused by transformer parasitics in the high voltage capacitor charging application.

VIII. INVESTIGATION USING AN EF25 CORE

A. Practical implementation:

The TWAs investigated in the above sections using RM8 core are not suitable for generating the maximum voltage of 2.5 kV, which is needed to drive the DEAP actuators. Hence, it is needed to investigate the parameters of the transformer further with a higher turns ratio (e.g., $n=20$). From Section VII, the interesting TWAs for the mentioned actuator application are W_3 , W_4 , and W_6 . When the secondary turns are very high, implementing the TWAs with bank winding scheme (W_4 and W_6) in the laboratory was extremely difficult, and hence W_3 was considered. Table VII provides the details of transformer design using EF25 core [35].

In addition, four different TWAs such as non-interleaved and non-sectioned (W_2), interleaved and non-sectioned (W_5), non-interleaved and sectioned (W_3), and interleaved and sectioned (W_8 , which is a new TWA) have been practically implemented, using an EF25 transformer. The measured parameters of the transformer for each TWA are provided in Tables VIII, IX, X, and XI, respectively.

TABLE VII
DETAILS OF THE TRANSFORMER WITH A TURNS RATIO OF 20

Parameter	Value
Number of primary / secondary turns	18 / 360
Diameter of primary / secondary winding	0.4 mm (TEX [34]) / 0.14 mm
Number of layers of primary / secondary winding	3 / 4
Number of parallel wires of primary / secondary	3 / 1
Type of core / material	EF25 / N87

By comparing the transformer parasitics of all TWAs with an EF25 core, the non-interleaved and sectioned TWA (W_3) has the lowest self and interwinding capacitances, followed by the interleaved and sectioned TWA (W_8). The self-capacitances of TWAs W_8 and W_3 are comparable. However, the leakage inductance of W_8 is approximately half of W_3 , due to very high

TABLE VIII
PARAMETERS FOR NON-INTERLEAVED (P/S) AND NON-SECTIONED TRANSFORMER [W_2]

Parameter	Value
Magnetizing inductance of primary / secondary	53 μ H / 23 mH
Leakage inductance referred to primary / secondary	1.2 μ H / 490 μ H
DC resistance of primary / secondary winding	42 m Ω / 16 Ω
AC resistance referred to primary / secondary winding at 50 kHz	98 m Ω / 39 Ω
AC resistance referred to primary / secondary winding at 100 kHz	130 m Ω / 52 Ω
Self-capacitance of the high voltage winding	42 pF
Interwinding capacitance	59 pF

TABLE IX
PARAMETERS FOR INTERLEAVED (S/P/S) AND NON-SECTIONED TRANSFORMER [W_5]

Parameter	Value
Magnetizing inductance of primary / secondary	47 μ H / 20 mH
Leakage inductance referred to primary / secondary	590 nH / 236 μ H
DC resistance of primary / secondary winding	43 m Ω / 19 Ω
AC resistance referred to primary / secondary winding at 50 kHz	98 m Ω / 38 Ω
AC resistance referred to primary / secondary winding at 100 kHz	108 m Ω / 43 Ω
Self-capacitance of the high voltage winding	21.5 pF
Interwinding capacitance	160 pF

TABLE X
PARAMETERS FOR NON-INTERLEAVED (P/S) AND SECTIONED (4 SECTIONS) TRANSFORMER [W_3]

Parameter	Value
Magnetizing inductance of primary / secondary	49 μ H / 21 mH
Leakage inductance referred to primary / secondary	1 μ H / 357 μ H
DC resistance of primary / secondary winding	39 m Ω / 14 Ω
AC resistance referred to primary / secondary winding at 50 kHz	91 m Ω / 38 Ω
AC resistance referred to primary / secondary winding at 100 kHz	117 m Ω / 43 Ω
Self-capacitance of the high voltage winding	4.3 pF
Interwinding capacitance	44 pF

TABLE XI
PARAMETERS FOR INTERLEAVED (S/P/S) AND SECTIONED (4 SECTIONS) TRANSFORMER [W_8]

Parameter	Value
Magnetizing inductance of primary / secondary	49 μ H / 21.5 mH
Leakage inductance referred to primary / secondary	420 nH / 175 μ H
DC resistance of primary / secondary winding	43 m Ω / 19 Ω
AC resistance referred to primary / secondary winding at 50 kHz	90 m Ω / 39 Ω
AC resistance referred to primary / secondary winding at 100 kHz	100 m Ω / 43 Ω
Self-capacitance of the high voltage winding	6.8 pF
Interwinding capacitance	150 pF

interwinding capacitance, making it unsuitable for high voltage capacitor charge and discharge applications where conducted and radiated EMI are critical. From the above observations, it can be concluded that redesigning the transformer to reduce the interwinding capacitance, usually leads to increased leakage inductance. In other words, interleaving the transformer reduces the leakage inductance and increases the interwinding capacitance.

B. Discussion:

If it is not possible to progressively wind the secondary winding in high turns ratio transformers, it is better to always section the bobbin for end-to-end winding voltages greater than around 250 VRMS which ensures safety and reliability. Furthermore, the maximum voltage rating of the wire insulation should not be exceeded. Almost all transformers in medical applications, have a Farady shield (not a continuous metal layer around the core, it has gap between the ends) between the primary layer(s) and the secondary. This will minimize the common-mode capacitance and help EMI as well. Common mode capacitive coupling is seen and measured during Hi-pot AC testing of the transformer [37].

IX. CONCLUSIONS

The analytical equations for calculating the transformer ac resistance, leakage inductance and self-capacitance for seven different winding architectures have been presented. The calculated parasitics for a RM8 transformer, with a turns ratio of 10, are evaluated experimentally, and with FEA simulations. The main contribution to the errors in the comparison, is due to practical winding issues which are not accounted for in the equations. The flyback transformer energy loss distribution is based on the calculated values, and it clearly shows that the TWAs where the self-capacitance is lowest are particularly suitable for high voltage charging applications. Another investigation has been made with an EF25 transformer having a turns ratio of 20. For applications where EMI is not a big problem, interleaved and sectioned TWA is the best TWA, since it has lower leakage inductance compared to the non-interleaved and sectioned TWA. Nevertheless, non-interleaved and sectioned TWA could be most suitable for HV capacitor charge and discharge applications for applications (e.g., medical) where EMI is a major problem.

APPENDIX A

To find the power dissipation in a winding layer, the current density distribution within a layer is integrated. The current density is obtained by solving the Maxwell's equations [31]. Integrating it gives the total copper loss P in layer, and is given by [10],

$$P = R_{DC,layer} \frac{Q}{T_l^2} \left\{ (F^2(h) + F^2(0)) \Delta_1 - 4F(h)F(0) \Delta_2 \right\} \quad (A1)$$

Refer to Section V, for the definition of all variables in (A1). If $F(0)$ and $F(h)$ are the magneto motive forces (MMFs) at the start and end of each layer, respectively. If I is the current flowing through the winding, then,

$$F(h) - F(0) = T_l I \quad (A2)$$

$F(h)$ can be rewritten in terms of m as

$$F(h) = m T_l I \quad (A3)$$

From (A2) and (A3),

$$\frac{F(0)}{F(h)} = \frac{m-1}{m} \quad (A4)$$

The power loss P becomes

$$\begin{aligned} P &= R_{DC,layer} \frac{Q}{T_l^2} F^2(h) \left\{ \left(1 + \frac{F^2(0)}{F^2(h)} \right) \Delta_1 - 4 \frac{F(0)}{F(h)} \Delta_2 \right\} \\ &= R_{DC,layer} Q \frac{F^2(h)}{T_l^2 m^2} \left\{ (2m^2 - 2m + 1) \Delta_1 - 4m(m-1) \Delta_2 \right\} \end{aligned} \quad (A5)$$

By using (A3) in (A5), the total power loss P is

$$P = R_{DC,layer} Q \cdot I^2 \left\{ (2m^2 - 2m + 1) \Delta_1 - 4m(m-1) \Delta_2 \right\} \quad (A6)$$

If $R_{AC,layer}$ is the effective or ac resistance in a given layer, then (A6) can be re-written as,

$$R_{AC,layer} \cdot I^2 = R_{DC,layer} Q \cdot I^2 \left\{ (2m^2 - 2m + 1) \Delta_1 - 4m(m-1) \Delta_2 \right\} \quad (A7)$$

The ac resistance in a given winding layer is given by,

$$R_{AC,layer} = R_{DC,layer} Q \left\{ (2m^2 - 2m + 1) \Delta_1 - 4m(m-1) \Delta_2 \right\} \quad (A8)$$

REFERENCES

- [1] Y. Bar-Cohen, *Electroactive Polymer [EAP] Actuators as Artificial Muscles: Reality, Potential, and Challenges*, 2nd ed. Washington, DC: SPIE, 2004.
- [2] R. E. Pelrine, R. D. Kornbluh, and J. P. Joseph, "Electrostriction of polymer dielectric with compliant electrodes as a means of actuation," *Sens. Actuators A*, vol. 64, pp. 77–85, 1998.
- [3] R. E. Pelrine, R. D. Kornbluh, Q. Pei, and J. P. Joseph, "High-speed electrically actuated elastomers with strain greater than 100%," *Science*, vol. 287, pp. 836–839, 2000.
- [4] M. Tryson, H. E. Kiil, M. Benslimane, "Powerful tubular core free dielectric electro active polymer (DEAP) push actuator," in *Proc. SPIE*, vol. 7287, 2009.
- [5] R. Sarban, B. Lassen, M. Willatzen, "Dynamic Electromechanical Modeling of Dielectric Elastomer Actuators With Metallic Electrodes," *IEEE/ASME Trans. on Mechatronics*, vol. 17, no. 5, pp. 960–967, Oct. 2012.
- [6] P. Thummala, Z. Zhang, M. A. E. Andersen, S. Rahimullah, "Dielectric electro active polymer incremental actuator driven by multiple high-voltage bi-directional DC-DC converters," in *Proc. IEEE ECCE USA*, Sept. 2013, pp. 3837–3844.
- [7] P. Thummala, H. Schneider, Z. Zhang, Z. Ouyang, A. Knott, M. A. E. Andersen, "Efficiency Optimization by Considering the High Voltage Flyback Transformer Parasitics using an Automatic Winding Layout Technique," *IEEE Trans. Power Electronics*, vol. 30, no. 10, pp. 5755–5768, Oct. 2015.

- [8] P. Thummala, D. Maksimovic, Z. Zhang, M. A. E. Andersen, "Digital control of a high-voltage (2.5 kV) bidirectional DC-DC converter for driving a dielectric electro active polymer (DEAP) based capacitive actuator," in *Proc. IEEE ECCE USA*, Sept. 2014, pp. 3435–3442.
- [9] L. Huang, Z. Zhang, M.A.E. Andersen, "Design and development of autonomous high voltage driving system for DEAP actuator in radiator thermostat," in *Proc. IEEE APEC*, pp. 1633–1640, 16–20 March 2014.
- [10] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," 2nd ed. New York: Springer, 2001.
- [11] H. Schneider, P. Thummala, L. Huang, Z. Ouyang, A. Knott, Z. Zhang, M. A. E. Andersen, "Investigation of transformer winding architectures for high voltage capacitor charging applications," in *Proc. IEEE APEC*, Mar. 2014, pp. 334–341.
- [12] E. C. Snelling, *Soft Ferrites-Properties and applications*, 2nd ed. London, UK, Butterworth, 1988.
- [13] M. K. Kazimierczuk, *High-Frequency Magnetic Components*, 2nd ed. Chichester, U.K.: Wiley, 2009.
- [14] W. G. Hurley and D. J. Wilcox, "Calculation of leakage inductance in transformer windings," *IEEE Trans. Power Electronics*, vol. 9, pp. 121–126, 1994.
- [15] J. Biela and J. W. Kolar, "Electromagnetic integration of high power resonant circuits comprising high leakage inductance transformers," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, pp. 4537–4545.
- [16] Z. Ouyang, Z. Zhang, O. C. Thomsen and M. A. E. Andersen, "Planar-integrated magnetics (PIM) module in hybrid bidirectional DC-DC converter for fuel cell application," *IEEE Trans. Power Electronics*, vol. 26, pp. 3254–3264, 2011.
- [17] S. R. Cove, M. Ordonez, F. Luchino, and J. E. Quaicoe, "Applying Response Surface Methodology to Small Planar Transformer Winding Design," *IEEE Trans. Industrial Electronics*, vol. 60, pp. 483–493, 2013.
- [18] J. Zhang, Z. Ouyang, M. C. Duffy, M. A. E. Andersen, W. G. Hurley, "Leakage Inductance Calculation for Planar Transformers With a Magnetic Shunt," *IEEE Trans. Industry Applications*, vol. 50, no. 6, pp. 4107–4112, Dec. 2014.
- [19] Z. Ouyang, J. Zhang, W. G. Hurley, "Calculation of Leakage Inductance for High-Frequency Transformers," *IEEE Trans. Power Electronics*, vol. 30, no. 10, pp. 5769–5775, Oct. 2015.
- [20] W. T. Duerdoth, "Equivalent capacitance of transformer windings," *Wireless Eng.*, vol. 23, pp. 161–167, Jun. 1946.
- [21] F. Blache, J-P. Keradec, B. Cogitore, "Stray capacitances of two winding transformers: equivalent circuit, measurements, calculation and lowering," *IEEE Industry Applications Society Annual Meeting*, pp. 1211–1217 vol. 2, 2–6 Oct. 1994.
- [22] A. Massarini and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 671–676, Jul. 1997.
- [23] H. Y. Lu, J. Zhu, S. Y. R. Hui, and V. S. Ramesden, "Measurement and Modeling of stray capacitances in high frequency transformers," in *Proc. Power Electron. Spec. Conf.*, pp. 763–769, 1999.
- [24] T. Duerbaum, "Capacitance model for magnetic devices," in *Proc. Power Electron. Spec. Conf.*, vol. 3, pp. 1651–1656, 2000.
- [25] T. Duerbaum and G. Sauerlander, "Energy based capacitance model for magnetic devices," in *Proc. IEEE APEC*, vol. 1, pp. 109–115, 2001.
- [26] H. Y. Lu, J. G. Zhu, and S. Y. R. Hui, "Experimental determination of stray capacitances in high-frequency transformers," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1105–1112, Sep. 2003.
- [27] L. Dalessandro, F. da Silveira Cavalcante, J. W. Kolar, "Self-Capacitance of High-Voltage Transformers," *IEEE Trans. Power Electronics*, vol. 22, no. 5, pp. 2081–2092, Sept. 2007.
- [28] J. Biela, J. W. Kolar, "Using Transformer Parasitics for Resonant Converters—A Review of the Calculation of the Stray Capacitance of Transformers," *IEEE Trans. Industry Applications*, vol. 44, no. 1, pp. 223–233, 2008.
- [29] W.G. Hurley, E. Gath, J. G. Breslin, "Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Trans. Power Electronics*, vol. 15, no. 2, pp. 369–376, Mar 2000.
- [30] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Trans. on Power Electronics*, vol. 9, no. 1, pp. 127,131, Jan 1994.
- [31] J. Vandellac and P. D. Ziogas, "A novel approach for minimizing high frequency transformer copper losses," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 266–277, Jul. 1988.
- [32] S. H. Kang, "Efficiency optimization in digitally controlled flyback DC-DC converters over wide ranges of operating conditions," Ph.D. dissertation, Dept. Electr., Comput. Energy Eng., Univ. Colorado Boulder, Boulder, CO, USA, 2011.
- [33] P. Thummala, Z. Zhang, M. A. E. Andersen, "High Voltage Bi-directional Flyback Converter for Capacitive Actuator," in *Proc. European Power Electronics Conference (EPE)*, pp. 1–10, 3–6th Sept. 2013.
- [34] Furukawa webpag. (2015, July 24). Triple insulated wire: Standard type TEX-E. Furukawa Electric, Tokyo, Japan. [Online]. Available: http://www.furukawa.co.jp/makisen/eng/product/texe_series.htm.
- [35] P. Thummala, "Switch-mode high voltage drivers for dielectric electro active polymer (DEAP) incremental actuators," Ph.D. dissertation, Dept. Electrical Eng., Technical University of Denmark, Kongens Lyngby, Denmark, 2014.
- [36] E. Bennett and S. C. Larson, "Effective resistance to alternating currents of multilayer windings," in *Electrical Engineering*, vol. 59, no. 12, pp. 1010–1016, Dec. 1940.
- [37] Voltech webpage. (2015, Sept. 7), Hi-pot AC Test (HPAC). Voltech Instruments, USA. [Online]. Available: [http://www.voltech.com/Articles/104-162/006/6_5_Hi_pot_AC_Test_\(HPAC\)](http://www.voltech.com/Articles/104-162/006/6_5_Hi_pot_AC_Test_(HPAC)).



Prasanth Thummala (S'11–M'15) was born in Andhra Pradesh, India in 1987. He received the B.Tech. degree in Electrical and Electronics Engineering from Acharya Nagarjuna University, Guntur, India, in 2008, the M.Tech degree in Control Systems engineering from the Department of Electrical Engineering, Indian Institute of Technology Kharagpur, Kharagpur, India, in 2010, and the Ph.D. degree in Power Electronics from the Department of Electrical Engineering, Technical University of Denmark (DTU), Kongens Lyngby, Denmark, in 2015.

Currently, he is a Postdoctoral Research Fellow at the Department of Electrical and Computer Engineering, National University of Singapore. He was a Visiting Ph.D. Student with Colorado Power Electronics Center, University of Colorado Boulder, Boulder, CO, USA, from September 2013 to January 2014.

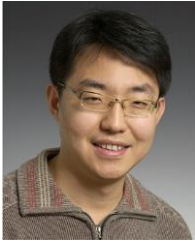
His research interests include dc-dc converters, modelling and control of power electronic converters, high-voltage switch-mode power converters for driving capacitive loads, magnetic design, and digital control. Dr. Thummala received the Best Student Paper Award at the IEEE ECCE USA Conference, Denver, CO, USA, in 2013.



Henrik Schneider (S'11–M'15) was born in Denmark. He received both the Master's degree and Ph.D. degree in Electrical Engineering from Technical University of Denmark, Kongens Lyngby, Denmark, in 2009 and 2015, respectively.

Currently, he is a Postdoc in the Department of Electrical Engineering, Technical University of Denmark. He was an R&D Engineer within power electronics. His research interests include efficiency and power density optimization of power electronics, audio system integration, magnetic design, and finite-element modelling.

Dr. Schneider received the Best Paper Award at the IEEE ECCE Asia Conference, Melbourne, Australia, in 2013, and the Best Presentation Award at the IEEE APEC Conference, Dallas, USA, 2014.



Zhe Zhang (S'07–M'11) received the B.Sc. and M.Sc. degrees in power electronics from Yanshan University, Qinhuangdao, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2010.

He is currently an Associate Professor at the Department of Electrical Engineering, Technical University of Denmark. From 2005 to 2007, he was an Assistant Professor with Yanshan University. From June 2010 to August 2010, he was with the University of California, Irvine, CA, USA, as a Visiting Scholar. He was a Postdoctoral Researcher and an Assistant Professor at the Technical University of Denmark between 2011 and 2014. He has authored or co-authored more than 70 transactions and conference papers.

His current research interests include dc/dc converters, multiple-input converters, and multilevel inverters for renewable energy systems, hybrid electric vehicles, and uninterruptible power supplies.



Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively.

He is currently a Professor in power electronics and the Head of the Electronics Group, Technical University of Denmark. Since 2009 he has been the Deputy Head of the Department of Electrical Engineering, Technical University of Denmark.

His research areas include switch mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers. He has authored and co-authored more than 280 publications.

Dr. Andersen received the best poster prize in UPEC 1991 Conference. From 2010, he has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.