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Investigation on Common Mode Voltage Suppression in Smart Transformer-fed Distributed Hybrid Grids

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***Abstract*— High frequency (HF) switching and AC side unbalanced loads challenge Smart Transformer (ST)-fed hybrid grids (both AC and DC), causing common-mode (CM) voltage variations and DC Link oscillation. The HF switching introduces a HF CM voltage and the AC grid unbalanced loads introduce a fundamental frequency CM voltage in hybrid grids. The CM voltage in ST-fed distributed grids degrades the power quality, threatens the safety of the connected devices, and potentially constitutes a health risk for the operators of such devices. Therefore, this paper systematically analyzes the root causes of the ST CM voltage variations and the impacts on hybrid grids. Based on the two typical configurations (three- and four-leg converters), the performance and requirements of CM inductor filter and bypass CM filter on HF CM voltage suppression are studied in detail. By considering the CM voltage suppression and DC capacitor lifetime, a four-leg converter with improved modulation strategy and small DC bypass film capacitor is proposed. The simulation and experimental results clearly verify the feasibility and correctness of the proposed strategies.**

***Index Terms*— Common mode voltage, smart transformer, three-phase four-leg converter, three-phase four-wire system, unbalanced three-phase loads**

I. Introduction

With the development of distributed generators (DGs) and electric vehicle charging stations, the hybrid grids are attracting increasing attention. The Smart Transformer (ST), as shown in Fig. 1, where the medium voltage (MV) DC bus can be used for fast charging station, large wind and PV, the low voltage (LV) DC link integrates the storage system, and both LV AC and DC grid can integrate distributed generators and charging station, is a candidate to enable the hybrid grids while offering ancillary services to AC grids [1]–[6].

However, due to the absence of the delta-wye transformer in AC side, the common-mode (CM) component may exist in both voltage and current, which, in LV AC and DC grids, may significantly degrade the power quality. Moreover, the CM problem potentially affects the safety of EMC-sensitive devices and humans.

The issues of CM have been widely investigated in motor drives and PV systems, improving lifetime and safety. For the hybrid grids, only two-wire single-phase and three-wire three-phase AC grid CM voltage suppression methods were proposed in [7], [8]. Due to absence of neutral line offered by the converter, the impacts from the neutral line current on the CM voltage is not considered. Moreover, only phase-to-phase voltage exists, which means that the voltage quality is not degraded by the CM component and only the parasitic capacitor enables the CM current circulation. Instead, for the ST-fed distribution grid (three-phase four-wire system), the CM may exist between three-phase and neutral line and in turn the CM current can flow directly through the loads, making the CM issue even more serious.

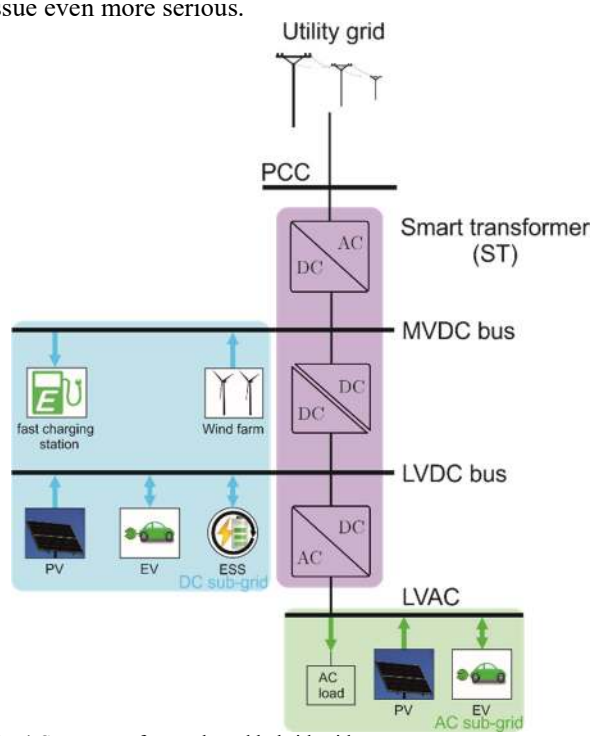


Fig. 1 Smart transformer-based hybrid grids

Additionally, in aforementioned applications, the power converters are current controlled, but the ST low voltage side converter (LVSC) is voltage controlled. In these two cases, the mechanism of high frequency (HF) CM voltage is similar, caused by the switching of the power converter, but the low frequency CM voltage is different. In the voltage controlled case, although the PCC voltage is controlled balanced, the unbalanced load results in fundamental frequency (FF) CM voltage in the DC grid, which has been not researched for four-leg converter so far, based on the current literature.

On the other hand, the impacts of the neutral line current on DC side capacitor does not exist in two-wire and three-wire system anymore [7], [8], due to lack of neutral line. In a four-wire system, the neutral line current may flow into the DC capacitor and therefore the lifetime of the electrolytic capacitor is significantly degraded [9].

Generally, the CM component suppression strategies are based on the converter architecture [10]–[12], modulation strategy [13], [14], and CM filter [15], [16]. An effective strategy to suppress the CM voltage should combine all

aforementioned factors. Regarding the four-wire architecture for the LV AC grid, where the converter is voltage controlled, so far, there is still no standard for LVSC structure with extra neutral line. Instead, UPS system with three or four wires already represent an industry standard. The midpoint of the DC link [17]–[19], the wye connection point of the AC side filter capacitors [13], and connection of the DC-link capacitor midpoint and wye point of AC filter capacitors [20], [21], were proposed to be used as neutral line for three-leg converter. The neutral line can also be supplied by an additional leg [13], [22].

The goal of this paper is to analyze the CM of the three- and four-leg converters, constituting 3-phase 4-wire system. Only a few papers discussed the CM problem in UPS system [13], [22] and in TT (Terra-Terra) LV grid [22], but the CM suppression in hybrid grids and effects from AC grid unbalnaced loads are still not yet considered.

A passive CM filter can be composed of a CM inductor [23], [24], AC side bypass LRC filter [7], [20], [25] and DC-side bypass filter [26]. For the CM inductor filter, when the converter is voltage control, the voltage quality is determined by the CM current, and consequently, in three-leg converter four-wire system, the filter is non influential when the AC grid is no loads or with light loads, as it will be explained in the following. Since the bypass CM filter can avoid the aforementioned drawback, it is used for CM suppression in the hybrid grids in this paper. However, as the bypass filter is mainly used in single-phase [26] and three-phase three-wire system [21] [24] so far, the impacts from the unbalanced AC loads on the filter performances have not been studied. The mechanism and attenuation of the fundamental CM voltage caused by unbalanced AC loads are never considered.

The individual requirements on the bypass filter in three- and four-leg converters for HF CM suppression are investigated. The mechanism of the FF CM voltage caused by unbalanced AC loads is studied in detail and then an improved modulation strategy is proposed to attenuate the FF CM voltage for the four-leg converter.

This paper is organized as follows. The effects of conventional AC side LC filter on CM components as well as the effects of unbalanced loads on PCC voltage are studied in detail in Section II. Considering the unbalanced AC loads, the parameters requirement of the bypass CM filter in three- and four-leg converters are studied, and the improved modulation is proposed to attenuate FF CM voltage in Section III. The simulation and experimental results are shown in Section IV and V, respectively. Section VI concludes this paper.

II. THREE-PHASE FOUR-WIRE LVSC

The topology of three-stage solid-state transformer-based ST is shown in Fig. 1. The MV side converter works as the conventional active front-end rectifier to control MV DC bus voltage as well as MV grid current. The DC/DC converter with a medium or HF transformer isolates MV and LV DC buses and controls LV DC grid voltage. The ST LVSC is controlled as a voltage source to form the grid voltage. In order to substitute the conventional distribution transformer in a TT (Terra-Terra, doubly grounded) distribution, three lines and a neutral conductor must be distributed.

A Design of Neutral point

According to applications of UPS, two typical configurations of three-phase four-wire LVSC are shown in Fig. 2. In three-leg ST, midpoint of DC-link capacitors is used as the neutral line, as shown in Fig. 2(a), and in four-leg ST the forth-leg is used to offer neutral line as shown in Fig. 2(b). They both have small fundamental impedance in neutral line and therefore are possible to be used for distribution grid.

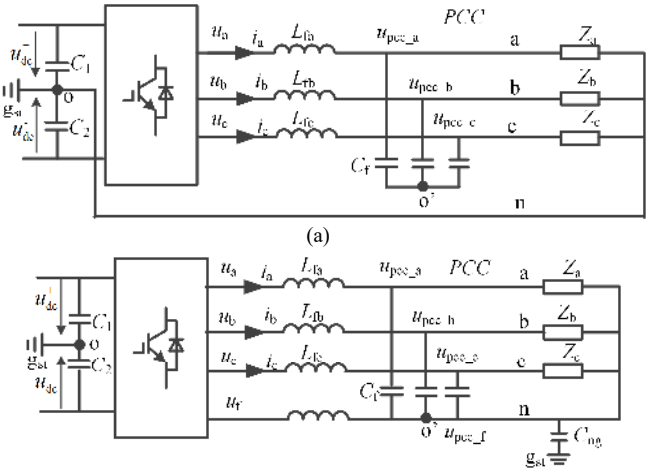


Fig. 2 LVSC topology with neutral line in (a) three- and (b) four-leg ST

B CM and DM characteristic of ST-fed grids

In order to simplify the analysis, two-level converters are considered. When the midpoint of DC-link capacitor is regarded as the reference, the voltage can be split into CM and DM component, and can be expressed by the switching function as,

$$u_{\mathrm{cm}} = \frac{s_{\mathrm{i}} + s_{\mathrm{j}} + s_{\mathrm{k}} + s_{\mathrm{f}}}{n} \frac{u_{\mathrm{dc}}}{2} \tag{1}$$

$$u_{\mathrm{dm\_i}} = \frac{2}{3}\left(s_{\mathrm{i}} - \frac{s_{\mathrm{j}} + s_{\mathrm{k}} + s_{\mathrm{f}}}{n-1} \right) \frac{u_{\mathrm{dc}}}{2} \tag{2}$$

where i, j k and f represent the phase-a, -b, -c and fourth-leg, respectively, and i≠j≠k≠f. s is the switching function, when s=1, the upper switch is on, and when s=-1, the lower switch is on in each leg. n is the number of converter leg (n=3 or 4). Subscripts "cm" and "dm" represent the CM and DM voltage, respectively.

The equivalent circuit of three- and four-leg ST is shown in Fig. 3, where C_{ng} is the parasitic capacitor. The red line represents the CM current loop. It clearly shows that in three-leg ST, the CM components flow through loads directly even without stray capacitor as shown in Fig. 3 (a). The grid voltage quality is seriously deteriorated during light load condition, which is a common occurrence in distribution grid. Therefore, the CM inductor filter cannot be used in three-leg ST system. Additionally, the neutral line current during load unbalanced conditions will flow into the DC capacitor and as a consequence the lifetime of the DC capacitor will be significantly degraded [9] and it will be discussed in Section III.

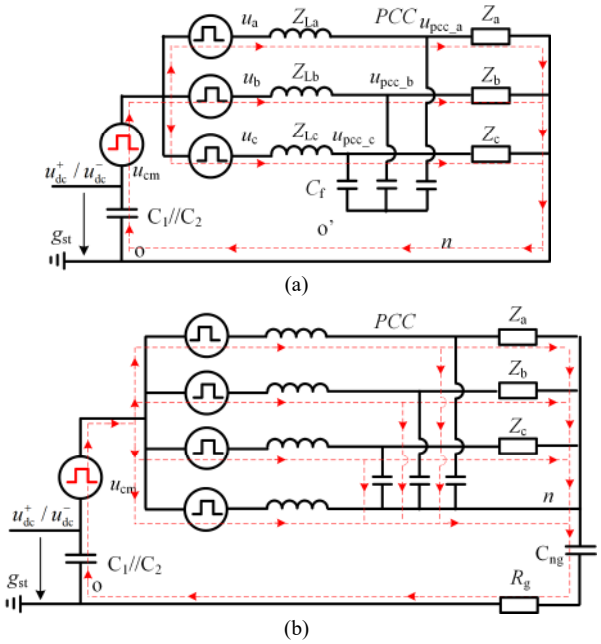


Fig. 3 HF CM and DM equivalent circuit for (a) three-leg ST (b) four-leg ST

Conversely, in four-leg ST, the CM component is similar to the PV and motor driving: a stray capacitor C_{ng} closes the current loop, as shown in Fig. 3(b). The single-phase voltage is the phase-to-neutral DM voltage, which can be filtered by the conventional LC filter, and therefore has high quality compared to that in three-leg ST. Therefore, four-leg ST is a better candidate.

In order to simplify the expression of Taylor's series, the CM and DM voltage in (1) and (2) can be expressed in terms of FF component, low and HF component.

$$\begin{cases} u_{cm} = u_{cm\_f} + u_{cm\_low} + u_{cm\_hig} \\ u_{dm\_j} = u_{dm\_j\_f} + u_{dm\_j\_low} + u_{dm\_j\_hig} \end{cases} \tag{3}$$

where subscripts "f", "low" and "hig" represent the FF, low frequency and HF components, respectively.

The low frequency component is determined mainly by the reference voltage and modulation, which is equal to zero by the SPWM. Thanks to the LC filter, the phase-to-neutral voltage can be obtained as,

$$u_{PCC} = u_{dm\_f} + u_{dm\_low} \tag{4}$$

The PCC to neutral voltage quality can be improved by tuning the parameter of the conventional LC filter.

If the stray capacitor is neglected, due to the absence of a closed current loop for CM voltage, at each point of the AC grid, the CM voltages are equal. Thus, the voltage between the neutral point to ground is equal to

$$u_{ng} = u_{cm} \tag{5}$$

Additionally, the negative and positive DC buses to neutral line both have the similar CM voltage as (5). The CM voltage affects the load when the parasitic capacitor is non-negligible, such as PV panel connecting to the ST [27].

C. Effects of three-phase unbalanced loads on FF CM voltage.

Unlike the HF CM voltage, which is affected by the HF switching of the power converter as shown in (1), the FF CM voltage is affected by the control strategy and load conditions. Assumed that the leg output voltage only includes positive sequence component and paralleled DC capacitor impedance is negligible as shown in Fig. 3(a), it can be obtained that,

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} U_m^+ \angle 0 \\ U_m^+ \angle -\frac{2}{3}\pi \\ U_m^+ \angle \frac{2}{3}\pi \end{bmatrix} \tag{6}$$

Since only the FF component is considered in this case, the impacts of filter capacitor can be neglected, due to high impedance at FF. The filter inductance and load impedance are assumed as,

$$\begin{bmatrix} Z_{La} \\ Z_{Lb} \\ Z_{Lc} \end{bmatrix} = \begin{bmatrix} Z_1 \angle \theta_1 \\ Z_1 \angle \theta_1 \\ Z_1 \angle \theta_1 \end{bmatrix}, \begin{bmatrix} Z_a \\ Z_b \\ Z_c \end{bmatrix} = \begin{bmatrix} pZ_m \angle \theta \\ Z_m \angle \theta \\ Z_m \angle \theta \end{bmatrix}, 0 \le p < 1 \tag{7}$$

The voltage drop across the filter inductance can be expressed as,

$$\begin{bmatrix} u_{La} \\ u_{Lb} \\ u_{Lc} \end{bmatrix} = \frac{U_m^+ Z_1 \angle \theta}{Z_1 \angle \theta_1 + Z_m \angle \theta} \frac{1}{3} \left(\underbrace{\begin{bmatrix} (2+m)\angle 0 \\ (2+m)\angle -\frac{2}{3}\pi \\ (m-1)\angle \frac{2}{3}\pi \end{bmatrix}}_{u_L^+} + \underbrace{\begin{bmatrix} (m-1)\angle 0 \\ (m-1)\angle \frac{2}{3}\pi \\ (m-1)\angle -\frac{2}{3}\pi \end{bmatrix}}_{u_L^-} + \underbrace{\begin{bmatrix} (m-1)\angle 0 \\ (m-1)\angle 0 \\ (m-1)\angle 0 \end{bmatrix}}_{u_L^0} \right) \tag{8}$$

$$m = \frac{Z_1 \angle \theta}{Z_1 \angle \theta_1 + pZ_m \angle \theta}$$

Thus, the PCC to neutral voltage is equal to

$$\begin{bmatrix} u_{pcc\_a} \\ u_{pcc\_b} \\ u_{pcc\_c} \end{bmatrix} = \begin{bmatrix} u_{c\_a}^+ \\ u_{c\_b}^+ \\ u_{c\_c}^+ \end{bmatrix} - \begin{bmatrix} u_{La}^+ \\ u_{Lb}^+ \\ u_{Lc}^+ \end{bmatrix} - \begin{bmatrix} u_{La}^- \\ u_{Lb}^- \\ u_{Lc}^- \end{bmatrix} - \begin{bmatrix} u_{La}^0 \\ u_{Lb}^0 \\ u_{Lc}^0 \end{bmatrix} \tag{9}$$

It clearly shows that the unbalanced loads lead to PCC voltage including positive, negative and zero sequence (CM) voltage, respectively, if only positive sequence voltage is controlled at the leg voltage.

III High and Fundamental Frequency CM Voltage Suppression in Four-leg ST

As analyzed above, the high frequency CM component exists in ST-fed hybrid grids, and AC unbalanced load leads to FF CM voltage. Effective strategies for CM voltage suppression are proposed as follows.

A High frequency CM suppression

The high frequency CM equivalent circuit with bypass CM filter is shown in Fig. 4, where the HF CM components in DC and AC grid do not exist anymore. However, compared to Fig. 2(b), when three-phase loads are unbalanced, there are two possible options for the neutral line current to flow back converter, i.e., fourth-leg or DC capacitor, which is mainly determined by the line impedance.

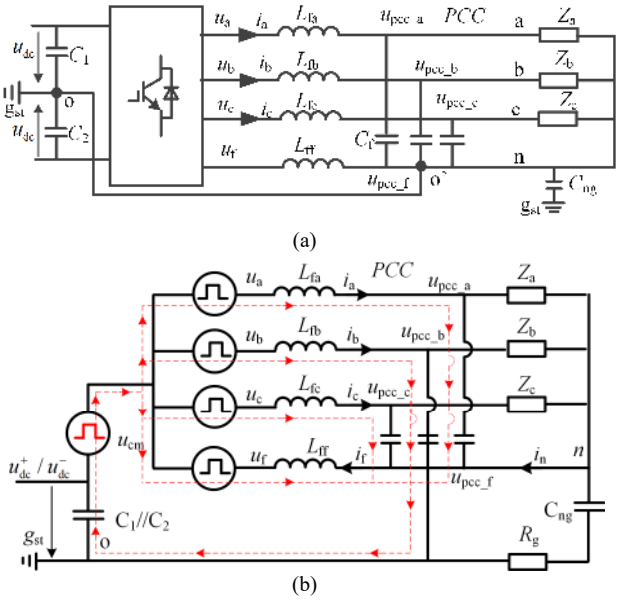


Fig. 4 High frequency CM suppression for four-leg ST with bypass CM filter (a) topology and (b) equivalent circuit.

The impedance of the fourth-leg inductor and the DC parallel capacitor is shown in Fig. 5. If the DC capacitance is 2200μF and the inductance is 1.6mH, the impedances of the capacitor and inductance at 50Hz are similar, which leads to neutral line current flowing into the midpoint of DC capacitors and the similar problem in capacitor lifetime as the three-leg ST.

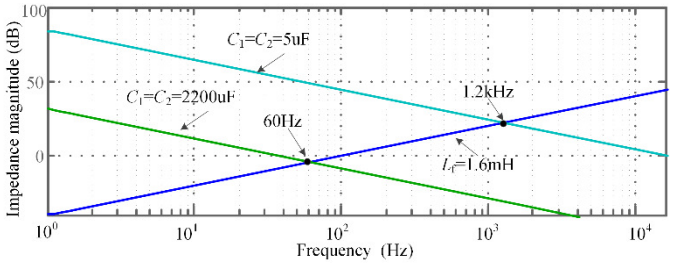


Fig. 5 Comparison of filter inductor and DC capacitor impedance

As shown in Fig. 5, if a film capacitor, 5μF, is used, instead of the electrolytic capacitors, the large impedance at low frequency can ensure the neutral line current only flows back to fourth-leg to mitigate lifetime degradation of the DC capacitor and the low impedance at high frequency can effectively suppress the high frequency CM voltage at PCC. In contrast, the three-leg ST cannot use the small bypass capacitors in DC link, because this small capacitor has large FF impedance, hindering neutral line current flowing back to neutral point and thus leading to load neutral potential deviation, which potentially results in single-phase device overvoltage.

B. Improved modulation to reduce FF CM voltage.

The FF CM (9) in AC grid is easily to be suppressed by adding a zero sequence voltage control loop to the positive and negative sequence voltage control loop. However, as shown in Fig. 4(b), the fourth-leg voltage at PCC, caused by neutral line current and voltage control strategy, will act on the DC capacitor, leading to the DC grid voltage oscillation.

In this case, the high frequency characteristic can also be neglected, and only FF component is considered. According to the Kirchhoff voltage law, closed-loop voltage equations in Fig. 4(b) can be expressed as,

$$\begin{cases} u_{\mathrm{a}} - L_{\mathrm{fa}}\, di_{\mathrm{a}}/dt - Z_{\mathrm{a}} i_{\mathrm{a}} = u_{\mathrm{pcc\_f}} \\ u_{\mathrm{b}} - L_{\mathrm{fb}}\, di_{\mathrm{b}}/dt - Z_{\mathrm{b}} i_{\mathrm{b}} = u_{\mathrm{pcc\_f}} \\ u_{\mathrm{c}} - L_{\mathrm{fc}}\, di_{\mathrm{c}}/dt - Z_{\mathrm{c}} i_{\mathrm{c}} = u_{\mathrm{pcc\_f}} \end{cases} \tag{10}$$

When phase-to-neutral voltage at PCC is controlled to be balanced, the voltage drop on the loads are balanced and their sum is equal to zero. Additionally, during unbalanced load conditions, the sum of three-phase current is equal to the neutral line current.

$$\begin{cases} u_{\mathrm{pcc\_a}} + u_{\mathrm{pcc\_b}} + u_{\mathrm{pcc\_c}} = 0 \\ i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}} = i_{\mathrm{f}} \end{cases} \tag{11}$$

where $\begin{cases} Z_{\mathrm{a}} i_{\mathrm{a}} = u_{\mathrm{pcc\_a}} \\ Z_{\mathrm{b}} i_{\mathrm{b}} = u_{\mathrm{pcc\_b}} \\ Z_{\mathrm{c}} i_{\mathrm{c}} = u_{\mathrm{pcc\_c}} \end{cases}$.

By adding three equations in (10) and then substituting (11) into it, it can be obtained that,

$$u_{\mathrm{pcc\_f}} = \frac{u_{\mathrm{a}} + u_{\mathrm{b}} + u_{\mathrm{c}}}{3} - \frac{L_{\mathrm{ff}}}{3}\frac{d}{dt} i_{\mathrm{f}} \tag{12}$$

The fourth-leg voltage equation can also be expressed as,

$$u_{\mathrm{pcc\_f}} = u_{\mathrm{f}} + L_{\mathrm{ff}}\frac{d}{dt} i_{\mathrm{f}} \tag{13}$$

By substituting (13) into (12), it derives that,

$$u_{\mathrm{f}} = \frac{u_{\mathrm{a}} + u_{\mathrm{b}} + u_{\mathrm{c}}}{3} - \frac{4}{3} L_{\mathrm{ff}}\frac{d}{dt} i_{\mathrm{f}} \tag{14}$$

The voltage in (12) acts on the DC capacitor and fourth-leg inductor, as shown in Fig. 4(b). With balanced loads, (12) is equal to zero and DC bus voltage will be smooth, while with unbalanced loads the DC bus voltage includes FF oscillations. If the modulated voltage of the fourth-leg includes an opposite term as shown in (15), (13) can be expressed as (16). Consequently, the DC bus voltage oscillation is reduced.

$$u_{\mathrm{f\_1}} = -\frac{u_{\mathrm{a}} + u_{\mathrm{b}} + u_{\mathrm{c}}}{3} \tag{15}$$

$$u_{\mathrm{pcc\_f}} = -\frac{L_{\mathrm{ff}}}{3}\frac{d}{dt} i_{\mathrm{f}} \tag{16}$$

It depicts that the DC capacitor voltage oscillation caused by can be further reduced by reducing the forth-leg filter inductance. Based on (15) and the carrier wave based modulation, the overall modulation block diagram is shown in Fig. 6.

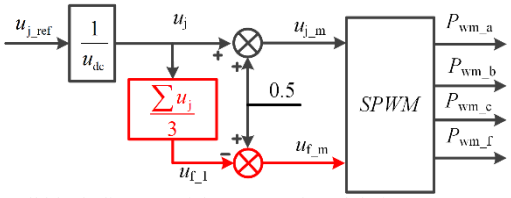


Fig. 6 Overall block diagram of the proposed modulation

The improved modulation strategy can reduce the FF CM voltage in DC link to not only improve the power quality but also increase the reliability of the DC capacitor which will be discussed as follows.

C. Reliability comparison

As analyzed above, in Fig. 4(b), the neutral line current flows into the DC capacitors, leading to not only DC voltage oscillation but also the DC capacitor lifetime reductions. In order to estimate the lifetime reduction caused by the neutral line current, the DC capacitor lifetime model is given in (17) [28].

$$L = L_0 \left(\frac{V}{V_0}\right)^{-n} 2^{\left(\frac{T_{h0}-T_a}{10}\right)} 2^{\left(\frac{-\Delta T_h}{10}\right)} \tag{17}$$

where L_0 is the based lifetime given by the manufacturer, V_0 and T_{h0} are the voltage and hotspot temperature at testing condition, respectively, V, T_a and ΔT_h are the operating voltage, ambient temperature and the temperature rise caused by neutral line current, respectively. The exponent n is from around 7 to 9.4 for metallized polypropylene film capacitors and from 3 to 5 for aluminum electrolytic capacitors.

For a serial connection of the DC capacitors, the temperature rise in each capacitor caused by the neutral line current can be expressed as,

$$\Delta T_h = \frac{1}{4} I_n^2 R_{ESR} R_{th} \tag{18}$$

where I_n is the neutral line current and R_{ESR} is the equivalent serial resistance at 50 Hz, R_{th} is the thermal resistance.

Based on the laboratory test, for a 4500μF 500V electrolytic capacitor, R_{th} is 2.9K/w, R_{ESR} is 22.8mOhm at 50Hz. By substituting that two values and (18) into (17), since only the effects of neutral-line current is considered, the other factors can be regarded as a constant, C, (17) can be re-expressed as,

$$L = L_0 C 2^{\left(-\frac{0.0661 I_n^2}{4}\right)} \tag{19}$$

The last term on the right hand side of (19) clearly indicates the effects from the neutral line current. In order to compare fairly, the same conditions are adopted, i.e., two 4500μF capacitors and two 5μF capacitors connecting in series, respectively. For the 4500μF capacitor, its relative lifetime versus the neutral line current is clearly shown in Fig. 7. Therefore, the neutral line current must be limited, which can be achieved by replacing the electrolytic capacitor with a film capacitor. Such as a 5μF film capacitor can block the neutral line current flowing into the mid-point of capacitor and in turn the lifetime of the DC capacitor is nearly regardless with the neutral line current.

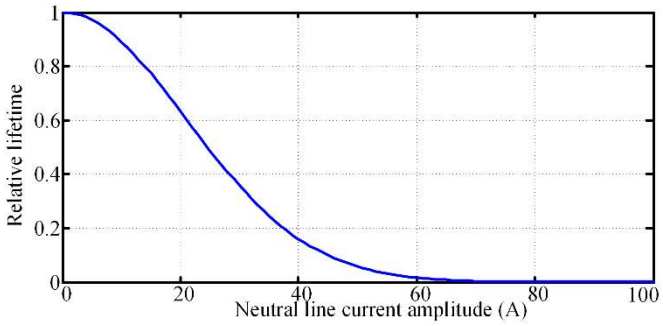


Fig. 7 Relative lifetime of the capacitor versus neutral line current

Besides the effects from the neutral line current, according to the manufacture datasheet, the DC link voltage periodic oscillation also has significantly impacts on the capacitor lifetime as shown in (17). By considering the DC link voltage ripples, the working voltage can be equivalent as [29],

$$V = V_{dc} + \frac{V_{ripp}}{2} \tag{20}$$

where V_{dc} is the continuous voltage, V_{ripp} is the peak to peak value of ripple voltage.

Since the proposed CM voltage suppression, based on four-leg ST with improved modulation strategy and small film capacitor (several μF) in DC link of the bypass filter, can not only limit the neutral line current, but also reduce the capacitor voltage ripple. Thus, the proposed strategy can significantly increase the reliability of the DC capacitors.

VI Simulation Results

In order to validate the theoretical analyses, the simulation was carried out in Matlab/Plecs. The simulation parameters are summarized in Table I.

Table I
Simulation Parameters

Parameters	Symbols	Values
AC voltage (V)	U_g	400
DC voltage (V)	U_{dc}	800
Switching frequency (kHz)	f_s	10
DC Electrolytic Capacitor (F)	C_{dc1}, C_{dc2}	1200e-6
DC Electrolytic Capacitor (F)	C_{dc1}, C_{dc2}	5e-6
AC DM inductance (H)	L_{dm}	1.6e-3
AC CM inductance (H)	L_{cm}	5.5e-3
AC filter capacitance (F)	C_f	5e-6
Load inductance (mH)	L_g	0.02e-3
Load resistance (Ohm)	R_g	5

A. Performances with the CM inductor filter

The simulation results of three- and four-leg ST phase-to-neutral voltages at PCC with 5.5mH CM inductor filter are shown in Fig. 8 and Fig. 9, respectively. The hardware circuits are similar to Fig. 2(a) and (b), respectively.

In Fig. 8, it clearly shows the PCC CM voltage is significantly affected by the loads. When load resistance is 5 Ohm and corresponding load current is 64A, the PCC to neutral voltage includes a smaller CM voltage, about 50V, as shown in Fig. 8(a). In contrast, during no load condition, the PCC voltage are seriously distorted and the CM voltage is from -400V to 400V as shown in Fig. 8(b).

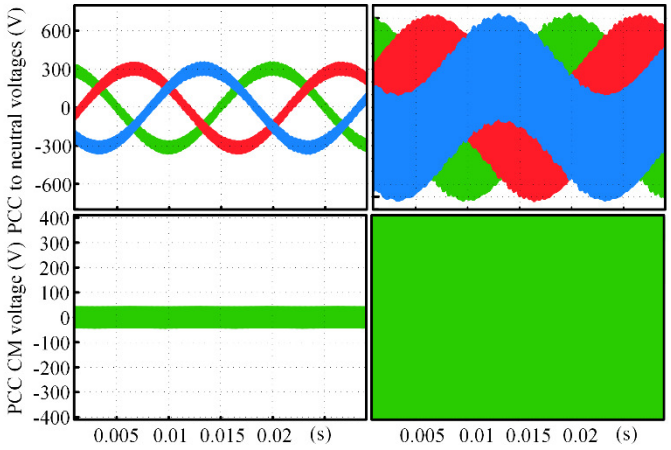


Fig. 8 Simulation results of PCC to neutral voltage of three-leg ST with CM inductor filter (L_{cm}=5.5e-3H) (a) R=5Ohm and (b) no loads.

For the four-leg ST, the PCC to neutral voltage quality is improved and do not effect by the loads any more. However, the PCC to ground and DC bus to neutral line CM voltage are both existed as shown in Fig. 9.

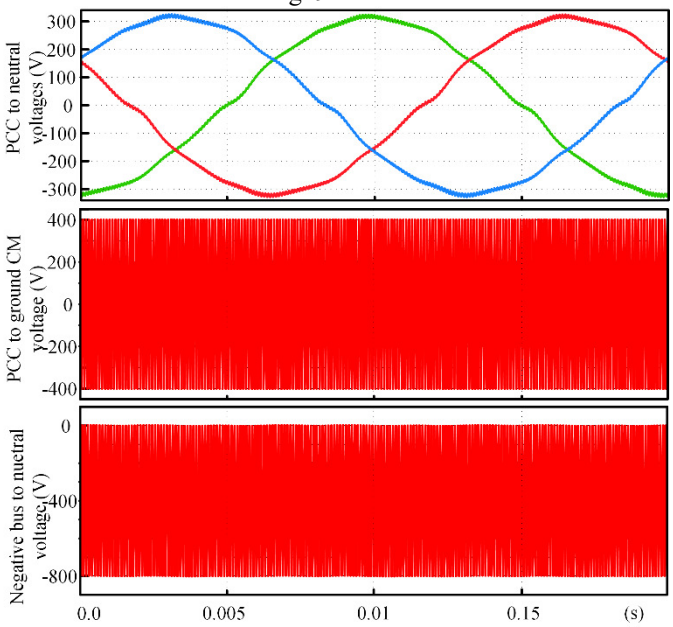


Fig. 9 Simulation results of four-leg ST with CM inductor filter connected 5Ohm resistive loads.

B. Performances of bypass CM filter

With the bypass CM filter, the three-leg ST CM voltage in phase-to-neutral voltage at PCC is regardless with the load currents and has high quality as shown in Fig. 10. However, during unbalanced grid loads conditions, the neutral line current flows into the DC capacitor directly, leading to DC grid voltage oscillation, harmful for DC capacitor.

The simulation results of phase-to-neutral voltage and current of four-leg ST are shown in Fig. 11. When three-phase loads are all 5Ohm, the current and voltage are both balanced and sinusoidal, as shown in Fig. 11(a). When the three-phase load resistances are 3, 5 and 5 Ohm, respectively, the simulation results are shown in Fig. 11(b), where the PCC voltages are controlled well, balanced and sinusoidal.

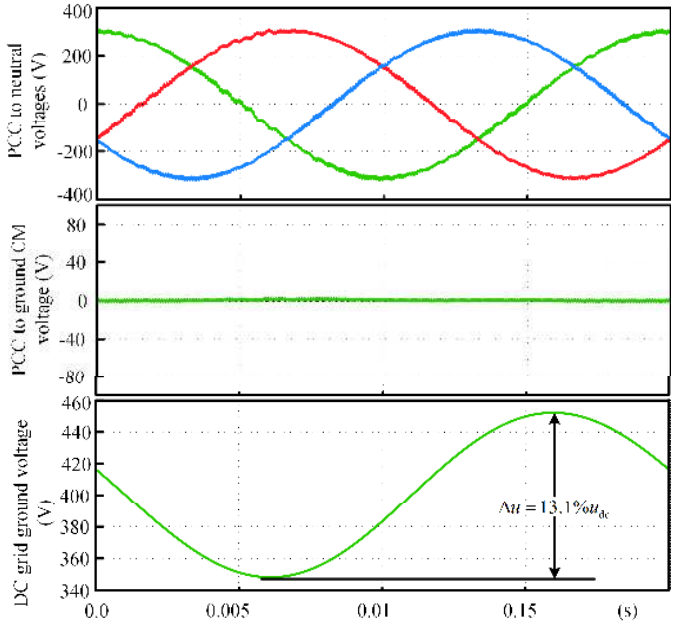


Fig. 10 Simulation results of three-leg ST with bypass filter(C_{dc1}=C_{dc2}=1200e-6μF)

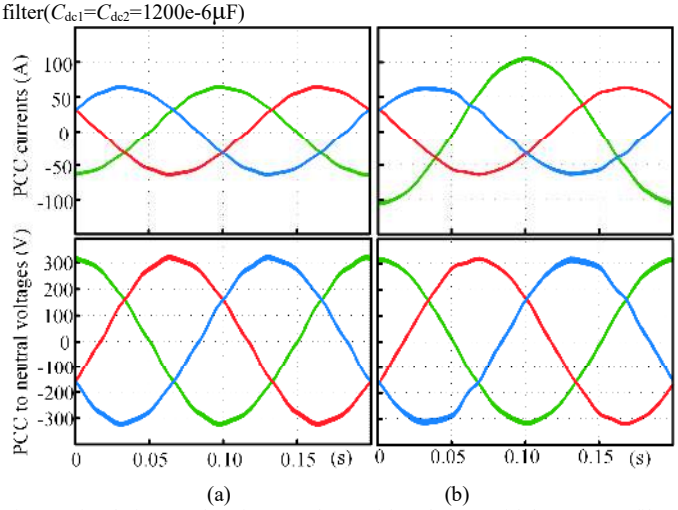
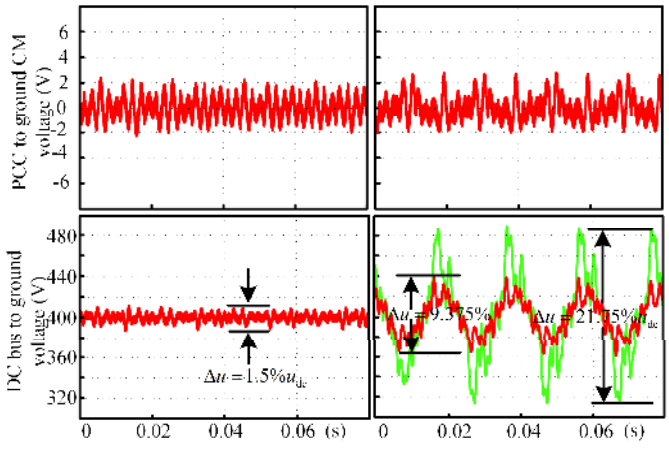


Fig. 11 Simulation results of PCC voltage of four-leg ST with bypass CM filter under (a) balanced loads (b) unbalanced loads (i_a=i_b=64A, i_c=106A) (C_{dc1}=C_{dc2}=5e-6μF)

The corresponding AC and DC side CM voltage under balanced and unbalanced load conditions are shown in Fig. 12. In both conditions, the AC CM voltages are effectively suppressed and are smaller than 6V (peak-peak value). However, during unbalanced load conditions, with conventional modulation strategy, the DC bus oscillation is 21.75% of DC link voltage. In contrast, with the proposed modulation strategy, the DC bus oscillation is reduced to 9.375% of the DC link voltage. Therefore, the proposed modulation strategy effectively reduces the DC bus voltage oscillation, as compared to the conventional modulation.

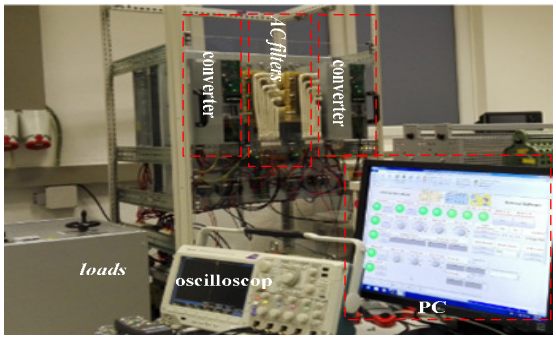


(a) (b)

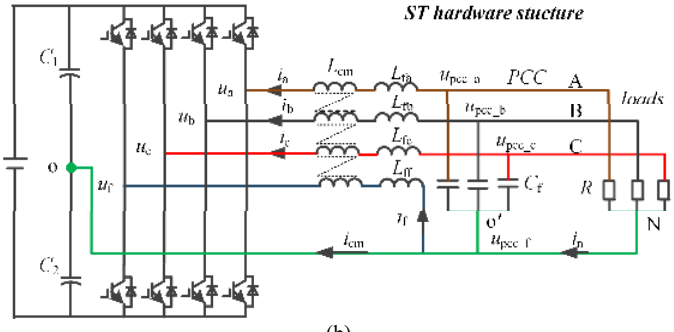
Fig. 12 Simulation results of PCC and positive DC bus to ground CM voltage of four-leg ST under (a) balanced loads (b) unbalanced loads (i_a=i_b=64A, i_c=106A, i_a/i_c=60.4%) (green line is conventional modulation, and red line is the proposed modulation)

V Experimental Results

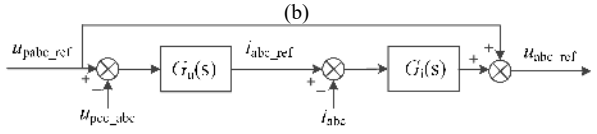
In order to validate the theoretical analysis, a four-leg ST-based setup was built in laboratory and controlled by the dSPACE MicroLABbox. The photograph, system configuration, and control diagram are shown in Fig. 13. The hardware parameters and the control system parameters are listed in TABLE II and TABLE III.



(a)



(b)



(c)

Fig. 13 Experimental setup (a) photograph (b) system structure, and (c) control diagram

TABLE II
EXPERIMENTAL HARDWARE PARAMETERS

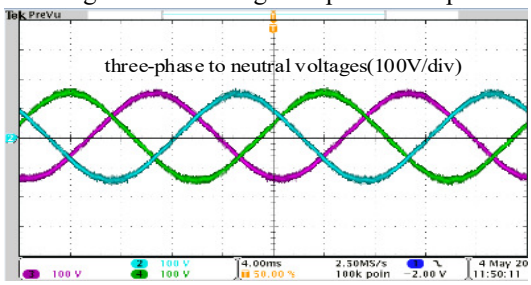
Parameters	Value
DC Voltage (V)	350
Rated Power of Converter (kW)	4
Load resistance (Ohm)	39
CM filter inductance (H)	5.5e-3
AC filter inductance (H)	1.6e-3
AC filter capacitor (F)	5.0e-6

TABLE III
CONTROL PARAMETERS OF THE EXPERIMENT

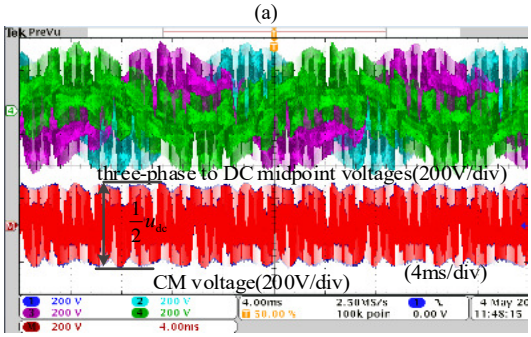
Parameters	Value
Rated AC phase voltage (V)	150
Rated AC voltage frequency (Hz)	50
Switching frequency (kHz)	10
Current loop integrational gain (k_{ii})	150
Current loop proportional gain (k_{ip})	15
Voltage loop integrational gain (k_{ui})	15
Voltage loop proportional gain (k_{up})	0.3
Voltage loop resonant gain (k_{rp})	15

A Four-leg ST AC CM voltage and DC oscillation suppression

Without the proposed CM filter, three-phase to neutral voltage are sinusoidal and thus three-phase to neutral CM voltage is nearly equal to zero as shown in Fig. 14(a). However, as analyzed in Fig. 3 (b), the phase to ground voltage and CM voltage all have high ripples, as shown in Fig. 14(b). Therefore, without the proposed CM filter, these ripple voltages may generate leakage current through the parasitic capacitance.



(a)



(b)

Fig. 14 Experimental results of four-leg ST with CM inductor filter (a) three-phase to neutral voltage, and (b) three-phase and CM voltage of PCC to midpoint of DC capacitor.

In contrast, with the proposed CM filter, the PCC to neutral and to ground voltages are the same, and the CM voltage is only equal to 4.3% of DC-link voltage, during balanced load condition, as shown in Fig. 15(a). When phase-c current is 1.25 times higher than phase-a and -b current amplitude, the AC CM voltage is only 5.4% of DC-link voltage. The experimental results in Fig. 15 clearly validate the theoretical analysis and show that AC side to ground CM voltage under balanced and unbalanced load conditions both can be effectively suppressed.

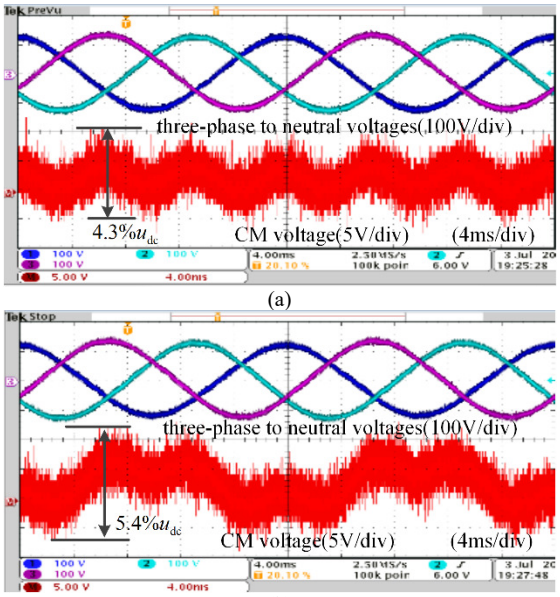


Fig. 15 PCC to neutral and CM voltage with proposed strategy under (a) balanced, and (b) unbalanced load conditions (i_a=i_b=4A, i_c=5A), (C_{dc1}=C_{dc2}=5μF)

In addition to the AC grid CM voltage, the DC grid performances are compared in Fig. 16. Without the proposed CM filter, the negative and positive DC grid to AC neutral line voltages have high CM component, 0.5u_{dc}, as shown in Fig. 16 (a). If the proposed CM filter is adopted, the DC CM voltage amplitude is only 2.85% of the DC link voltage, during balanced load conditions.

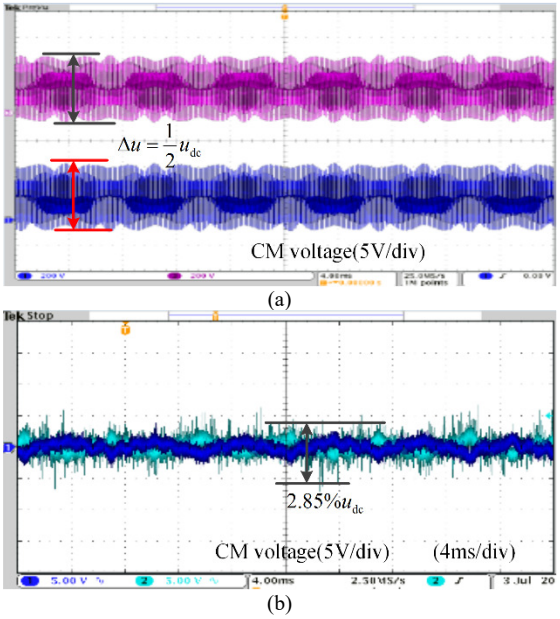


Fig. 16 DC bus to ground voltage (a) during balanced condition without CM filter, (b) during balanced condition with CM filter (i_a=i_b=i_c=4A), (C_{dc1}=C_{dc2}=5μF)

When the load is unbalanced, with the proposed CM filter, the simulation and experimental results of DC link voltage oscillations are compared in Fig. 17, where i_a=i_b=4A, i_c=9A. With the conventional modulation strategy, the DC link voltage oscillation peak-to-peak value is 36V, while with the proposed modulation strategy the DC link voltage oscillation is reduced to 26V, as shown in Fig. 17 (a) and (b), respectively. Similar results are obtained from the simulation results as shown in Fig. 17 (c) and (d), respectively. The simulation and experimental results match well, and furtherly validate the correctness of the theoretical analyses.

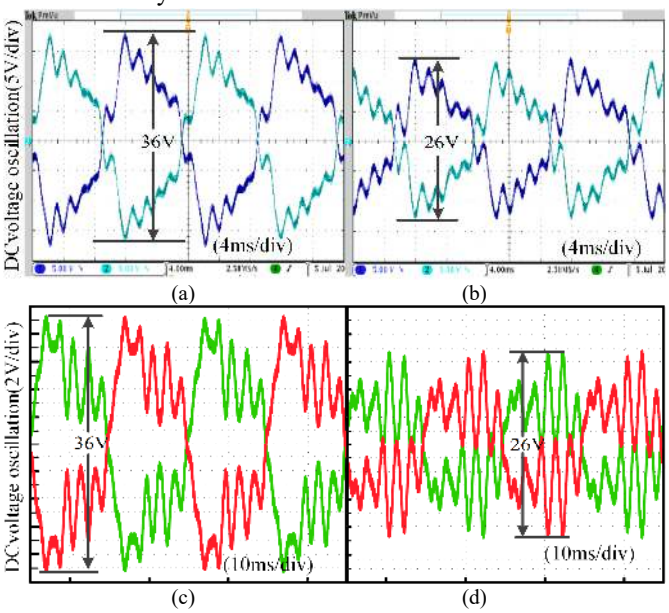


Fig. 17 Comparison of DC voltage oscillation under unbalance load conditions (i_a=i_b=4A, i_c=9A, i_a/i_c=44.4%), (a) (b) are experimental results, (c) (d) are simulation results, (a) (c) with the conventional modulation strategy, (b) (d) with the proposed modulation

B Effects of DC capacitor on fourth-leg current

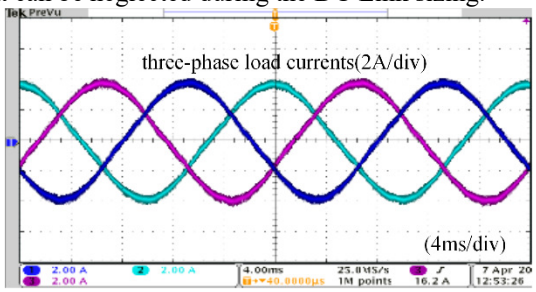
During balanced and unbalanced load conditions, the impacts of DC-link bypass filter capacitor on fourth-leg and DC capacitor midpoint currents are compared in Fig. 18 and Fig. 19, where the capacitances are 2200μF and 5μF, respectively.

The experimental results during balanced load conditions are shown in Fig. 18. Three-phase currents are 4A as shown in Fig. 18(a). Since the load is not completely balanced and the dead time is non-zero, the neutral line current is non-zero in both cases, as shown Fig. 18 (b) and (c). Compared to Fig. 18 (c), the DC capacitor midpoint current includes low frequency oscillation, which indicates that the FF current flows into the DC capacitors, as shown in Fig. 18 (b).

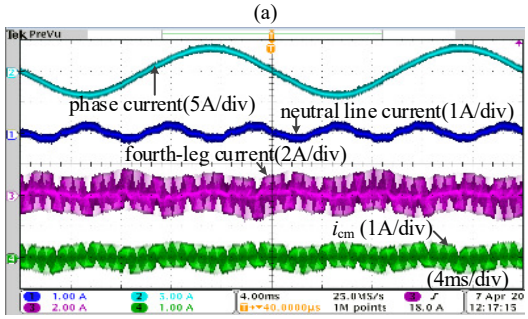
When the load is unbalanced, the three-phase currents, i_a=i_b=4.2A, i_c=3A, are shown in Fig. 19(a), neutral line current, fourth-leg current and DC capacitor midpoint current are shown in Fig. 19(b) and (c). When the DC capacitor is 2200μF, the fourth-leg current is almost unchanged as compared to that in Fig. 18 (b) and the neutral line current almost flows into the midpoint of the DC capacitors, as shown in Fig. 19(b). When the DC capacitor is 5μF, compared to Fig. 18 (c), the DC capacitor midpoint current is similar, and thus the neutral line current flows into the fourth-leg as shown in Fig. 19(c).

These results show how the proposed solution effectively prevents the neutral current to flow into the DC Link capacitors, demonstrating that the lifetime of these is unaffected by the degree of load imbalance. For ST applications, where many services to the AC grids are enabled by the energy stored in the

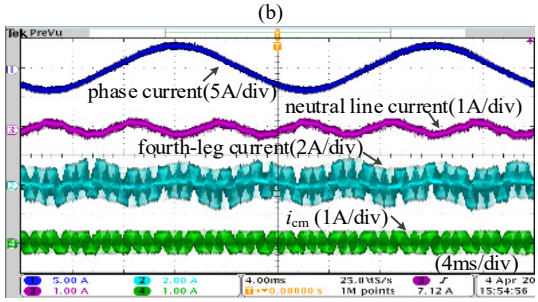
DC Links [6], this means that the magnitude of the neutral current can be neglected during the DC Link sizing.



(a)

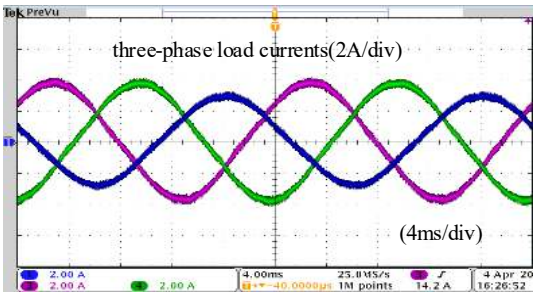


(b)

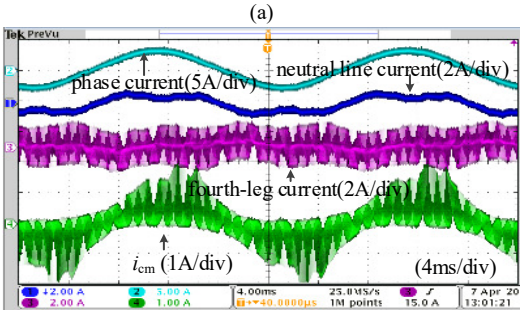


(c)

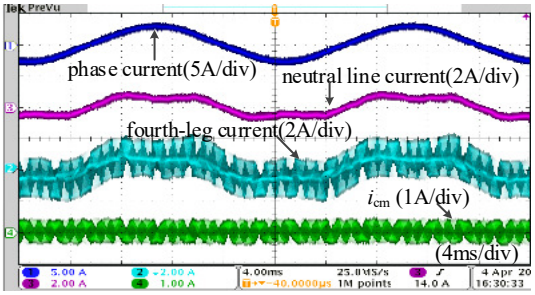
Fig. 18 voltages and currents of four-leg ST during balanced load conditions (a) three-phase current, (b) C_1=C_2=2200μF and (c) C_1=C_2=5μF



(a)



(b)



(c)

Fig. 19 voltages and currents of four-leg ST during unbalanced load conditions (a) three-phase current, (b) C_1=C_2=2200μF and (b), C_1=C_2=5μF

IV CONCLUSIONS

In this paper, CM voltage suppression and DC voltage oscillation reduction are studied for ST-fed hybrid grids. Due to the existence of the neutral line, the three-leg converter with CM inductor cannot effectively suppress CM voltage in AC grid, but the four-leg ST with bypass CM filter can effectively suppress the CM voltage. Based on the CM equivalent circuits, the working mechanism of a bypass CM filter on CM voltage suppression and DC side filter capacitor parameter design based on four-leg ST are studied in detailed. The neutral line current potentially leads to lifetime reduction of the DC electrolytic capacitor because of current path introduced by the bypass filter. Instead, a small film capacitor used to replace the electrolytic capacitor in DC side of bypass filter can significantly avoid the neutral line current flowing into the capacitors and in turn, the lifetime of the capacitor can be preserved. Although the four-leg ST with bypass filter can significantly reduce the high frequency CM voltage in hybrid grids, the FF CM voltage will be introduced during AC unbalanced load conditions. An improved modulation strategy is proposed to reduce the DC grid voltage FF voltage oscillation. The simulation and experimental results clearly validate the concept and the theoretical analysis.

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