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Investigation on the effects of interconnect RC in 3nm technology node using Path-Finding Process Design Kit

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ABSTRACT With the continuous development of front-end-of-line (FEOL) technology, the development of interconnection processes at nanoscale process nodes is becoming important. We conducted a post-layout circuit simulation to consider the effect of parasitic R and C components of middle-of-Line (MOL) and back-end-of-line (BEOL) on the circuit performance. We constructed a process design kit (PDK) for path-finding to analyze the circuit layout in a 3nm technology node based on gate-all-around FET (GAA-FET). It consists of the spice model library that satisfies the 3nm power performance area (PPA) target, and the layout versus schematic (LVS), parasitic extraction (PEX) model that checks whether the layout and schematic match, extracts the RC values in the FEOL MOL and BEOL areas. Subsequently, the effect of the interconnection on complex logic circuits (RO, full adder) was confirmed using PDK. As a result of quantifying the effects of FEOL, MOL, and BEOL on the circuit, circuit degradation due to the RC of MOL and BEOL accounts for more than 60%. Furthermore, we introduced the air spacer process as a way to improve the circuit performance by reducing the C_{MOL} owing to the reduction in the dielectric constant of the spacer. When an air spacer is introduced, based on 9-stages FO1 INV RO with k = 7 at V_{DD} = 0.7V, under iso-speed condition, the active power decreases by 30%, 35% when k is 3.3, 1.65, respectively. Under iso-power condition, frequency increases by 9%, 11% when k is 3.3, 1.65, respectively. And based on full adder with k = 7 at V_{DD} = 0.7V, Under iso-speed conditions, the active power decreases by 47%, 58% when k is 3.3, 1.65, respectively. Under iso-power conditions, the delay decreases by 14%, 20% when k is 3.3, 1.65, respectively. PDP decreases by 22%, 32% when k is 3.3, 1.65, respectively. EDP decreases by 31%, 44% when k is 3.3, 1.65, respectively. In conclusion, in this work, we provide a guide for determining the BEOL load and developing an improved wiring process.

INDEX TERMS Gate-All-Around FET, process design kit, parasitic extraction, benchmark, air spacer

I. INTRODUCTION

Semiconductor process technology has rapidly developed over time. Simultaneously, as digitization is further accelerated, various attempts are being made for low-power and high-speed operations. Planar MOSFET with single gate have long been miniaturized using Moore's law and Dennard scaling rules. Near the 20nm technology node, device architectures such as Fin-FET have been introduced and even 5 nm technology nodes have been utilized [1]-[2]. In the sub-3nm technology node after Fin-FET, the introduction of gate-all-around-FET (GAA-FET) device architecture, which can be further scaled down by increasing the controllability of the gate electrode channel, is being considered [3]-[4]. As such, with the continuous development of front-end-of-line (FEOL), development of the wiring process is also required. This is because the effect of the parasitic R and C components in the wiring of the circuit at the nanoscale technology node is similar to or greater than the FEOL effect. Wiring can be divided into Middle-of-Line (MOL) and Back-End-of-Line (BEOL) components, and development of a new MOL structure (e.g., Bar-type contact, Partial-contact, etc.) or metal, and the

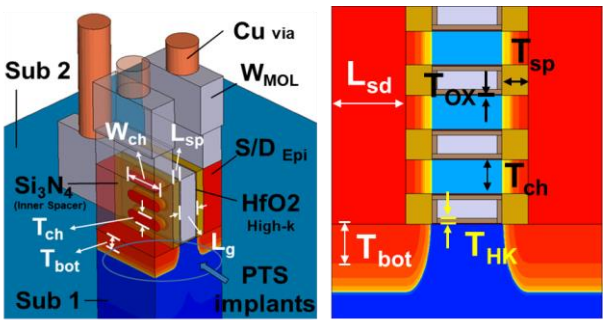
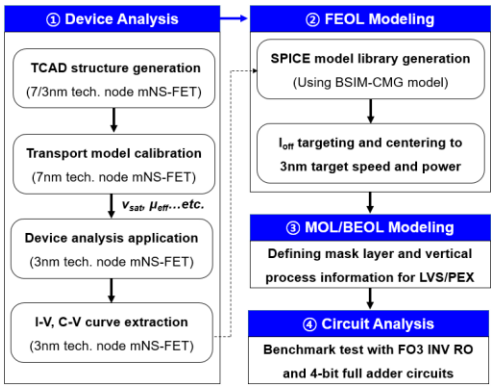


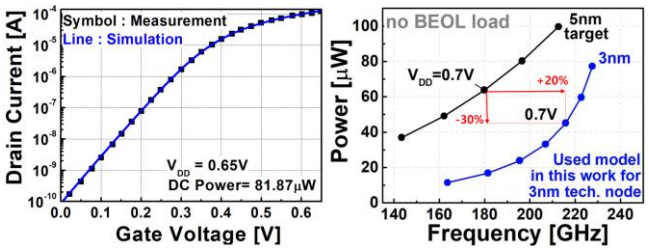
FIGURE 1. 3D structure and cross section view of (L)mNS-FET used in this work [4]

TABLE I
KEY DEVICE PARAMETERS FOR (L)MNS-FET USED IN THIS WORK TO DESCRIBE 3NM TECHNOLOGY NODE

Parameters	Values
Contacted poly-gate pitch (CPP)	45 nm
Gate length (l_g)	16 nm
Inner spacer thickness (T_{sp})	6 nm
Channel thickness (T_{ch})	8 nm
Channel width (W_{ch})	30 nm
Channel oxide thickness (T_{ox})	0.3 nm
Channel high-k thickness (T_{HK})	1.1 nm
Bottom oxide thickness (T_{BO})	20 nm
S/D over-etching depth (T_{bot})	8.5 nm
Channel doping	10^{17} cm^{-3}
S/D doping	$3 \cdot 10^{20}$ cm^{-3}
PTS doping (upper of substrate 1)	$3.6 \cdot 10^{18} \sim 1 \cdot 10^{19}$ cm^{-3}
Substrate 2 doping	10^{17} cm^{-3}



(a)



(b) (c)

FIGURE 2. (a) Overall workflow for the analysis of (L)mNS-FET-based device and circuit analysis, (b) calibration results of transport model parameters in TCAD software with measured data [4], and (c) FO3 INV RO simulation result after I_{OFF} targeting and centering to 3nm technology node target

dielectric materials are being continuously studied [5]-[9].

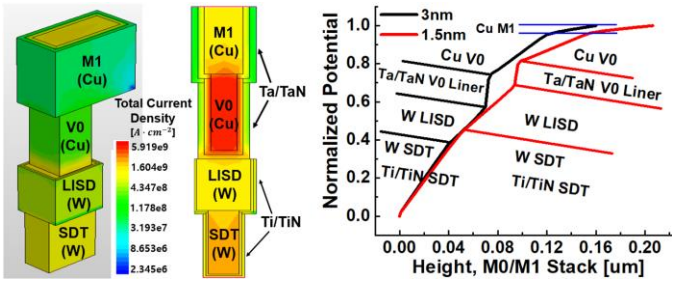
On the other hand, in order to design a circuit considering such wiring characteristics, it is impossible to perform schematic level circuit simulation, so layout-based circuit simulation is essential. To this end, a parasitic extraction (PEX) function is required to extract the RC values in the FEOL, wiring MOL, and BEOL areas from the circuit layout designed by the circuit designer in various forms and compose it into a netlist. In addition, the layout-versus-schematic (LVS) function that checks whether the layout and schematic match is also essential in the process of extracting the netlist including parasitic RC. The technology files are included in the process design kit (PDK) so that the mask information and vertical wiring material information at a specific technology node can be reflected in the electronic design automation (EDA) software that automatically performs these PEX and LVS functions. It is passed on from the process developer to the circuit designer [10]-[12].

In this work, we configured a PDK for path-finding to analyze the circuit layout in a 3 nm technology node based on a GAA-FET. path-finding PDK consists of the SPICE model library describing GAA-FET characteristics that satisfy 3nm power-performance-area (PPA) target characteristics, and models capable of performing LVS and PEX. Using this, it was possible to confirm the influence of the wiring effect on the logic integrated circuit. A multi-nanosheet FET was adopted as the architecture of the 3 nm GAA-FET. We quantitatively analyzed the effects of FEOL, MOL, and BEOL on circuit characteristics through path-finding PDK development at 3nm technology nodes, and the advantages of introducing an air spacer process that can most effectively improve circuit characteristics. As far as we know, these simulation results are the first in a 3nm technology node, and they will be helpful to determine the BEOL load for circuit design layouts and to guide the implementation of the improved wiring process. In the next section, the detailed environment and simulation results for this work are discussed.

II. Path-finding Process-Design-Kit (PDK) Setup and Integrated Circuit Analysis Results

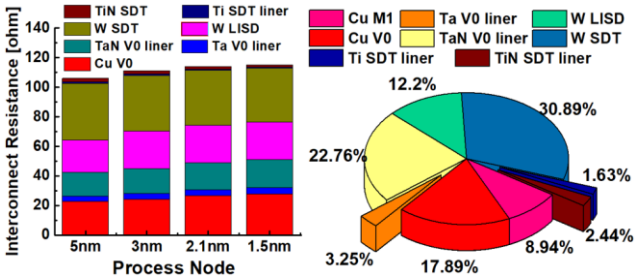
A. Front-End-of-Line Model

In this work, an (L)mNS-FET, a lateral multi-nanosheet field effect transistor using multiple nanosheet channels placed in the lateral direction in the 3nm technology node dimension, was used as the FEOL device. As shown in Fig.1, there are three nanosheet channels. In addition, the major dimensions of the 3nm technology node, such as contacted poly pitch (CPP) and channel length (L_{CH}), were set with reference to IRDS 2020, and their figures are summarized in Table1 [13]. The electrical properties of the (L)mNS-FET were simulated using the 3D TCAD software Synopsys' Sentarurus TM. The TCAD model used at this time was used by adding the following models to the drift-diffusion carrier transport model. The density gradient quantization model(eQuantumPotential) was



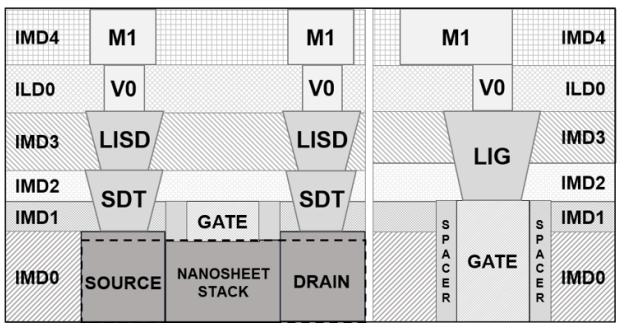
(a) (b)

FIGURE 3. **(a) Dual damascene-based 3D MOL structure used in TCAD simulation to extract MOL resistance to be utilized in PEX and current density profile, (b) potential profile at MOL region with L_{SD}=17nm (this work) and L_{SD}=20nm**



(a) (b)

FIGURE 4. **(a) MOL resistance extracted using 3D TCAD and trends in various L_{SD}, (b) Resistance segmentation results by MOL component at L_{SD}=17nm used in this work**



Layer	Width	Pitch	Relative Permittivity
M1-M3	12nm	24nm	3
V0-V2	8nm	17nm	3
LIG	12nm	45nm	7, 3.9
LISD	17nm	45nm	3.9
SDT	17nm	45nm	7
AR : 2		Gate height above top Nanosheet Stack : 20nm	

FIGURE 5. **Cross section view of MOL and BEOL stacks, and key parameters used in this work. Note that the aspect ratio(AR) of 2 is assumed all metals and via layers**

included to describe the quantum confinement effect, and the mobility model (phumob/high field saturation/Enormal) was utilized to consider the quantum effect, Coulomb scattering and interfacial surface roughness scattering. The Lombardi mobility model was included to calculate the mobility degradation by remote phonon and Coulomb scattering at the channel and insulator interface [14]-[15]. And a thin-layer mobility model was used to account for the thin channel thickness. To increase the accuracy of the TCAD model, the electrical characteristics of the (L)mNS-FET manufactured by hardware with 7 nm dimension and the TCAD model parameters were calibrated [4]. Then, using the BSIM-CMG model called the industry standard model, a BSIM-CMG model library that accurately describes the current-voltage and capacitance-voltage characteristics extracted through the TCAD simulation was created. Next, the BSIM-CMG model generated to satisfy the industry's 3nm circuit target speed and power consumption was simulated in an inverter ring oscillator circuit with fanout=3 (FO3 INV RO), which is a benchmark circuit, and centered to satisfy the target speed and power to produce the final FEOL model. This process is summarized in Fig.2, and the centered modeling results are also included.

B. Middle-of-Line and Back-End-of-Line Model

For circuit characteristic analysis, including layout-based wiring, parasitic RC extraction in the MOL and BEOL areas is required. The MOL area utilized the resistance value extracted from the metal layer through TCAD simulation, and for the capacitor, it was implemented using the dielectric value at the 3nm technology node indicated in the IRDS 2020 edition and previous work [10]. For the resistance value of the MOL region, the target value to be implemented in the EDA software, which that functions as PEX, was extracted through the 3D TCAD structure simulation, as shown in Fig.3(a). It has a structure composed of a source drain trench (SDT) and a local interconnect source drain (LISD) as a dual damascene process is applied, and a liner/barrier (Ti/TiN) is included in addition to the main conductor metal (tungsten, W), respectively.

Each dimension was determined by scaling the values applied to the 22 nm FinFET process to fit the 3nm technology node of the IRDS 2020. V0 represents the via metal (copper, Cu) between the LISD and metal 1 (M1), which also considers the liner/barrier (Ta/TaN). Through the TCAD environment constructed as shown in Fig.3 (a)-(b), the current density and potential profile in each MOL layer can be obtained, so that the resistance value of each layer can be predicted. To improve the simulation accuracy, the resistivity value of each MOL layer was calibrated using the previously reported resistance value of each MOL layer measured in the 22 nm FinFET process [16]-[17]. Fig.4 (a)-(b) show the extracted resistance value and portion of each MOL layer under the assumption that the liner/barrier thickness is fixed when the source/drain contact dimension (CD) is scaled down. As such, in order to consider the resistance values extracted

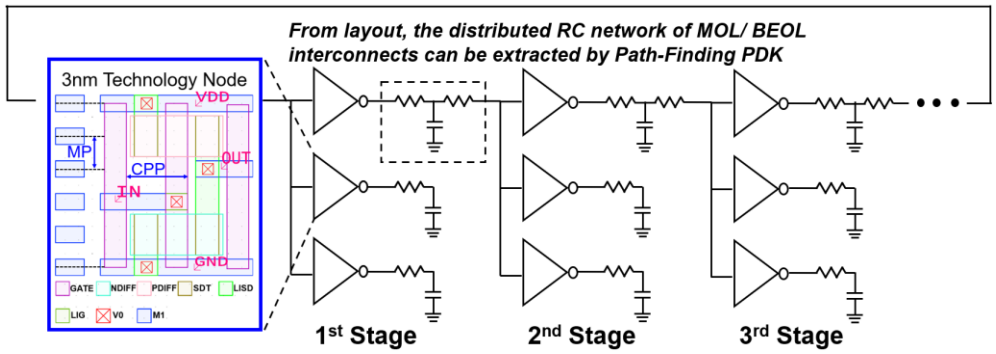
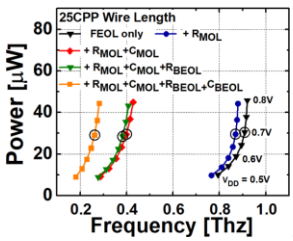


FIGURE 6. Schematic of FO3 INV RO, including INV unit cell layout. From layout, the distributed RC network of MOL/BEOL interconnects can be extracted automatically by using path-finding PDK



(a)

I_{OFF}= 4nA	Relative Frequency	Relative Power
Intrinsic	100% (Ref.)	100% (Ref.)
Int.+R_{MOL}	96% (-4%)	97% (-3%)
Int.+R_{MOL}+C_{MOL}	42% (-54%)	97% (0%)
Int.+R_{MOL}+C_{MOL}+R_{BEOL}	38% (-4%)	93% (-4%)
Int.+R_{MOL}+C_{MOL}+R_{BEOL}+C_{BEOL}	6% (-32%)	95% (+2%)

(b)

FIGURE 7. (a) Power versus frequency characteristics according to V_{DD}=0.5V to 0.8V in the FO1 INV RO circuit composed of 3nm GAA (L)mNS-FET to check the contribution of each wiring component, and (b) a table that summarizes the changes in relative speed and power by adding each wiring component

from the 3D TCAD during circuit layout, each mask layer was defined in the LVS/PEX function and applied to the resistance-related parameters. Fig.5 shows the vertical structure of the setup MOL and BEOL [12]. In Fig.5, the effective delivery of vertical information is different from the actual length ratio, and the actual dimension is specified in the table in Fig.5. In addition, the relative dielectric constant values of inter-layer dielectrics (ILD) and inter-metal dielectric (IMD) are included in the table in Fig.5. It is assumed that a low-k (=3.0) SiCOH material is used in the BEOL region ILD/IMD, and it can be confirmed that the C_W value of 208 aF/μm, which is the capacitance target value per BEOL unit length presented in IRDS 2020, is satisfied [10], [13]. In addition, the resistance-related parameters of M1 and M2 were set to satisfy R_W value of 301 Ω/μm, which is the resistance value per BEOL unit length presented in IRDS 2020.

C. Middle-of-Line (MOL), Back-End-of-Line (BEOL) Model

By post-layout simulation of INV RO and full-adder circuits using the completed path-finding PDK as described above, the PPA characteristics in logic operation and the air spacer process that can improve circuit characteristics were analyzed. Because Ioff=4nA is fixed, power is the active power consumption and performance represents the operating frequency, which is the reciprocal of the delay normalized by the INV stage number. Fig.6 shows a schematic of 9-stages FO3 INV RO, including the INV unit cell layout. For the 3 nm dimension, the contacted poly pitch (CPP) was 45 nm, the metal pitch (MP) is 24 nm and the number of track was 5. We confirmed the degradation of the circuit characteristics by MOL/BEOL by changing the FO number of the INV RO. and the wire length between the INV stages. In addition, we attempted to provide an effective wiring process guide for improving circuit performance by analyzing each parasitic component. Fig.7 shows the degradation of the circuit characteristics by adding MOL resistance (R_{MOL}), MOL capacitance (C_{MOL}), BEOL resistance (R_{BEOL}), and BEOL capacitance (C_{BEOL}) to the intrinsic characteristics of (L)mNS-FET. The circuit used is FO1 INV RO, and when supply voltage (V_{DD})=0.7V, the speed decreases by 4% and the power decreases by 3% by R_{MOL}, the speed decreases by 54% and the power fluctuation is insignificant by C_{MOL}. The case of BEOL may vary depending on the layout type, however as shown in Fig.7, the speed decreases by 4% and the power decreases by 4% by R_{BEOL}, the speed decreases by 32%, and the power increases by 2% by C_{BEOL}. In conclusion, it can be confirmed that the deterioration of the circuit characteristics due to capacitance is greater than that due to resistance. In particular, reducing C_{MOL} is the most effective in improving the circuit speed. The results of this analysis are summarized in the table of Fig.7. Through this, it can be seen that the development of a wiring process applied with a low-k dielectric in MOL and BEOL is more effective than the application of low resistive metal in improving circuit characteristics.

Fig.8 shows the result of the change in circuit characteristics according to BEOL loading as the wire length (L_{WIRE}) between the INV stages was varied. L_{WIRE} was normalized using CPP. In this work, the EDA software reflects the precise netlist using distributed RC, compared to the results [15],[18] in which the parasitic RC of the interconnection is manually reflected in the netlist, which is a more accurate analysis result. Short (L_{WIRE}=2 CPP), medium (L_{WIRE}=10 CPP, 25 CPP), and long (L_{WIRE}=50 CPP) tracks were analyzed. Medium-track is used for connection between cells or blocks, and long-track is used as buses at the macro-block level [19].

As shown in Fig.8(a), as the L_{WIRE} increases, the power-speed curve seems to shift to the left, which means that the speed decreases without a significant change in power. When L_{WIRE} is 2 CPP, 10 CPP, 25 CPP, and 50 CPP, the speeds decrease by 12%, 9%, 17%, and 26%, respectively, compared with W/O BEOL (BEOL is not applied) at V_{DD}=0.7V. As shown in Fig.8(b), the respective delays for the short, medium, and long interconnects are evaluated as

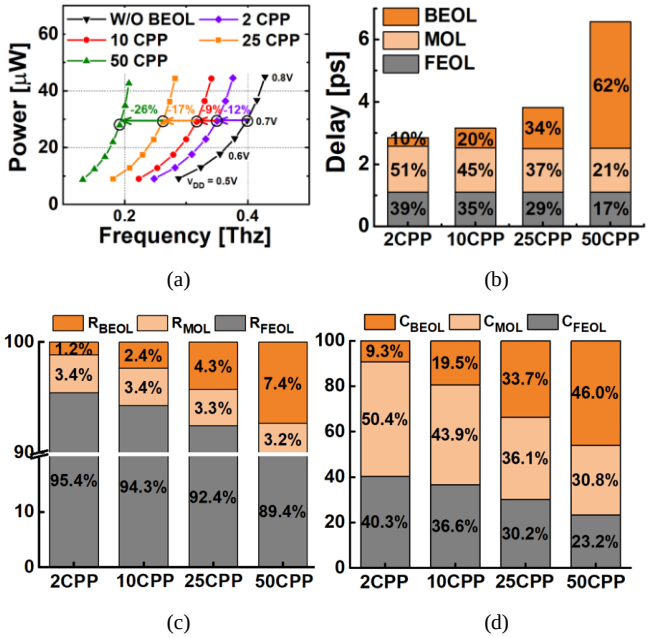


FIGURE 8. **(a) Power versus frequency characteristics according to V_{DD}=0.5V to 0.8V in the FO1 INV RO circuit composed of 3nm GAA (L)mNS-FET to check the influence of LWIRE variations, (b) changes in circuit delay characteristics according to LWIRE variations and analysis of contribution by FEOL, MOL, and BEOL components, (c) effective resistance (R_{EFF}) and (d) effective capacitance (C_{EFF}) extracted from simulated circuit operating characteristics at V_{DD}=0.7V, including contributions by FEOL, MOL, and BEOL components**

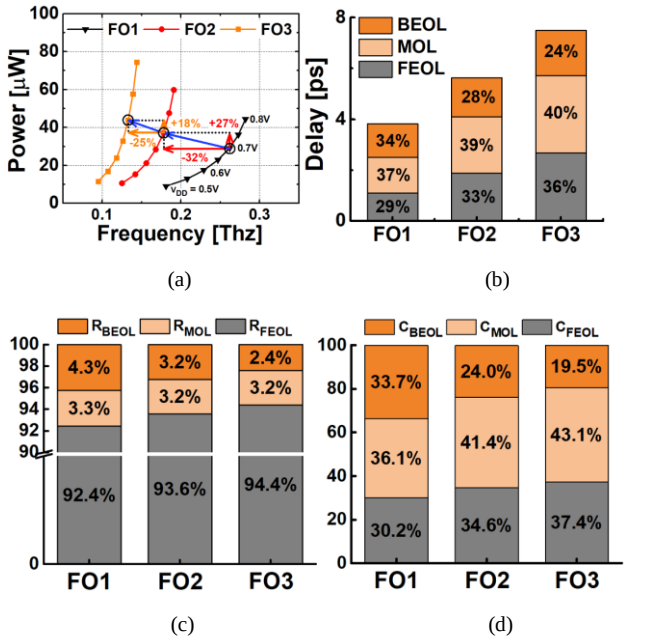


FIGURE 9. **(a) Power versus frequency characteristics according to V_{DD}=0.5V to 0.8V in the FO1 INV RO circuit composed of 3nm GAA (L)mNS-FET to check the influence of FO number, (b) changes in circuit delay characteristics according to FO number and analysis of contribution by FEOL, MOL, and BEOL components, (c) effective resistance (R_{EFF}) and (d) effective capacitance (C_{EFF}) extracted from simulated circuit operating characteristics at V_{DD}=0.7V, including contributions by FEOL, MOL, and BEOL components**

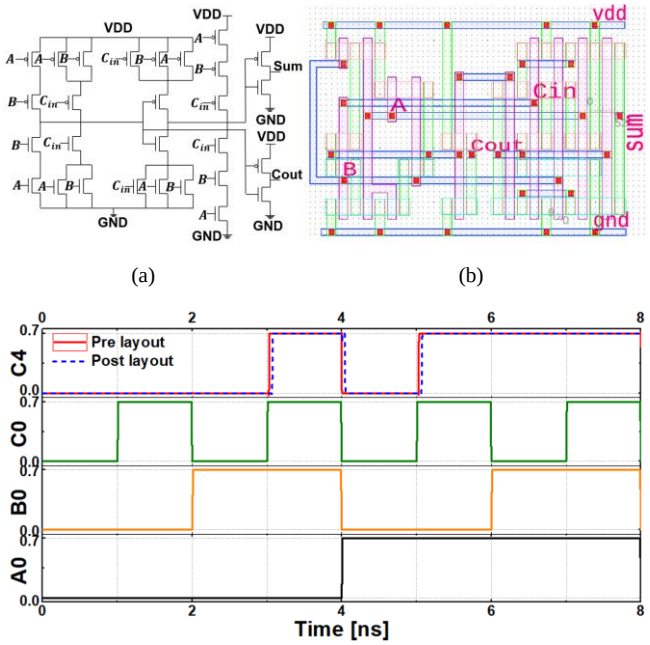
2.85ps, 3.16ps, 3.82ps and 6.57ps. Looking at the factors influencing the delay for each component, it can be seen that in the long track, approximately >60% is due to the BEOL, and in the short track, it is reduced to 10%, but still occupies a large portion.

As shown in Fig.7, the delay degradation due to the MOL is the largest, and among the R_{MOL} and C_{MOL} components, C_{MOL} has a greater effect, as shown in Fig.8(c)-(d). In addition, R_{FEOL} and C_{FEOL} have the greatest influence on delay in short track, but R_{BEOL} and C_{BEOL} have the greatest influence on delay in the medium track and long track. In particular, BEOL has a greater effect on circuit characteristics than MOL when the resistance is L_{WIRE}>25·CPP and the capacitance is L_{WIRE}>50·CPP.

Next, we observed the circuit characteristics by varying the number of FO. As shown in Fig.9(a), the speeds decrease and powers increase are simultaneously observed as the FO number increases. This is different from the change in L_{WIRE}, which showed only a decrease in speed. Compared with FO1 at V_{DD}=0.7V, the speed decreases by 32% and the power increases by 27% in FO2, and the speed decreases by 25% and the power increases by 18% in FO3. This is because the total C_{EFF} increases owing to the increase in the INV number between the input and output stages. As shown in Fig.9(b)-(d), the portion of MOL and BEOL on delay according to the change in FO number does not change significantly. In the R_{EFF} and C_{EFF}, the portions of each FEOL, MOL, and BEOL component does not change significantly. In the C_{EFF}, but the change in FO1→2 is larger than that in FO2→3. Consequently, it can be seen that the increase in C_{FEOL} and C_{MOL} has the greatest influence on the degradation of the circuit characteristics.

To analyze the change in circuit characteristics owing to wiring in a complex logic circuit, a conventional full-adder (28T FA) circuit consisting of 28 transistors (14 NMOS, 14 PMOS) was used as shown in Fig.10(a)-(b). The 28T FA circuit was designed with (L) mNS-FET-based path-finding PDK of a 3 nm technology node, and it was analyzed by using the key Figure of merit (FoM): standby power(P_{STAND}), dynamic power (P_{DYN}), delay (t_{DELAY}), energy-delay product (EDP), and power-delay product (PDP). In this work, a 1-bit full adder was used to measure the power and a 4-bit full adder was used to measure the delay. In the 4-bit full adder, the carry-in (C_{IN}) and carry-out (C_{OUT}) of four full adders were connected to each other, and the wire length was 25·CPP. When '0000 (A_3A_2 A_1A_0) + 1111 ($B_3B_2B_1B_0$) +1 (C_0)' is calculated, the time from the C_0 (C_{IN}) of the first full adder to the C_4 (C_{OUT}) of the last full adder is t_{DELAY} [20]. From the waveform of C4 in Fig.10 (c), it can be observed that there is a difference in t_{DELAY} in the pre- and post-layout simulations.

The results of the analysis are shown in Fig.11(a). Delay and power increase more in the post-layout than in the pre-layout owing to parasitic RC, and PDP and EDP also increase significantly. In the post-layout considering the wiring area, Fig.7-9 shows that the effects of MOL and BEOL are fatal to devices that satisfy 3nm node PPA. And parasitic RC caused by 28T Full Adder designed with 28 transistors and a minimum area greatly increased power and delay. Furthermore, it can be seen that PDP and EDP show



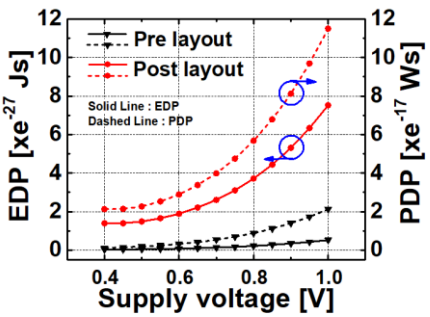
(a) (b)

(c)

FIGURE 10. **(a) Schematic and (b) layout of 28T CMOS full adder circuit, and (c) pre-layout and post-layout simulation waveform of 4bit full adder circuit**

	VDD [V]	Td [ps]	P_{DYN} [nW]	$P_{standby}$ [nW]	PDP [W·s]	EDP [J·s]
Pre-layout	0.7	24.65	220.3	12.87	$0.54e^{-17}$	$0.13e^{-27}$
Post-layout	0.7	65.4	610.3	12.87	$3.99e^{-17}$	$2.61e^{-27}$

(a)



(b)

FIGURE 11. **(a) Summary table of pre-layout and post-layout full adder circuit performance and (b) comparison of full adder circuit characteristics (EDP, PDP) in pre-layout and post-layout according to V_{DD}=0.4V-1.0V variation**

a larger increase because they are indicators made up of the product of delay and power. In addition, as shown in Fig.11(b), the difference in the PDP and EDP between the pre-layout and post-layout increases as V_{DD} increases. These results indicate that the characteristics of logic circuits can be changed up to two times or more by wiring, so wiring effects must be considered new process evaluation and circuit design in the next-generation node at the nanoscale.

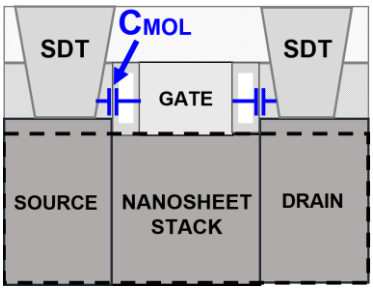
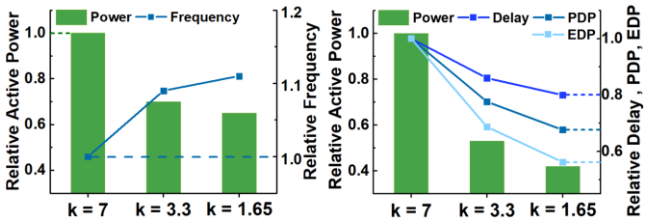


FIGURE 12. **A cross-sectional view of spacer introduced with Air spacer process**



(a) (b)

FIGURE 13. **(a) Comparison of FO1 INV RO circuit characteristics (active power, frequency) in post-layout according to V_{DD}=0.7V (b) Comparison of full adder circuit characteristics (active power, delay, PDP, EDP) in post-layout according to V_{DD}=0.7V.**

Next, we quantitatively analyzed the changes in the circuit characteristic when the air spacer process was introduced. Based on the results so far (Fig.7 and 8), it can be seen that the C_{MOL} has the greatest influence on the circuit characteristics. The dielectric constant is one of the important factors that determine the capacitance. Since the dielectric constant and capacitance have a proportional relationship, when the dielectric constant decreases, the capacitance can be reduced. The dielectric constant (=k) of air is 1 and it is much smaller than other dielectric materials (ex, SiO2's k = 3.9, SiN's k =7). Therefore, we introduced the air spacer process to reduce the degradation of circuit characteristics caused by C_{MOL} [21]-[22].

Fig.12 shows a simplified cross-sectional view when an air gap was inserted into the spacer area. It is a picture that shows the air gap, so it is different from the actual designed dimensions. For the dimensions, please refer to Table1 and Fig.5. As the portion occupied by the air pocket increases, the dielectric constant of the air spacer decreases. This enables a low-k dielectric process. In this work, when analyzing the change when introducing the air-spacer process, it is assumed that the air spacer consists of 20% and 50% air pockets. According to [21]-[22], the air pocket portion is 20% and 50% based on SiN (k=7), and the air spacer's k is reduced to 3.3 and 1.65, respectively. As the capacitance decreases with the decreased value of k, the degradation of circuit performance due to C_{MOL} is also improved. Because the parallel cap between the GATE and the SDT occupies the largest portion of the C_{MOL}, it is possible to improve the circuit characteristics using the C_{MOL} when the air spacer is introduced.

Fig.13 (a) shows the change in the characteristics of the 9-stages FO1 INV RO circuit when an air spacer is introduced.

It is based on the post-layout, L_{WIRE} is 25CPP. Also, the active power and speed of low-k spacer is normalized with k=7 at V_{DD}=0.7V. Under iso-speed conditions, the active power decreases by 30% when k is 3.3, and decreases by 35% when k=1.65. Under iso-power conditions, the frequency increased by 9% when k is 3.3, and increased by 11% when k=1.65. It can be seen that as the C_{MOL} decreases, the circuit characteristics are improved in the form of a decrease in active power and an increase in speed.

Fig.13 (b) shows the change in the circuit characteristics of the full adder through the same air pocket assumption and conditions as those of the RO. Under iso-speed conditions, the active power decreases by 47% when k is 3.3, and decreases by 58% when k=1.65. Under iso-power conditions, the delay decreases by 14% when k is 3.3, and decreases by 20% when k=1.65. PDP decreases by 22% when k is 3.3, and it decreases by 32% when k is 1.65. EDP decreases by 31% when k is 3.3, and it decreases by 44% when k is 1.65.

According to the above results, a significant improvement in the circuit characteristics can be expected owing to the introduction of a low-k dielectric process in the MOL region. This implies that it is important to introduce an advanced IMD process because the performance can be improved without improving the FEOL transistor with a complex 3D structure.

III. Conclusion

In this work, we constructed a path-finding PDK consisting of the LVS-PEX model implemented appropriately for the dimensions of a 3 nm GAA-FET and the spice model library made with 3-D TCAD for post-layout circuit analysis. Using the path-finding PDK, we quantitatively analyzed the effects of FEOL, MOL, and BEOL on the circuit characteristics at the 3nm node. As a result, the influence of the MOL and BEOL areas on the circuit characteristics was greater than 60%. We confirmed the effect of the interconnects in FO1 INV RO. When L_{WIRE} was 2 CPP, 10 CPP, 25 CPP, and 50 CPP, the speeds decreased by 12%, 9%, 17%, and 26%, respectively, compared with W/O BEOL. In the full adder, delay and power increase more than two times in the post-layout compared to the pre-layout due to interconnects. Next, we analyzed the changes in the circuit characteristics by introducing an air-spacer process. It can reduce C_{MOL} by making a low-k dielectric. Based on 9-stages FO1 INV RO with k = 7 at V_{DD} = 0.7V. Under iso-speed condition, the power is improved by 30%, 35% when k is 3.3, 1.65, respectively. Under iso-power condition, the speed is improved by 9%, 11% when k is 3.3, 1.65, respectively. And based on full adder with k = 7 at V_{DD} = 0.7V, Under iso-speed conditions, the active power is improved by 47%, 58% when k is 3.3, 1.65, respectively. Under iso-power conditions, the delay is improved by 14%, 20% when k is 3.3, 1.65, respectively. PDP is improved by 22%, 32% when k is 3.3, 1.65, respectively. EDP is improved by 31%, 44% when k is 3.3, 1.65, respectively. In conclusion, for circuit design in the next-generation node, the wiring effect must be considered, and an advanced IMD process must be introduced.

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