

# Investigation on the Ripple Voltage and the Stability of SR Buck Converters With High Output Current and Low Output Voltage

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**Abstract**—Synchronous rectifiers (SRs) composed of MOSFETs have recently been employed to replace the conventional rectifiers with diodes. SRs are widely used in switched-mode power supplies with low output voltage and high output current for efficiency improvement. Owing to the high-efficiency characteristic, it is adequate to use an SR buck converter in a voltage regulator for powering a central processing unit. Normally, such SR buck converter must operate at fairly high switching frequency for miniaturizing a whole circuit and achieving a fast response. However, at the conditions of low output voltage, high output current, and high switching frequency, the influence of parasitic elements to circuit operation will become extremely obvious. Therefore, the design considerations concerning the ripple voltage and the stability of such SR converters should be carefully investigated and clarified. By establishing the equivalent circuit and using a state-space averaged method, the ripple ratio of output voltage and the static and dynamic characteristics of the SR buck converter with nonnegligible parasitic elements are obtained. Thus, the design criteria concerning the output ripple voltage and the stability are clarified.

**Index Terms**—Ripple ratio, stability, synchronous rectifier (SR), voltage regulator.

## I. INTRODUCTION

OWING TO the miniaturization of electronic products, the switched-mode power supplies (SMPSs) for these electronic products are required to become smaller. In order to realize the miniaturization of the SMPSs, the switching frequency should be raised properly before the adverse effect of miniaturization appears. However, at high switching frequency, the influence of parasitic elements [such as the equivalent series resistance (ESR) of output capacitor, the equivalent series inductance (ESL) of output capacitor, etc.] will not be negligible. In addition, with the development of the integration technology, the power requirement of most microprocessors tends to be high current and low voltage [1]–[5].

Thus, the power supplies for the microprocessors will be forced to face the combined conditions of high switching frequency, low output voltage, and high output current, which will extremely enhance the influence of the parasitic elements. In particular, for the synchronous rectifier (SR) buck converters [6]–[28], which are used in voltage regulator for supplying

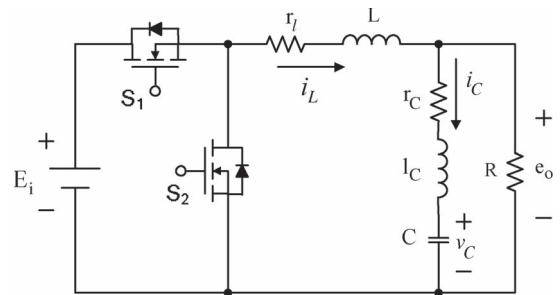


Fig. 1. Buck converter with SR.

power to a central processing unit (CPU), the operation conditions are extremely severe. In order to power a CPU, these converters are normally designed with the conditions of high switching frequency (500 kHz–1 MHz), very low output voltage (1.0–1.5 V), and very high output current (80–100 A).

Generally, most research topics regarding such SR buck converters are focused on the efficiency improvement and control method. However, this paper presents a unique point of view to link the ripple ratio of the output voltage and the stability by investigating the effects of the parasitic elements. In this paper, the effects of the parasitic elements on the output ripple voltage and the stability of the SR buck converter are analyzed and clarified. Moreover, several useful design considerations concerning the output ripple voltage and the stability are well summarized.

## II. EFFECTS OF THE PARASITIC ELEMENTS ON THE RIPPLE RATIO OF OUTPUT VOLTAGE

Fig. 1 shows an SR buck converter with SR, which can be used for powering a CPU. Due to the very low input voltage of the CPU, the output ripple voltage of the SR buck converter becomes an important issue.

Usually, an output capacitance is usually forced to be increased for suppressing the output ripple voltage. Although, theoretically, the output voltage ripple will decrease with the increase of the output capacitance, a minimum value of ripple voltage will exist practically. This minimum value is caused by the effects of the output capacitor's ESR and ESL.

### A. Derivation of Output Ripple Ratio

When  $S_1$  is in OFF state and  $S_2$  is in ON state, the equivalent circuit of Fig. 1 is shown in Fig. 2. In Fig. 2,  $L$  and  $C$  represent the output inductance and output capacitance, respectively;  $r_{S2}$ ,

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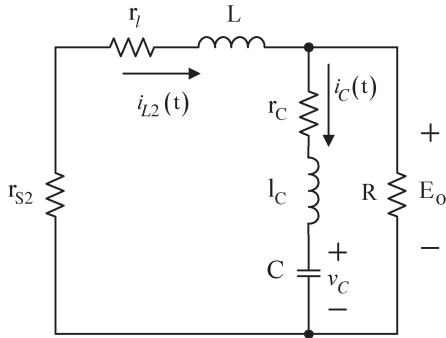
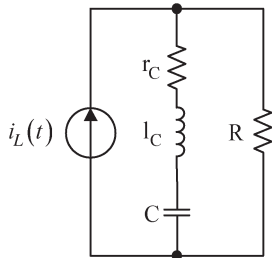

 Fig. 2. Equivalent circuit of the SR buck converter ( $S_1$  OFF;  $S_2$  ON).


Fig. 3. Equivalent circuit for shunt mechanism.

$r_l$ ,  $r_c$ ,  $R$ , and  $l_c$  represent the ON resistance of  $S_2$ , the spurious resistance of output inductor, the ESR of output capacitor, load resistance, and the ESL of output capacitor, respectively; and  $i_{L2}$  and  $E_O$  represent the instantaneous value of the current flowing through  $S_2$  and the averaged value of the output voltage  $e_O$ , respectively.

For the condition of large output capacitance (for the experimental prototype used in the research, the large output capacitance can be regarded as no less than 2000  $\mu\text{F}$ ), the output voltage  $e_O$  in Fig. 1 can be assumed as a constant value  $E_O$  in Fig. 2; thus, the circuit equation of  $i_{L2}$  can be expressed by

$$i_{L2}(t) = I_L^* e^{-\left(\frac{r_2}{L}\right)t} - \frac{1}{r_2} \left(1 - e^{-\left(\frac{r_2}{L}\right)t}\right) E_O \quad (1)$$

where  $I_L^*$  represents the initial value of  $i_{L2}$ , and  $r_2 = r_{S2} + r_l$ .

Under high switching frequency condition, the ripple current of output inductor can be obtained as

$$\Delta I_L = \frac{D'T_S E_O}{L} \left(1 + \frac{r_2}{R}\right) \quad (2)$$

where  $T_S$  and  $D$  represent the switching period and duty ratio, respectively, and  $D'$  is equal to  $1 - D$ .

According to (2), the circuit equation of the output inductor's current in the durations  $0 < t \leq DT_S$  and  $DT_S < t \leq T_S$  can be obtained at the same time axis, as given in (3), shown at the bottom of the page.

Owing to the output condition of high current and low voltage, a part of the current ripple in the output inductor will flow

into the load. The equivalent circuit for this shunt mechanism is shown in Fig. 3.

According to the equivalent circuit shown in Figs. 2 and 3, the ripple ratio of output voltage  $r_v$  can be derived as

$$\begin{aligned} r_v &\equiv \frac{\Delta E_O}{E_O} \\ &= \frac{1}{L} \frac{R}{(R+r_c)^2 + \omega^2 l_c^2} \left( \frac{[r_c(R+r_c) + \omega^2 l_c^2] D'}{f_s} + \frac{R l_c}{D} \right) \\ &\quad \times \left( 1 + \frac{r_{S2} + r_l}{R} \right) \end{aligned} \quad (4)$$

where  $\omega = 2\pi f_s$ .

By using the differential method, the maximum ripple ratio  $r_{v,\max}$  with respect to  $l_c$  can be obtained as (5), where the value of  $l_{c,\max}$ , which causes the  $r_{v,\max}$ , is shown in

$$r_{v,\max} = \frac{R}{L} \left( 1 + \frac{r_2}{R} \right) \left[ \frac{4\pi^2 D D' (R+r_c) g^2 + Rg + D D' R}{D f_s (R+r_c) (1 + 4\pi^2 g^2)} \right] \quad (5)$$

$$l_{c,\max} = \frac{(R+r_c)}{f_s} \left( D D' + \sqrt{D^2 D'^2 + (1/4\pi^2)} \right) \quad (6)$$

where  $g = D D' + \sqrt{D^2 D'^2 + (1/4\pi^2)}$ .

It is shown from (3) that, under the conditions of high switching frequency, low output voltage, and high output current, theoretically, these parasitic elements will definitely affect  $r_v$ . Equations (4) and (5) clearly indicate the existence of the maximum ripple ratio  $r_{v,\max}$  and the specific value of  $l_{c,\max}$  which causes it. They will provide an important reference for choosing the output capacitor in the design phase.

Under the condition of high switching frequency, the ESL of the output capacitor will be affected by many parameters, such as component selecting, printed circuit board layout, circuit wiring, and so on. Therefore, for designing SMPSs with high switching frequency, low output voltage, and high output current, the  $r_{v,\max}$  should be carefully taken into account to ensure  $r_v$  to its specification.

## B. Experimental Results

In order to clarify the shunt mechanism and practical characteristics of  $r_v$ , an experimental prototype is implemented. Tables I and II show the specifications and component values of this prototype, respectively. For observing the output ripple voltage clearly, an external resistor (38.75 m $\Omega$ ) is in series with the output capacitor. Thus, the equivalent  $r_c$  is equal to 42 m $\Omega$ .

Fig. 6 shows the experimental waveform of the prototype's output voltage. The measured value  $r_v$  in Fig. 4 is 0.158. Under the same condition, the simulated value  $r_v$  according to (4) is 0.146. It is shown that the simulated result is very close to the experimental result.

$$i_L(t) = \begin{cases} -\frac{\Delta I_L}{2} + \frac{\Delta I_L}{DT_S} t = \frac{D'E_O}{DL} \left(1 + \frac{r_2}{R}\right) \left(t - \frac{DT_S}{2}\right), & 0 < t \leq DT_S \\ \frac{\Delta I_L}{2} - \frac{\Delta I_L}{D'T_S} (t - DT_S) = -\frac{E_O}{L} \left(1 + \frac{r_2}{R}\right) \left(t - DT_S - \frac{D'T_S}{2}\right), & DT_S < t \leq T_S \end{cases} \quad (3)$$

TABLE I  
SPECIFICATIONS OF THE PROTOTYPE

Symbol	Definition	Value
$f_s$	Switching frequency	500kHz
$E_i$	Input voltage	12V
$E_o$	Output voltage	1.5V
$I_o$	Output current	15A
$k$	Feedback constant	$0.17V^{-1}$

TABLE II  
COMPONENT VALUES OF THE PROTOTYPE

Symbol	Definition	Value
$r_l$	Spurious resistance of output inductor	1.1 m $\Omega$
$r_{S2}$	ON resistance of $S_2$	5.9 m $\Omega$
$L$	Output inductance	0.6 $\mu$ H
$C$	Output capacitance	2280 $\mu$ F
$R$	Load resistance	100 m $\Omega$
$r_C$	ESR of output capacitor	3.25 m $\Omega$
$l_C$	ESL of output capacitor	8nH

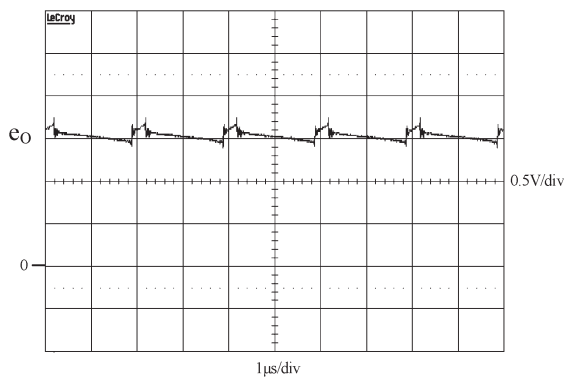


Fig. 4. Experimental waveform of output voltage ( $r_2 = 7$  m $\Omega$ ,  $r_C = 42$  m $\Omega$ ,  $R = 100$  m $\Omega$ , and  $l_C = 8$  nH).

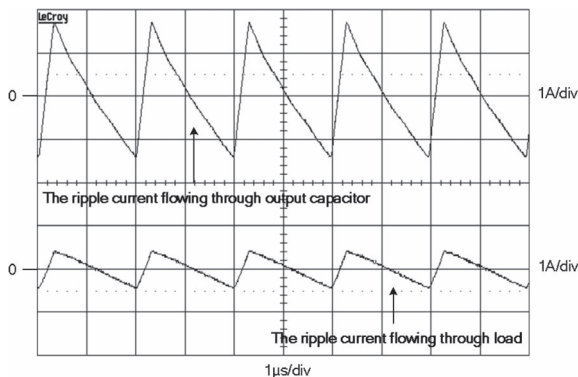


Fig. 5. Output ripple currents.

In this prototype, owing to the ESR of output capacitor that is close to the load resistance under a heavy-load condition, the shunt mechanism of the output ripple current through the load resistance and the output capacitor's ESR can be obviously observed. Fig. 5 shows the practical shunt waveform of output ripple current. It is shown that the ripple current flowing

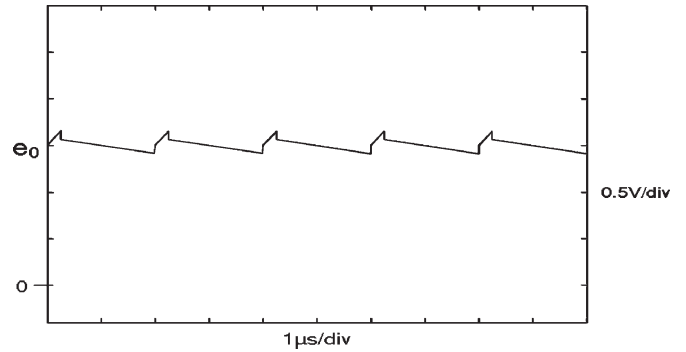


Fig. 6. Simulated waveform of output voltage ( $r_2 = 7$  m $\Omega$ ,  $r_C = 42$  m $\Omega$ ,  $R = 100$  m $\Omega$ , and  $l_C = 8.6$  nH).

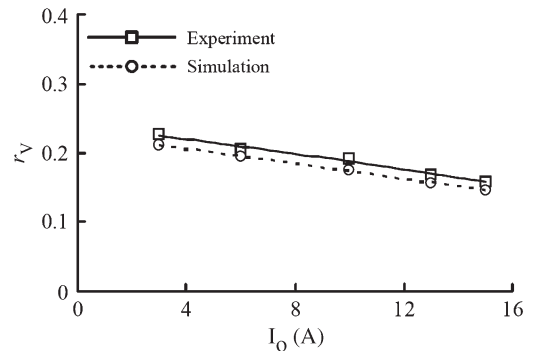


Fig. 7. Simulated and experimental results of  $r_v$  versus  $I_o$ .

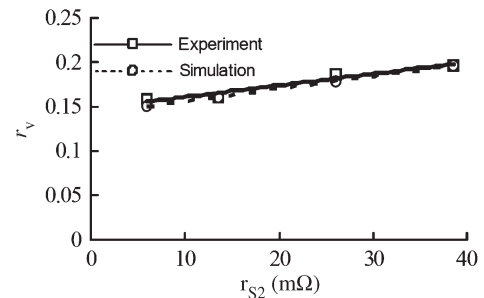


Fig. 8. Simulated and experimental results of  $r_v$  versus  $r_{S2}$ .

through the output capacitor is 2.81 A, and the ripple current flowing through the load is 0.89 A.

For verifying the theoretical analysis, Fig. 6 shows the simulated waveform of the output voltage. Figs. 7–10 show the simulated and experimental  $r_v$ 's with respect to different  $I_o$ ,  $r_{S2}$ ,  $r_C$ , and  $l_C$  values, respectively. All of the simulated results are based on the derived equations shown previously.

From Figs. 4 and 6, it can be seen that the simulated waveform of the output voltage agrees very well with the experimental waveform. Thus, the correctness of the theoretical analysis is confirmed. By varying the load resistance, the experimental results of  $r_v$  versus  $I_o$  can be obtained. Fig. 7 shows both the simulated and experimental results of  $r_v$  versus  $I_o$ . Being different from the  $r_v$  of ideal buck converters,  $r_v$  will vary with  $I_o$  due to parasitic elements. From Fig. 7, it is shown that the experimental results agree well with the simulated results, both of them show that  $r_v$  decreases with the increase of  $I_o$  in this case.

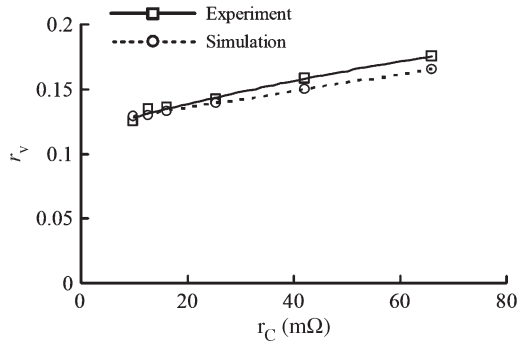


Fig. 9. Simulated and experimental results of  $r_v$  versus  $r_C$ .

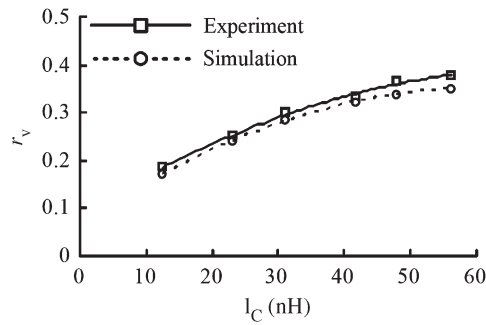


Fig. 10. Simulated and experimental results of  $r_v$  versus  $l_C$ .

By adding different resistors in series with  $S_2$ , the experimental results of  $r_v$  versus  $r_{S2}$  can be obtained. Fig. 8 shows both the simulated and experimental results of  $r_v$  versus  $r_{S2}$ . From Fig. 8, the simulated results are almost equal to the experimental results. Both the results show that  $r_v$  increases linearly with the increase of  $r_{S2}$ .

By adding different resistors in series with the output capacitor, the experimental results of  $r_v$  versus  $r_C$  can be obtained. Fig. 9 shows both the simulated and experimental results of  $r_v$  versus  $r_C$ . According to Fig. 9, the simulated results agree well with the experimental results. It is confirmed that  $r_v$  is monotonously increased with the increase of  $r_C$ .

In order to investigate the effects of the output capacitor's ESL on  $r_v$ , different inductors are put in series with the output capacitor. Fig. 10 shows both the simulated and experimental results of  $r_v$  versus  $l_C$ . Based on Fig. 10, it is verified that the simulated results agree well with the experimental results. In this case,  $r_v$  will increase with the increase of  $l_C$ .

From Figs. 7–10, it can be seen that all the experimental results agree well with the simulated results, although there are very small differences between them.

### III. EFFECTS OF THE PARASITIC ELEMENTS ON THE STABILITY

In order to clarify the stability characteristics of the SR buck converter with high output current and low output voltage, this paper investigates the effects of parasitic elements (including the spurious resistance of output inductor  $r_l$ , the ESR of output capacitor  $r_C$ , and the ESL of output capacitor  $l_C$ ) on the stability of such SR buck converter. By using a state-space averaged

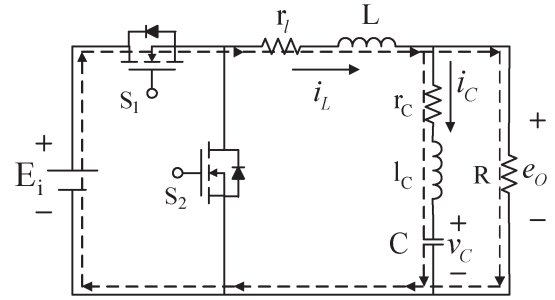


Fig. 11. Operation state A.

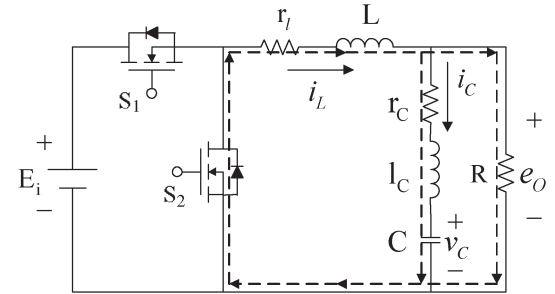


Fig. 12. Operation state B.

method [29]–[33], the static and dynamic characteristics of the SR buck converter can be obtained.

#### A. Analysis of Static and Dynamic Characteristics of the SR Buck Converter

Fig. 1 shows the circuit configuration of the SR buck converter. Based on the circuit operation of the SR buck converter, there are two operation states in one switching period. They are operation states A and B. The operation state A refers to the state that  $S_1$  is ON and  $S_2$  is OFF, and operation state B refers to the state that  $S_1$  is OFF and  $S_2$  is ON. Figs. 11 and 12 show the circuit operations of operation states A and B, respectively. For the simplicity of the stability analysis, the ON resistances of  $S_1$  and  $S_2$  are regarded as the same. Moreover, they are combined in  $r_l$ ; thus, the equivalent  $r_l$  for each operation state is equal to 7.8 mΩ.

Based on Figs. 11 and 12, the circuit equations of each operation state can be formulated as follows.

For operation state A,

$$\left. \begin{aligned} L \frac{d}{dt} i_L + r_l i_L + R(i_L - i_C) &= E_i \\ l_C \frac{d}{dt} i_C + r_C i_C + v_C &= R(i_L - i_C) \\ C \frac{d}{dt} v_C - i_C &= 0. \end{aligned} \right\} \quad (7)$$

For operation state B,

$$\left. \begin{aligned} L \frac{d}{dt} i_L + r_l i_L + R(i_L - i_C) &= 0 \\ l_C \frac{d}{dt} i_C + r_C i_C + v_C &= R(i_L - i_C) \\ C \frac{d}{dt} v_C - i_C &= 0. \end{aligned} \right\} \quad (8)$$

The state-space averaged method is used for the theoretical analysis. From the given equations, the state equations of the SR buck converter can be derived. Thus, the state equations and the

static and the dynamic characteristics of the SR buck converter are obtained as follows:

For the state equations,

$$\frac{d}{dt}\hat{\mathbf{X}} = \mathbf{A}\hat{\mathbf{X}} + \mathbf{b}E_i \quad (9)$$

where

$$\mathbf{A} = \begin{bmatrix} -\left(\frac{R+r_l}{L}\right) & \frac{R}{L} & 0 \\ \frac{R}{l_C} & -\left(\frac{R+r_C}{l_C}\right) & -\frac{1}{l_C} \\ 0 & \frac{1}{C} & 0 \end{bmatrix}$$

$$\mathbf{b} = \begin{bmatrix} \frac{D}{L} \\ 0 \\ 0 \end{bmatrix}$$

$$\hat{\mathbf{X}} = \begin{bmatrix} \hat{i}_L \\ \hat{i}_C \\ \hat{v}_C \end{bmatrix}.$$

For the static characteristics (conversion ratio),

$$M \triangleq \frac{E_O}{E_i} = \frac{DR}{r_l + R}. \quad (10)$$

For the dynamic characteristics,

$$G_{ED}(s) \triangleq \frac{\Delta e_O(s)}{\Delta D(s)} = \frac{p_{D0} + p_{D1}s + p_{D2}s^2}{Q_{D0} + Q_{D1}s + Q_{D2}s^2 + Q_{D3}s^3} \quad (11)$$

where

$$\begin{aligned} p_{D0} &= E_i R \\ p_{D1} &= E_i RC r_C \\ p_{D2} &= E_i RC l_C \\ Q_{D0} &= R + r_l \\ Q_{D1} &= L + RC(r_l + r_C) \\ Q_{D2} &= RLC \\ Q_{D3} &= CLL_C. \end{aligned}$$

## B. Theoretical and Experimental Results

Based on the prototype's specifications shown in Table I and the derived equations of the static and the dynamic characteristics, the stability characteristics of the SR buck converter can be analyzed in the following two parts.

1) *Theoretical Investigation:* According to (11), the stability characteristics of the SR buck converter will be affected by many parameters theoretically. Each individual parameter will contribute different influences to the stability characteristics of this converter. Since the load resistance and parasitic elements exist in practical circuits, their combined effects on the stability characteristics will be very complex. In order to analyze the effect of each individual parameter on the stability characteristics, the influence contributed by other parameters shall be minimized.

TABLE III  
SIMULATED PHASE MARGIN ( $r_C = 0$ ,  $l_C = 0$ , AND  $r_l = 0$ )

$I_O$ (A)	Phase margin (degree)
3	2
10	5
15	8

TABLE IV  
SIMULATED PHASE MARGIN ( $l_C = 0$ ;  $r_l = 0$ )

$r_C$ (m $\Omega$ )	Phase margin (degree)		
	$I_O=3A$	$I_O=5A$	$I_O=15A$
3.25	30	34	36
16.2	95	96	98
25.3	108	109	110

TABLE V  
SIMULATED PHASE MARGIN ( $r_C = 0$ ;  $r_l = 0$ )

$l_C$ (nH)	Phase margin (degree)		
	$I_O=3A$	$I_O=10A$	$I_O=15A$
8	1.56	5.2	7.8
21.6	1.53	5.1	7.6
35	1.5	5	7.5

Thus,  $l_C$ ,  $r_C$ , and  $r_l$  shall be set to zero for investigating the effect of load resistance on the stability of the SR buck converter. According to (11), the phase margin of this converter can be simulated to express the stability characteristics. The simulated results with respect to different output currents are shown in Table III. As shown in Table III, when  $l_C$ ,  $r_C$ , and  $r_l$  are all equal to zero, theoretically, the phase margin is slightly increased.

For investigating the effects of the output capacitor's ESR ( $r_C$ ) on the stability of the SR buck converter,  $l_C$  and  $r_l$  shall be set to zero. The simulated results with respect to different  $r_C$ 's and different output currents are shown in Table IV.

From Table IV, when  $l_C$  and  $r_l$  are equal to zero, theoretically, the phase margin will increase with the increase of  $r_C$  and output current.

For investigating the effects of the ESL of output capacitor ( $l_C$ ) on the stability of the SR buck converter,  $r_l$  and  $r_C$  shall be set to zero. The simulated results with respect to different  $l_C$ 's and different output currents are shown in Table V.

As can be observed in Table V, when  $r_l$  and  $r_C$  are equal to zero, theoretically, the phase margin will slightly increase with the increase of output current. Moreover, the increase of  $l_C$  has no effect on the phase margin.

2) *Comparison of the Theoretical and Experimental Results:* To investigate the practical stability characteristics of the SR buck converter, the gain and phase measurements are needed to verify the simulated Bode diagrams. With the comparison of the theoretical and experimental results, the theoretical and practical performances on the stability of this prototype will be clarified. For the most severe condition of the stability, the output current is fixed at a light load ( $I_O = 3$  A) in the experiments.

To investigate the effects of the output capacitor's ESR ( $r_C$ ) on the stability of the prototype, the parameters except  $r_C$  are fixed in the experiments. The experimental and theoretical



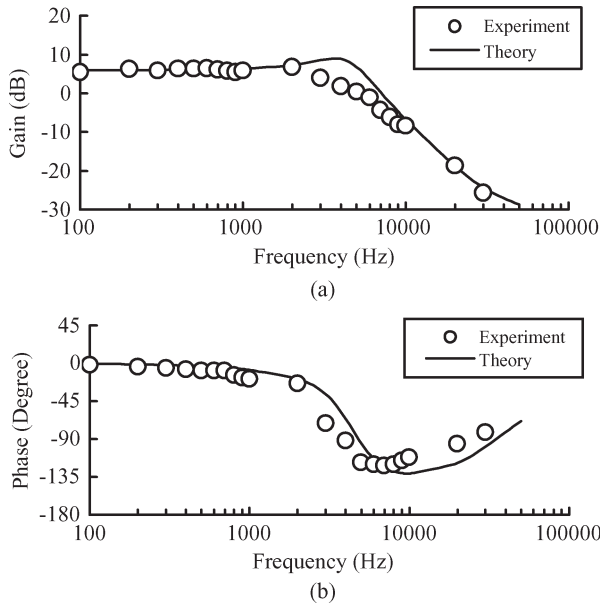


Fig. 13. Bode diagram of the prototype ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ ,  $l_C = 8$  nH, and  $r_C = 3.25$  m $\Omega$ ). (a) Gain. (b) Phase.

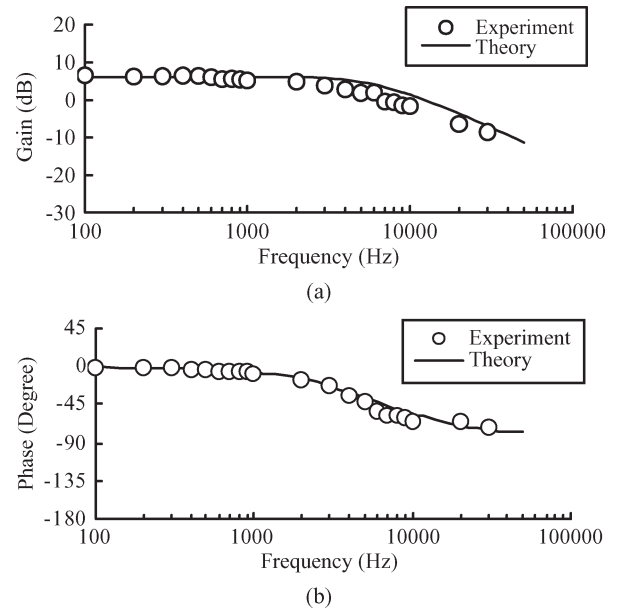


Fig. 15. Bode diagram of the prototype ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ ,  $l_C = 8$  nH, and  $r_C = 25.3$  m $\Omega$ ).

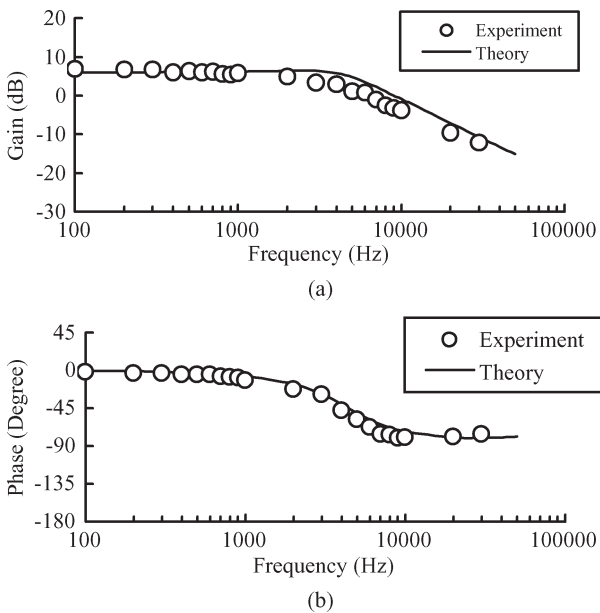


Fig. 14. Bode diagram of the prototype ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ ,  $l_C = 8$  nH, and  $r_C = 16.2$  m $\Omega$ ). (a) Gain. (b) Phase.

results with different  $r_C$ 's under a light load ( $I_O = 3$  A) are shown in Figs. 13–15, respectively.

As can be observed from Figs. 13–15, the experimental results agree well with the theoretical results. For the convenient of analysis, all the simulated and experimental phase margins are listed in Table VI. According to Table VI, as  $r_l$  and  $l_C$  are fixed under the condition of light load, theoretically and experimentally, the phase margin will obviously increase with the increase of  $r_C$ .

To investigate the effects of the ESL of output capacitor ( $l_C$ ) on the stability of the prototype, the parameters except  $l_C$  are fixed in the experiments. The experimental and theoretical

TABLE VI  
EXPERIMENTAL AND SIMULATED PHASE MARGINS ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ , AND  $l_C = 8$  nH)

$r_C$ (m $\Omega$ )	Theory	Experiment
	Phase margin (degree)	Phase margin (degree)
3.25	53	62
16.2	108	112
25.3	118	121

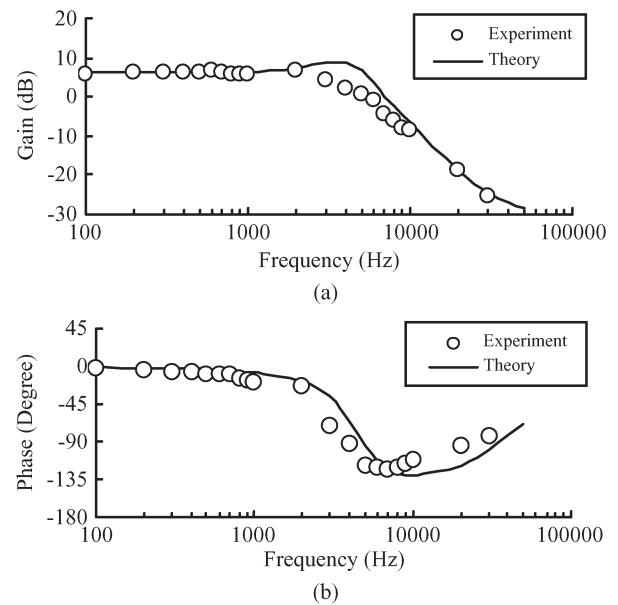


Fig. 16. Bode diagram of the prototype ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ ,  $l_C = 8$  nH, and  $r_C = 3.25$  m $\Omega$ ). (a) Gain. (b) Phase.

results under a light load ( $I_O = 3$  A,  $r_C = 3.25$  m $\Omega$ , and  $r_l = 7.8$  m $\Omega$ ) are shown in Figs. 16–18, respectively.

As can be observed from Figs. 16–18, the experimental results agree well with the theoretical results. According to

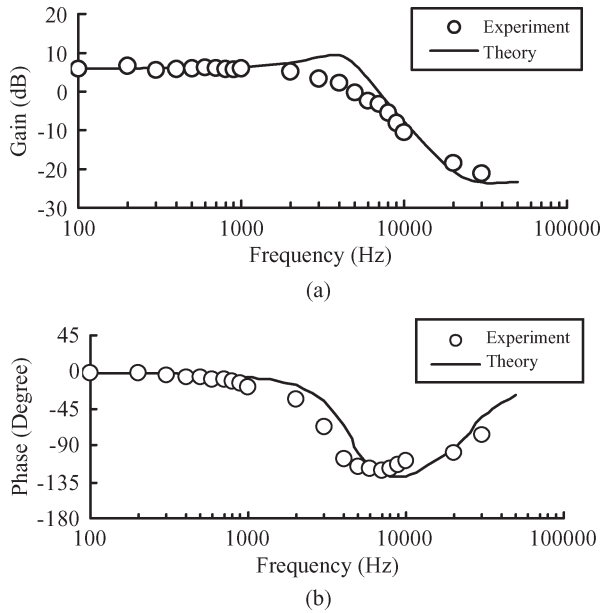


Fig. 17. Bode diagram of the prototype ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ ,  $l_C = 21.6$  nH, and  $r_C = 3.25$  m $\Omega$ ). (a) Gain. (b) Phase.

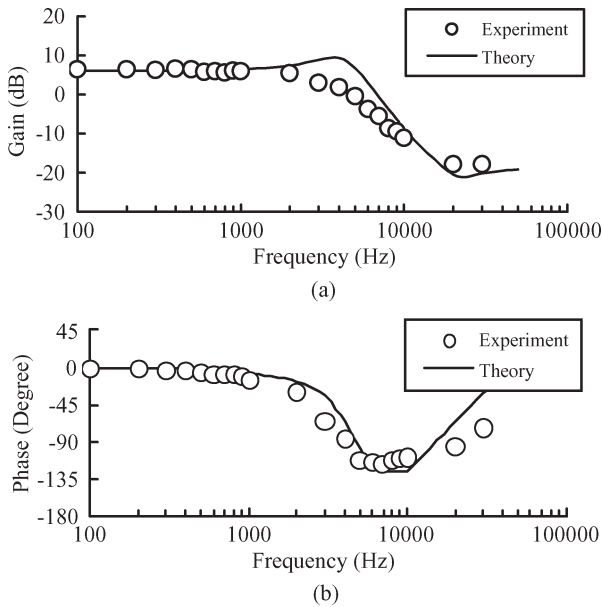


Fig. 18. Bode diagram of the prototype ( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ ,  $l_C = 35$  nH, and  $r_C = 3.25$  m $\Omega$ ). (a) Gain. (b) Phase.

TABLE VII  
EXPERIMENTAL AND SIMULATED PHASE MARGINS  
( $I_O = 3$  A,  $r_l = 7.8$  m $\Omega$ , AND  $r_C = 3.25$  m $\Omega$ )

$l_C$ (nH)	Theory	Experiment
	Phase margin (degree)	Phase margin (degree)
8	53	62
21.6	55	64
35	57	67

Figs. 16–18, the simulated and experimental phase margins are listed in Table VII. From Table VII, as  $r_l$  and  $r_C$  are fixed under the condition of a light load, the phase margin will slightly increase with the increase of  $l_C$  by both theory and experiment.

#### IV. DISCUSSION

Since the effects of parasitic elements on converters are fairly complex and able to be ignored for some cases, these elements are not usually taken into account at the design phase. However, under the conditions of high switching frequency, low output voltage, and high output current, the effects of the parasitic elements on circuit operation should be paid with attention.

Based on previous two sections, it is clear that the parasitic elements will affect the output ripple voltage and the stability of the whole circuit.

For the output ripple voltage, the following design considerations are summarized.

- 1)  $r_v$  will increase linearly with the increase of  $r_{S2}$ .
- 2)  $r_v$  is monotonously increased with the increase of  $r_C$ .
- 3)  $r_v$  will increase with the increase of  $l_C$ .
- 4) Equations (5) and (6) clearly indicate the existence of the maximum ripple ratio  $r_{v,max}$  and the specific value of  $l_{C,max}$  which causes it. This point of view will provide an important reference for choosing the output capacitor in the design phase.

For the stability, the following design considerations are summarized.

- 1) As  $r_l$ ,  $r_C$ , and  $l_C$  are zero, theoretically, the stability of the circuit will slightly increase with the increase of the load current.
- 2) As  $r_l$  and  $l_C$  are fixed, theoretically and experimentally, the phase margin will obviously increase with the increase of  $r_C$ .
- 3) As  $r_l$  and  $r_C$  are fixed, theoretically and experimentally, the phase margin will slightly increase with the increase of  $l_C$ .

Normally, it is believed that  $l_C$  will be adverse to the stability. However, it is found from this research that not only  $r_C$  but also  $l_C$  can improve the stability of the SR buck converter.

On the other hand, the output ripple voltage will increase with the increase of  $r_C$  and  $l_C$ . Therefore, for a balanced design on the ripple voltage and the stability, choosing an output capacitor with reasonable  $r_C$  and  $l_C$  will be helpful. Within the reasonable range of  $r_C$  and  $l_C$ , the output capacitor with larger  $l_C$  and smaller  $r_C$  is acceptable for higher output efficiency. A design example is shown as follows.

Generally, the reasonable value of  $r_C$  is about several milliohms to tens of milliohms (in this paper, 5–25 m $\Omega$ ), and the reasonable value of  $l_C$  is about several nanohenrys to tens of nanohenrys (in this paper, 5–25 nH). Under the condition of  $E_i = 12$  V,  $E_O = 1.5$  V,  $I_O = 3$  A,  $f_S = 500$  kHz,  $r_l = 1.1$  m $\Omega$ ,  $r_{S2} = 5.9$  m $\Omega$ ,  $L = 0.6$   $\mu$ H, and  $C = 2280$   $\mu$ F, the simulated results of phase margin with respect to different  $r_C$ 's and different  $l_C$ 's are shown in Table VIII. According to Table VIII, the value of  $r_C$  should be chosen between 15 and 25 m $\Omega$  for obtaining enough phase margin (greater than 100 $^\circ$ ).

Since the value of  $r_C$  is decided between 15 and 25 m $\Omega$ , the simulated results of  $r_v$  versus  $l_C$  can be seen in Fig. 19. According to Fig. 19, it is shown in this figure that the ripple ratio of the output voltage  $r_v$  with respect to two kinds of  $r_C$  is almost the same (the maximum difference between two curves

TABLE VIII  
SIMULATED PHASE MARGIN WITH RESPECT TO  
DIFFERENT  $r_C$ 'S AND DIFFERENT  $l_C$ 'S

$r_C$ (m $\Omega$ )	Phase margin (degree)		
	$l_C=5\text{nH}$	$l_C=15\text{nH}$	$l_C=25\text{nH}$
5	65	67	68
10	91	93	94
15	105	107	109
20	113	115	117
25	117	119	121

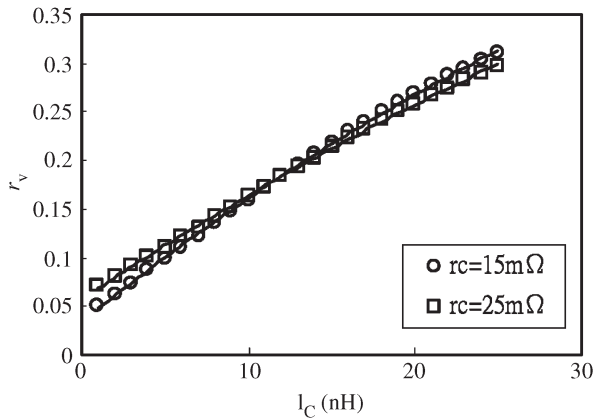


Fig. 19. Simulated results of  $r_v$  versus  $l_C$  (taking  $r_C$  as a parameter).

is 0.014). Based on the aforementioned results, an  $l_C$  of 25 nH and an  $r_C$  of 15 m $\Omega$  can be used to obtain enough phase margin and reduce the power dissipation of  $r_C$ .

## V. CONCLUSION

For SR buck converters with high output current and low output voltage, the parasitic elements have affected the circuit characteristics remarkably, particularly the output ripple voltage and stability. Moreover, in this paper, it has been shown that these parasitic elements link the ripple ratio of the output voltage and the stability.

All the research findings will provide designers an important reference to estimate the effects of the parasitic elements. With these design considerations, designers can make a good tradeoff on the circuit design and the component selection in the design phase.

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