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Wavy Channel TFT Architecture for High Performance Oxide Based Displays

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We show the effectiveness of wavy channel architecture for thin film transistor application for increased output current. This specific architecture allows increased width of the device by adopting a corrugated shape of the substrate without any further real estate penalty. The performance improvement is attributed not only to the increased transistor width, but also to enhanced applied electric field in the channel due to the wavy architecture.

Introduction

Amorphous Oxide Semiconductors (AOS) promise high mobility, high output current, low thermal budget and large scale integration opportunity, which make them potential candidates as backplane Thin Film Transistors (TFTs) for high resolution flexible Organic Light Emitting Diode (OLED) displays [1-3]. However, high resolution OLED displays require both smaller pixel size and high enough output currents to drive OLED pixels [4]. Recently we have shown effectiveness of wavy channel (WC) architecture for high performance transistors [5, 6]. The architecture allows expanding the device width vertically by corrugating the substrate to increase performance without extra chip area penalty. Here, we show ALD ZnO channel based WCTFT that employs fin-type *continuous* features, allowing expansion of TFT width, leading to enhanced 3.5× output current at drain voltage as low as 5V, 50% higher field effect mobility at the same gate overdrive voltage, and similar I_{ON}/I_{OFF} ratio compared to a planar transistor consuming the same chip area [7, 8]. The performance improvement is attributed not only to the increased transistor width, but also to enhanced applied electric field in the channel due to the wavy architecture. We have also studied the impact of gate-length scaling using the new architecture down to gate-length of 5 μm [9]. It was found that smaller gate lengths yield higher drain current for the same percentile increase in the device width due to a combination of electric field enhancement and threshold voltage shifting.

Device Fabrication

Fig. 1(a) shows the process flow to fabricate WCTFT, where the 1.5 μm fin features are first patterned on a heavily doped n-type silicon wafer, with a minimum resistivity of 8 mΩ.cm, which is also used as a back gate. Fin height was confirmed using a DEKTAK profilometer. This is followed by deposition of 50 nm of Atomic Layer Deposition (ALD) Aluminum Oxide (Al_2O_3) as a gate dielectric. Titanium-gold (Ti/Au) based

source/drain was then formed using sputtering and lift-off process. Finally, low-temperature Zinc Oxide (ZnO) is deposited using ALD and patterned by wet etching. Fig. 1(b) shows a 50 µm channel length transistor with 15 fins. The TFT architecture is Bottom Gate Bottom Contact (BGBC).

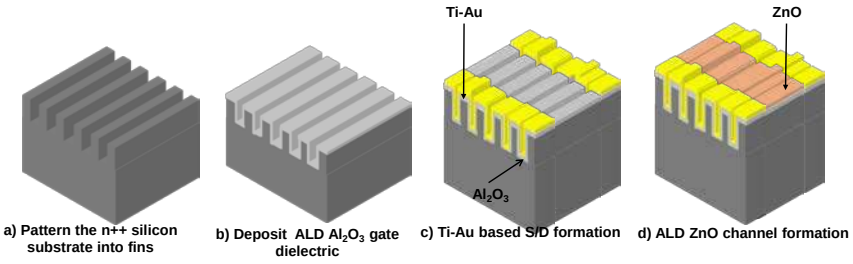

Fig. 1(a): Fabrication process flow for wavy channel thin film transistor. Obtained with permission from [8]. Copyright: IEEE 2014.

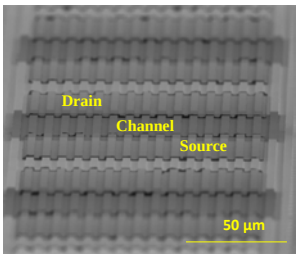

Fig. 1(b): SEM of the fabricated WCTFT. Obtained with permission from [8]. Copyright: IEEE 2014.

A cross sectional scanning electron microscope (SEM) of the ZnO/Ti-Au/Al_2O_3/Si confirmed (data not show) a thickness of ~47 nm of Al_2O_3,128 nm of Ti/Au layer and ~ 40 nm of ZnO, respectively. The films are uniform and conformal without any voids. The ZnO film resistivity was confirmed by a four-point probe measurement to be ~ 1 Ω.cm. An atomic force microscopic (AFM) scan of ZnO layer confirmed a roughness (RMS) of 1.54 nm (data not shown). The AFM image also indicates the amorphous state of the film due to the small grain size of ZnO. Grazing Incidence XRD (GIXRD) also confirmed that the film is mostly amorphous with very weak (100) and (002) Wurtzite peaks. To confirm this, we performed surface SEM image, and found ZnO nanocrystals whose size is less than 50 nm.

Electrical Characterization

The electrical characteristics of both the planar and WC devices were compared for channel lengths of 50, 20, 15, 10 and 5 µm. Keithley 4200 semiconductor parameter analyzer was used for measuring the electrical characteristics. All presented data are averages of 8 devices, and the device width used for normalization in the case of WC devices is (W_{planar} + W_{extra}). W_{extra} is calculated as 2× fin height (1.5 µm) × the number of fins per device. When comparing "ON" current ratios between planar and WC devices, we compared devices on the same die, so that the electrical characteristics involved in the comparison are prone to wafer-to-wafer, and die-to-die process variability.

Device Performance vs. Number of Fins

We have compared planar devices with W_{planar}/L (250/50) µm to WC devices, namely, 4 µm 1:1, 1:2, 1:3 and 1:5 devices, which have 32, 21, 16 and 10 fins, respectively, corresponding to extra device width (W_{extra}) of 96, 63, 48 and 30 µm. W_{extra} is calculated as 2× fin height (1.5 µm) × the number of fins per device. The naming

notation is such that 4 µm 1: y represents devices with 4 µm wide fins and (4 × y) µm distance between every two consecutive fins. Fig. 2(a) shows the gate leakage currents of planar and 32 fins devices, showing a normalized leakage current of 0.04 nA/µm and 0.06 nA/µm for the planar and 32 fins devices, respectively, which indicates that the gate leakage is not degraded in the WC architecture.

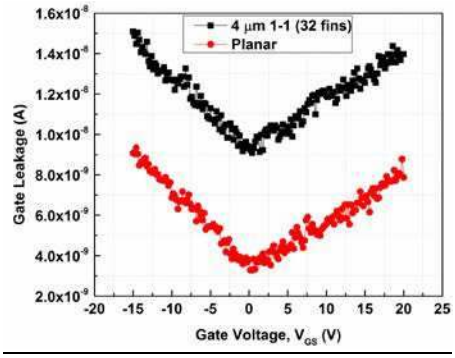

Fig. 2(a): Gate leakage currents of the 4 µm 1-1 (32 fins) devices *vs.* planar devices. Obtained with permission from [8]. Copyright: IEEE 2014.

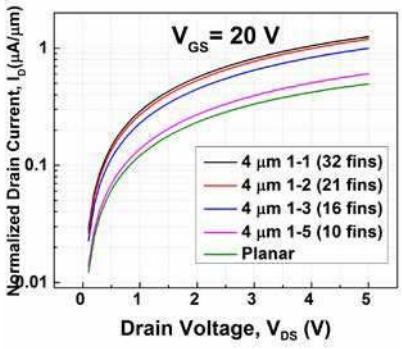

Fig. 2(b): Output characteristics comparison at V_g = 20V, at step size of 0.1V. Obtained with permission from [8]. Copyright: IEEE 2014.

Both threshold voltage, V_T, shift, as well as, an increase in the normalized drain current are noticed as a function of the number of fins. For example, Fig. 2(b) shows that the 32 fin devices (4 µm 1:1) have normalized current of 1.25 (µA/µm) while the planar devices have only 0.5 (µA/µm). The 4 µm 1:3 devices with an intermediate number of fins, 16 fins, show a normalized current of 1(µA/µm). As for switching characteristics, $I_{ON/OFF}$ ratios for both planar and WC devices were on the order of 10^5.

To look for a trend in the different devices characteristics as function of the number of fins, we have plotted the on-state drive current (I_{ON}), WC to planar I_{ON} ratio, threshold voltage (V_T), and saturation mobility, μ_{sat}, as a function of the number of fins in Fig. 3.

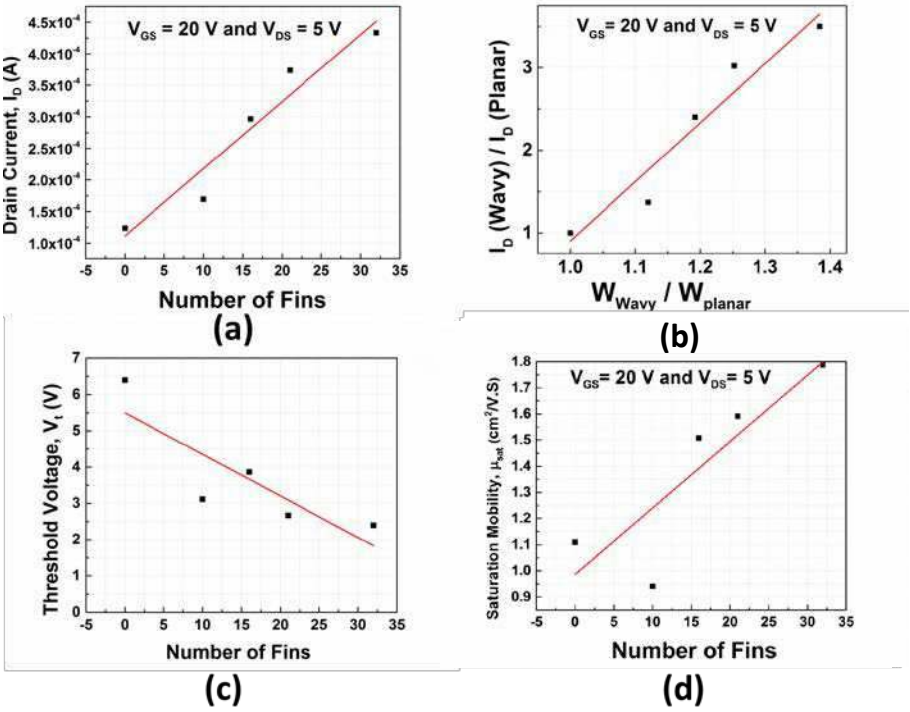

Fig. 3(a) Comparison of output characteristics drain current values at V_g = 20V and V_d = 5V as a function of the number of fins. (b) Fin to planar drain current ratio as a function of fin to planar device width ratio. (c) Threshold voltage, V_T, variation as a function of the number of fins. (d) Electric field mobility *vs.* number of fins. Obtained with permission from [8]. Copyright: IEEE 2014.

Fig. 3(a) shows a comparison of I_D values extracted from output characteristics, as a function of the number of fins at the same biasing conditions. It shows there is a linear dependence of the output current on the number of fins. Fig. 3(a) also shows that the 4 µm 1:1 (32 fin) devices has an average output current of 4.5×10^{-4} A while the planar devices have an output current of 1.25×10^{-4} A. The ratio of the output current of the WC devices to planar counterparts is shown in Fig. 3(b). The ratio of the output current of the WC 32 fin device to the planar device is 3.5, while their respective device width ratio is 1.4. Hence, the increase in the device current cannot be simply attributed to the extra width. Therefore, we analyzed the threshold voltage (V_T) dependence of the devices on the number of fins. V_T values were extracted from saturation region in the $\sqrt{I_D}$–V_{GS} curve by extrapolation from the point of the highest first derivative [10]. The voltage values are plotted in Fig. 3(c), which shows that V_T values linearly decrease as a function of the number of fins. The planar device has V_T of 6.4V, while WC devices have shown values of 3.1, 3.9, 2.7 and 2.4 for WC devices with 10, 16, 21 and 32 fins, respectively. Fig. 3(d) shows saturation field effect mobility, μ_{sat}, as a function of number of fins, showing linear scaling with the number of fins. Mobility values were extracted from the linear portion of the $\sqrt{I_D}$–V_{GS}, as shown in equation (1) [11]:

$$\mu_{sat} = \left(\frac{2L}{W}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2 \quad [1]$$

This confirms that μ_{sat} also linearly scales up with the number of fins.

To discount the V_T shift effect in the analysis of μ_{sat} as a function of gate bias, we plotted μ_{sat} *vs.* (V_{GS}–V_T) in Fig. 4. We found that the 32, 21 and 16 fins WC devices show higher saturation mobility when compared to 10 fins and planar devices. While planar devices show $\mu_{sat} = 1.3\frac{cm^2}{V.s}$ at V_{GS}–V_T =13.6V, the 32 fins WC device shows $\mu_{sat} = 1.85\frac{cm^2}{V.s}$ at the same V_{GS}–V_T value. This amounts 42% increase in μ_{sat} of WC devices when compared to planar devices.

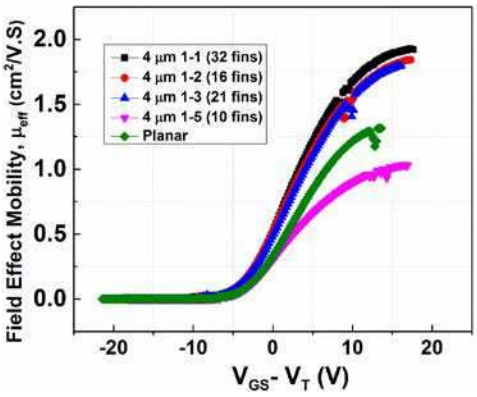

Fig. 4: Field effect mobility as a function of electric field applied to the gate.

Device Performance *vs.* Gate length

The performance of the WC architecture as function of the device gate length was tested in a different fabrication run. We compared the devices for the same number of fins, 8 fins, for 4 different gate lengths, namely 20, 15, 10 and 5 μm. The planar devices have a width of 140 μm, and the WC devices have an extra width due to fins of 18 μm. This amounts to 13% larger device width for WC devices when compared to the planar counterparts. Figs. 5(a, b) show the transfer and output characteristics of 20 μm gate length devices, respectively. The planar and WC TFTs show V_T values of 0.5V and 0.76V, respectively, as extracted from the transfer curve in Fig. 5(a). The devices also show an I_{ON}/I_{OFF} ratio of 10^5. Gate leakage of both devices was in the 100 pA range as shown in Fig. 5(a). The output characteristics in Fig. 5(b) show that the planar devices have $I_{ON\ planar}$ of 9×10^{-6} A while the WC counterpart have $I_{ON\ WC}$ = 1.35 $\times10^{-5}$ A. The lower current in this fabrication run is attributed to a higher film resistivity as measured by a four point probe and was found to be ~10 Ω.cm.

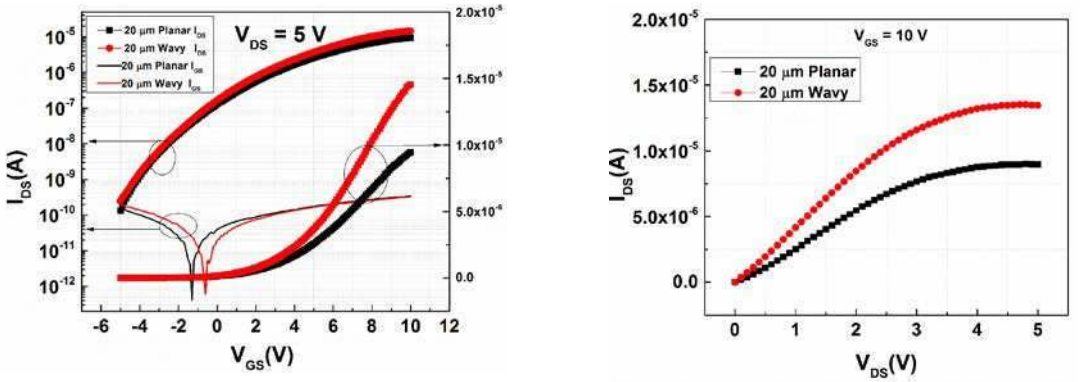

Fig. 5(a) Transfer and (b) output characteristics of planar and wavy transistors for gate length L_g = 20 μm. Obtained with permission from [9]. Copyright: Wiley-VCH 2014.

However, when comparing the ratios of planar and WC devices for L_g = 20 μm, it was found to be ~ 1.5× that of the planar counterpart, as shown in Fig. 6(a). The mask design was such that a row of planar devices lie within 200 μm distance from a row of WC devices to insure fair comparison when comparing 'ON' current ratio values. Thus, only neighboring devices were considered in calculating the ratio to minimize any die-to-die variation. Similar analysis was carried out for devices with gate lengths of 15, 10 and 5 μm, as shown in Fig. 6(b). The ratio was found to be ~1.5×, 1.65×, and 2.4× for the 15, 10, and 5 μm TFTs, respectively, when compared at the same biasing condition of V_{DS} = 5V and V_{GS} = 10V.

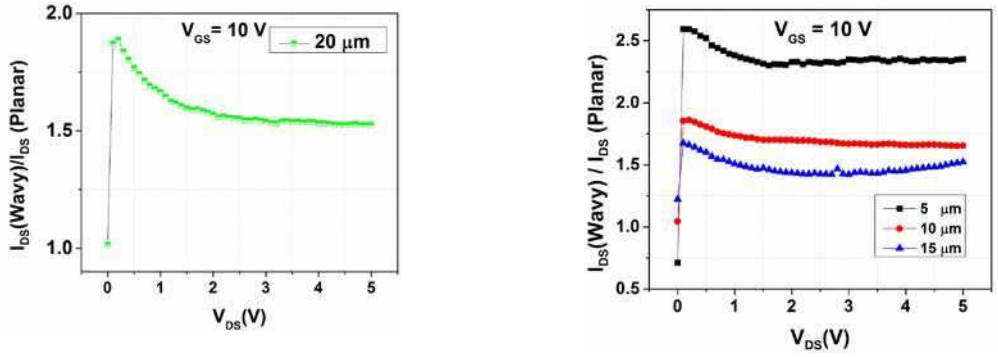

Fig. 6: (a) Wavy to planar ON current ratio for 20 μm gate length devices and for showing 1.5× increase for wavy ON current over planar counterpart (b) and ~1.5×, 1.65× and 2.4× for 15, 10 and 5 μm gate length devices, respectively. Obtained with permission from [9]. Copyright: Wiley-VCH 2014.

Discussion

To analyze why WC devices have shown 50% higher mobility and exhibited V_T shift as a function of the number of fins, we have simulated the electric field profile along the fin sidewall, since out devices are accumulation mode devices, and the turn on behavior is correlated with the electric field in the channel. Therefore, we have simulated the structure using COMSOL simulation tool to measure the electric displacement field (D)

map inside the Al_2O_3 dielectric, as shown in Fig. 7. For the simulation, we have used Cu as a metal back gate, Al_2O_3 (50 nm) gate dielectric and a voltage bias, representing the overdrive voltage (V_{GS}–V_T), of 5V. The simulation involved solving the displacement field equation, $\nabla . D = \rho_v$, where D is the displacement field, and ρ_v is the charge density, and the negative gradient of the potential equation, $E = -\nabla V$, where E is the electric field and V is the scalar charge potential. We have solved both equations for the displacement field, D. Fig. 7 also shows that that the electric field is higher around bottom corners, giving a D value of 0.007 C/m^2, while the D value is 0.005 C/m^2 in the planar parts. This would mean that charge accumulation would occur at an earlier gate voltage around the bottom corners, and could explain the V_T shift as a function of the number of fins. As for the top corners, we believe that a previously reported effect in FinFET, which shows that electrostatics of the fin geometry causes lowering of V_T in top corners up to 20% relative to sidewall threshold voltages [12]. The effect is independent of the fin width, and is dependent only on the shape of the top corner, which is highest when the angle of top corner is close to 90^o.

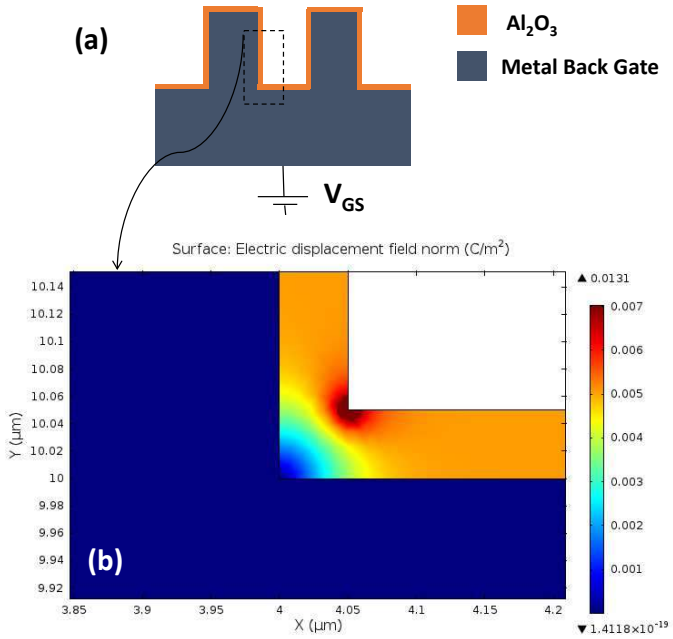

Fig. 7: (a) Schematic of the back gate dielectric interface, and (b) COMSOL simulation of Displace Electric Field, D, showing high D values at corners due to contribution from both the side walls and the planar part, which is termed L-shaped field enhancement. Obtained with permission from [8]. Copyright: IEEE 2014.

As for the shorter channel TFTs, specifically L = 5 µm, we believe that a combination of electric field enhancement, and lowering of V_T due to short-channel-effects [13], have caused the higher wavy-to-planar ratio, 2.4× of I_{ON} current. This shows that the architecture is scalable down to the L = 5µm, and could be effectively used to boost performance and allow for faster switching of OLED pixels. We believe coupling the WC architecture with higher mobility materials such as Indium Gallium Zinc Oxide (IGZO), or Low Temperature Poly Silicon (LTPS) could further enhance the switching

characteristics which is needed for faster OLED pixels switching since the architecture is material independent, as we previously have shown for poly-silicon TFTs [14].

Conclusion

We have shown ZnO TFT with both WC and planar architectures. Drain currents, threshold voltages and field effect mobility have shown to linearly scale with the number of fins. The device with maximum number of fins has shown 3.5× drain current values and almost twice the field effect mobility of its' planar counterpart. WC devices have shown 1.5×, 1.65× and 2.4× extra 'ON' current value when compared to planar counterparts for 20, 10 and 5 µm devices. The low 'OFF' current levels for WC devices, ~100 pA, and high $I_{on/off}$ ratios, ~10^5, insure that standby power consumption remain similar to planar counterpart, while improving 'ON' current values. This proves the significance of this new architecture for large area high resolution display applications. The enhancement in the wavy device performance cannot only be attributed to the extra device width, but also to and electric field enhancement in the channel due to the wavy TFT architecture.

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