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Cite as: AIP Advances **10**, 125225 (2020); https://doi.org/10.1063/5.0030098
Submitted: 19 September 2020 • Accepted: 23 November 2020 • Published Online: 21 December 2020

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Kelotchi S. Figueroa,[1] Nicholas J. Pinto,[1,a)] Chengyu Wen,[2] A. T. Charlie Johnson,[2] and Meng-Qiang Zhao[3]

AFFILIATIONS

[1]Department of Physics and Electronics, University of Puerto Rico at Humacao, Humacao, Puerto Rico 00791, USA
[2]Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, Pennsylvania 19104, USA
[3]Department of Chemical and Materials Engineering, New Jersey Institute of Technology, Newark, New Jersey 07102, USA

[a)]**Author to whom correspondence should be addressed:** nicholas.pinto@upr.edu

ABSTRACT

Monolayer MoS_2 crystals investigated in this work were grown via chemical vapor deposition on Si/SiO_2 substrates. Using a wet KOH etch, these crystals were transferred onto the edge of a freshly cleaved *p*-Si/SiO_2 wafer where they formed mechanically robust heterojunctions at the *p*-Si/MoS_2 interface. Electrical characterization of the device across the junction yielded an asymmetric I–V response similar to that of a *p*-*n* diode. The I–V response was electrostatically tunable via an ionic liquid gel gate. This is the first report demonstrating reversible gate control of the *p*-Si/MoS_2 diode current by several orders of magnitude while lowering its turn-on voltage. Fermi energy level shifts within the MoS_2 bandgap by the gate was believed to be responsible for the observed effects. The ease of fabrication, low operating voltages (<±2 V), and moderately high throughput currents (~1 μA) are attractive features of this diode, especially for use in sensors and power saving electronics.

I. INTRODUCTION

Modern-day solid-state devices are a result of scientific progress in the physics of semiconductors. Impurity doping gives these materials technologically important attributes, e.g., choice of charge carrier type[1] and control of charge concentration via, for example, an external electric field.[2] Generally classified as *p*- or *n*-type, semiconductors are essential components of the electronics industry. Bonding together a *p*- and an *n*-type semiconductor yields a junction diode that possesses unique characteristics, such as allowing current to flow in one direction across the junction while blocking it in the other.[3] It is a device that can rectify alternating signals, forming the fundamental building block in complex integrated circuits. Expanding the use of a *p*–*n* diode beyond rectification is an active field of study that has led to novel applications ranging from solar cells[4] to lasers[5] and light emitting diodes.[6] Controlling some of the diode parameters, like the current or the turn-on voltage, further enhances its functionality and is the primary focus of this work.

The recently discovered two-dimensional (2D) transition metal dichalcogenides (TMDCs) have similar electronic properties to classical semiconductors.[7,8] Investigating these materials is important from the viewpoint of new physics and device applications. Molybdenum disulfide (MoS_2) is one such TMDC that exhibits stable *n*-type semiconducting behavior and can be controllably grown in the laboratory via chemical vapor deposition (CVD).[9,10] Diodes using MoS_2 have recently been shown to be tunable in addition to exhibiting electro-optic properties.[11–15] We previously reported on a UV light tunable, CVD grown MoS_2/*p*-Si junction diode with rectifying capability.[16] Herein, we extend that study to include electrostatic tuning of a similar diode via an ionic liquid (IL) gel gate. Two factors motivated us to use an IL gel for gating: the diode architecture that was ideally suited for manual application of a liquid gate material (no cumbersome spin-coating or thermal evaporation was needed) and the high IL specific capacitance that ensured low operating voltages. This is the first report where IL gel gating is shown to reversibly control a MoS_2 based diode current by several orders of magnitude while lowering its turn-on voltage. The ease of fabrication, low operating voltages (<±2 V), and moderately high throughput currents (~1 μA) make this diode useful in sensors and as a power saving device in battery operated electronics.

II. EXPERIMENTAL

Monolayer MoS_2 crystals of varying sizes were grown on Si/SiO_2 substrates via CVD, as reported earlier,[10] and transferred to a new substrate for diode fabrication. In the transfer process, a thin film of poly (methyl methacrylate) (PMMA) was spin coated over the original substrate and then immersed in a 1M KOH solution. Slow dissolution of the SiO_2 layer resulted in a free standing PMMA film with MoS_2 crystals adhering to it on the underside. The film was placed in distilled water for several hours to ensure complete removal of KOH prior to the final transfer.

Separately, a *p*-(boron) doped Si (ρ = 0.1 Ω-cm–0.5 Ω-cm) substrate with a 200 nm thermally grown oxide layer was pre-patterned with Au electrodes using standard photolithography and lift off techniques. This substrate was then cleaved through the electrodes, resulting in several sliced Au contacts lining the cleaved edge. The PMMA film described above was carefully fished out of the water using the pre-patterned substrate, making sure that a part of the film reached past the cleaved edge. After drying in air at 90 °C overnight, the substrate was carefully washed in acetone to dissolve the PMMA. This resulted in MoS_2 crystals sticking firmly to the substrate's top and to the freshly exposed cleaved surfaces. Some crystals also lay bent along the cleaved edge, firmly in contact with the Au electrodes above and the *p*-Si below the oxide layer. Figure 1(a) shows a schematic of the device together with the electrical circuit used to characterize it. Figure 1(b) shows a top view scanning electron microscope image of the actual device. MoS_2 crystals are seen lying on the substrate's top surface and along the cleaved edge. Some crystals can also be seen on the sloped section of the cleaved surface, although blurry, as it was difficult to focus at once on the entire substrate. Figure 1(c) shows the Raman spectra of the as grown MoS_2 crystals. The peak separation of 21 cm^{-1} between the in-plane E^1_{2g} and the out-of-plane A_{1g} modes confirmed that the MoS_2 used was of monolayer thickness and of high purity.[17] The IL 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl) imide was used in this work because of its chemical stability and large specific capacitance. The final gate material (IL_{gel}) was prepared by gelation of the IL with the triblock copolymer poly(styrene-b-methyl methacrylate-b-styrene) in dichloromethane, as reported earlier.[18–20] The gel was placed in an oven at 70 °C for several minutes to increase its viscosity via solvent evaporation. This kept it from spreading after being cast on the substrate. A small drop of IL_{gel} was placed at the location of the diode, and a gold wire inserted into the drop served as the gate electrode. Figure 1(d) shows the same substrate as shown in Fig. 1(b) but at a lower magnification and after the IL_{gel} drop was placed over the substrate edge at the location of the diode. External electrical contacts to the device, as seen in Fig. 1(a), were hard wired using silver epoxy prior to electrical characterization. The asymmetric current–voltage (I–V) response confirms the formation of a *p-n* diode at the *p*-Si/MoS_2 interface, as explained later.

Electrical characterization of the diode was performed using a Keithley Model 6517B Electrometer in conjunction with a Keithley Model 2400 Source Meter. All measurements were made in the dark at room temperature and in a vacuum of 10^{-2} Torr to avoid effects of moisture. The IL was electrically characterized using an Agilent Technologies Model 4294A Precision Impedance Analyzer in conjunction with a HP 16453A modified dielectric test fixture.

III. RESULTS AND DISCUSSION

The IL_{gel} was electrically characterized in air prior to testing it in the device. For capacitance measurements, the IL_{gel} was carefully inserted into the space between closely spaced parallel Au electrodes of the test fixture via capillary action, as seen in the lower inset to Fig. 2. Figure 2 shows the IL_{gel} specific capacitance (C_i) as a function of the exciting electric field frequency in the range of 40 Hz–1 MHz. The voltage was fixed at 500 mV. C_i is relatively constant at low frequencies, consistent with previous results,[20] and decreases at high frequencies due to the inability of the heavy ions in the

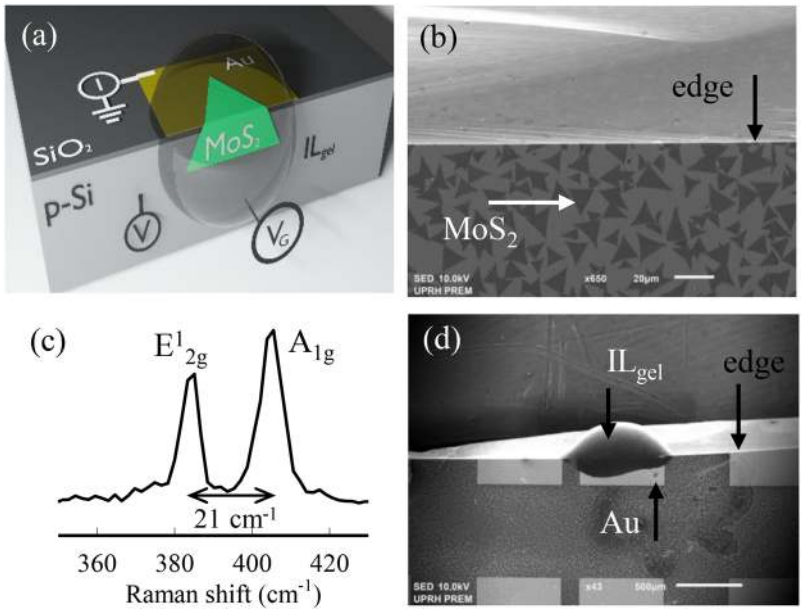

FIG. 1. (a) Schematic of the *p*-Si/MoS_2 diode with external electrical connections. (b) The top view SEM image of the actual diode. The MoS_2 crystals lie on the top surface of the substrate, and several MoS_2 crystals are seen along the cleaved edge. Some MoS_2 crystals can also be seen along the cleaved surface, although blurry due to lack of focus. The white scale bar is 20 μm. (c) The Raman spectrum of MoS_2 showing the characteristic peaks of monolayer crystals. (d) The top view low magnification image of (b) after an IL_{gel} drop is placed at the location of the diode. The white scale bar is 500 μm.

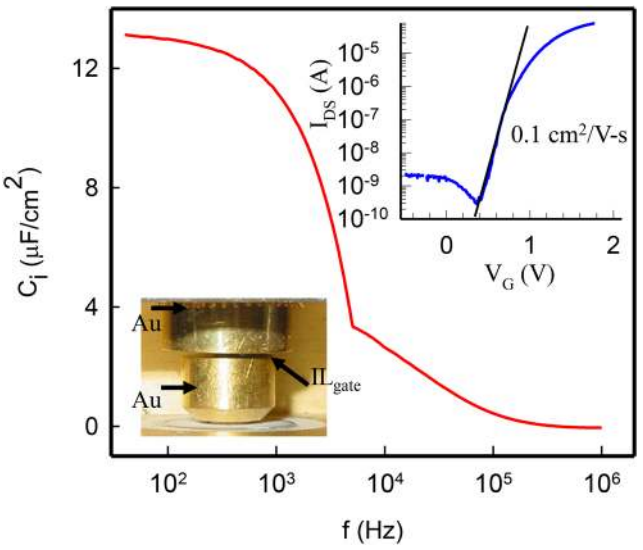

FIG. 2. Specific capacitance (C_i) of the ionic liquid gel (IL_{gel}) as a function of frequency (f). Lower inset: photograph of the IL_{gel} sandwiched between two parallel Au electrodes. Upper inset: drain-source current (I_{DS}) in a monolayer MoS_2 field effect transistor as a function of top gate voltage (V_G). The slope of the straight line was used to calculate the charge mobility (μ). The drain-source voltage (V_{DS}) was fixed at 0.5 V.

IL_{gel} to follow the oscillating electric field. Extrapolating the graph in Fig. 2, we observe that at very low frequencies, C*i* approaches 13 μF/cm^2, which is relatively high due to the formation of nanometer thick electrical double layers at the electrode–ionic liquid gel interface.[21] For comparison, the specific capacitance of a 150 nm thick SiO_2 layer is 20 nF/cm^2.[22] An advantage of using a high C*i* gate material is the large electric field generated by a low applied voltage.

Monolayer MoS_2 has a bandgap of 1.8 eV and exhibits *n*-type conduction.[8,23] This was independently verified by fabricating a MoS_2 field effect transistor (FET) in bottom contact geometry with Au source and drain electrodes and top IL_{gel} gating. The upper inset to Fig. 2 shows the FET trans-conductance curve, i.e., drain-source current (I_{DS}) as a function of gate voltage (V_G) for a fixed drain-source voltage (V_{DS}) on a semi-logarithmic scale. Figure S1(a) (supplementary material) shows the device I_{DS} vs V_{DS} curves for various gate voltages, and Fig. S1(b) shows the device trans-conductance curve using a linear scale, together with the gate leakage current. No reference electrode was inserted into the IL_{gel} for voltage measurements since the leakage current was several orders of magnitude smaller that the MoS_2 channel current. In Figs. S1(a) and S1(b), I_{DS} increased as V_G was made more positive and stayed small and relatively constant when V_G was made more negative. This confirmed *n*-type conduction with accumulation mode transport under a positive gate voltage and depletion mode for voltages below the threshold voltage (~0.3 V).[8] The mobility calculated from the device trans-conductance was ~0.1 cm^2/V-s, and the on/off ratio was ~3 × 10^5. These values were consistent with previous measurements.[16,24] Micro-cracks and/or wrinkles on the MoS_2 surface during the transfer process could be a reason for the low mobility. The linear variation of I_{DS} at low V_{DS} in Fig. S1(a) shows the absence of Schottky barriers, while the symmetric I_{DS}–V_{DS} in the upper inset to Fig. S1(a) confirms Ohmic MoS_2 contacts with the Au source and drain electrodes. In addition, the channel resistance of 5.3 kΩ calculated from the slope of the line in Fig. S1(a) confirmed a low contact resistance between MoS_2 and the Au electrodes.[9] These measurements are presented to support our explanation of the *p*-Si/MoS_2 diode response to a gate voltage.

Figure 3 shows the I–V response curves of the diode, as seen in Fig. 1(d), with V_G = 0 V. Connecting the external power supply's positive terminal to the *p*-Si contact and the negative power supply terminal to the MoS_2 contact of the diode resulted in the blue curve, where the diode was forward biased in the first quadrant and reverse biased in the third quadrant. Reversing the external connections yielded the red curve. These results were consistent with the standard operation of a *p*-*n* diode.[3] The Ohmic and low contact resistance of MoS_2 with the Au electrodes, as discussed earlier, suggested that the non-linear I–V curve in this device arose from the *p*-Si/MoS_2 junction. The observed currents were limited by the series resistances of each material away from the junction. Several diodes were tested with similar asymmetric I–V curves. For this diode, the turn-on voltage was 0.70 V and was determined by extrapolating the linear portion of the I–V curve under forward bias toward the voltage axis at zero current. The turn-on voltage for the other diodes tested with V_G = 0 V is not the same. This could be due to differences

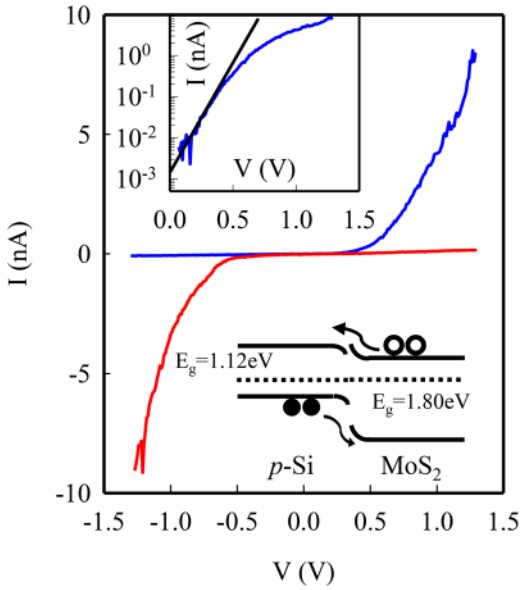

FIG. 3. Current–voltage (I–V) curves of the *p*-Si/MoS_2 diode with no voltage applied to the IL_{gel}. The blue and red curves represent two different external bias conditions, as discussed in the text. **Lower Inset**: the energy band diagram of the *p*-Si/MoS_2 diode in thermal equilibrium. E_g represents the energy bandgap. The dotted line represents the Fermi energy; the energy level above and below the Fermi level corresponds to the conduction and valence band, respectively. The empty circles represent electrons while the filled circles represent holes. **Upper Inset**: the semi-logarithmic plot of the current vs voltage curve under forward bias in the first quadrant. The slope of the straight line prior to diode turn-on was used to determine the ideality parameter.

in the physical contact between p-Si and MoS_2 at the interface for each diode. The ratio of the "on" state current to the "off" state current measured at a bias voltage of ±1.3 V was ~100 for this diode. The asymmetric I–V curve can be qualitatively explained using the band diagram corresponding to the two semiconductors, as shown in the lower inset to Fig. 3. MoS_2 has a bandgap of 1.8 eV[8,23] while for p-Si, it is ~1.12 eV.[1] The relative positions of the valence, conduction, and Fermi energy levels in each semiconductor are indicated in the inset. With no external bias voltage (V) and in thermal equilibrium, electrons (open circles) in MoS_2 diffuse across the junction and recombine with holes (closed circles) in p-Si, creating a depletion zone inside p-Si (since monolayer MoS_2 does not support a depletion region under forward bias[13]). This resulted in band bending inside p-Si that established a constant Fermi level across the junction. As a result, a potential barrier was set up that prevented further diffusion of electrons into p-Si. Externally biasing the diode resulted in the observed I–V curves shown in Fig. 3 as the Fermi levels readjusted in such way that the potential barrier to current across the junction increased (reverse bias) or decreased (forward bias) as V was varied. The I–V curve under forward bias increased exponentially and can be analyzed using the diode equation $I = I_s\left[\exp\left(\frac{eV}{nk_BT}\right) - 1\right]$, where I_s is the reverse saturation current, e is the electronic charge, n is the ideality parameter, k_B is the Boltzmann constant, and T is the temperature.[25] The upper inset to Fig. 3 shows the same data in the forward bias region on a semi-logarithmic plot. Using the slope of the straight line and the equation above, we calculated an ideality parameter of ~3.4 for this diode. Applying a gate voltage retained the asymmetric shape of the I–V curve, but it also led to changes in the diode current and turn-on voltage, as discussed in the next paragraph.

Figures 4(a) and 4(b) show the IL gated diode I–V curves for different gate voltages starting at $V_G = -1.4$ V. At the end of each I–V scan, V_G was increased by +0.1 V successively until $V_G = +1.4$ V. The data plotted in Fig. 4 are split in two panels to better observe the changes in the "on" state current that is measured at V = +2 V. Each panel contains data for a few selected gate voltages, as indicated near each plot. Figures S2(a) and S2(b) show the complete I–V measurements as V_G was changed from −1.4 V → +1.4 V → −1.3 V in steps of 0.1 V and confirmed the reversibility of these results. If the MoS_2 film in the diode was replaced with a drop of silver paint, the I–V curve was symmetric with no significant changes as V_G was varied, as seen in Fig. S3. This strengthens our claim that the p-Si/MoS_2 interface results in a junction diode. Figure S3 also shows that IL gating does not affect charge concentration in p-Si. Two distinct features are visible in Figs. 4(a) and 4(b), and Fig. S2(a). The "on" state currents increase and the diode turn-on voltage decreases as V_G is made more positive. The "off" state current measured at V = −2.0 V was small compared to the "on" state current. The "off" state current for $V_G < 0$ was comparable to the gate leakage current which was typically a few nA. This made it difficult to accurately determine the diode on/off rectification ratio. We therefore focus on the changes in the "on" state current of the diode and the turn-on voltage as V_G is varied.

The insets to Figs. 4(a) and 4(b) show the semiconductor band diagrams under specific applied voltages as indicated, and these help explain the asymmetry of the I–V curves. A comparison can be made to the band diagram shown in the inset to Fig. 3 for energy level identification. The highest recorded "on" state current flows

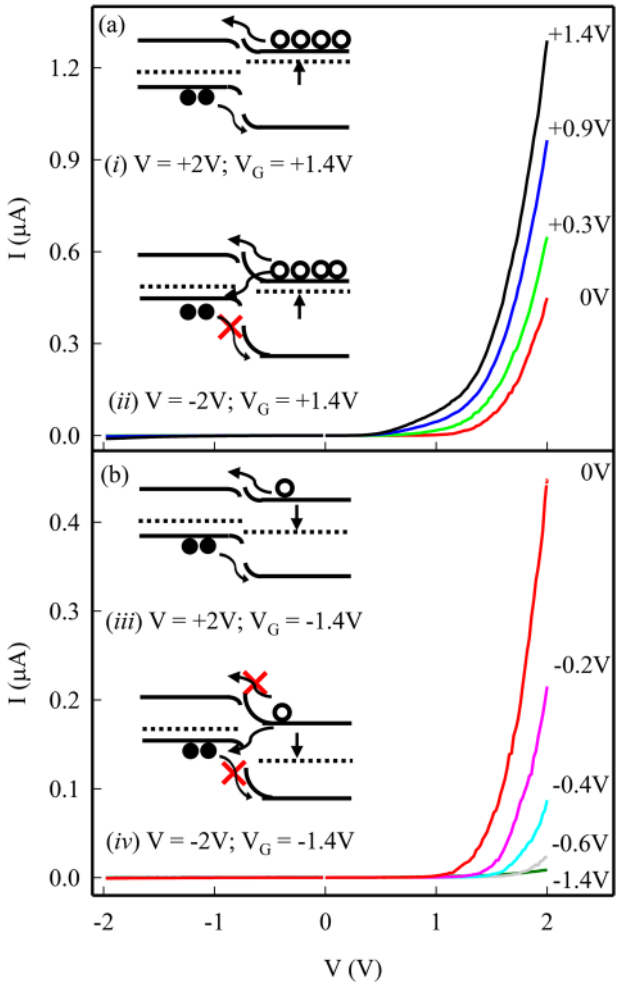

FIG. 4. I–V curves of the diode shown in Fig. 1(b), where the gate voltage was changed from −1.4 V to +1.4 V in steps of 0.1 V and plotted in two panels for clarity: (a) V_G changed from 0 V to +1.4 V, and (b) V_G changed from −1.4 V to 0 V at a few selected gate voltages, as indicated near each curve. The complete run where V_G is changed from −1.4 → +1.4 V → −1.3 V is shown in supplementary section Figs. S2(a) and S2(b). The insets represent the energy band diagram of the p-Si/MoS_2 diode under specific applied voltages as shown.

through the diode when V = +2.0 V and V_G = +1.4 V. Under these conditions, the Fermi level in MoS_2 shifts upward closer to the conduction band, as indicated by the vertical up arrow in inset (i). Electrons are electrostatically induced into the conduction band of MoS_2, resulting in accumulation mode operation. The diode is also forward biased by V, which reduces the potential barrier as seen in this inset figure. Electrons in MoS_2 flow into the conduction band of p-Si, and holes in p-Si flow into the valence band of MoS_2, resulting in a large observed current. When V_G = +1.4 V and V = −2.0 V, as seen in inset (ii), the diode is reverse biased which increases the potential barrier, making it difficult for holes or electrons to flow into the corresponding valence or conduction band, respectively. The current under reverse bias is therefore reduced

even though the positive gate voltage maintains accumulation mode transport in MoS_2. As seen in inset (*ii*), it is possible that electrons in MoS_2 tunnel across the junction and recombine with holes in *p*-Si, with the excess electrons contributing to the observed current at V = −2.0 V, as seen in Fig. 5(c). The barrier for hole transport from *p*-Si into the valence band of MoS_2 is too high, and hole charge transport is unlikely, as indicated with a red X sign. When V_G = −1.4 V, the Fermi level shifts downward toward the center of the band, as seen in inset (*iii*), and MoS_2 operates in the depletion mode. The overall induced electron density in MoS_2 is small so that even under forward bias (V = +2.0 V), the "on" state current is small. The effective barrier is also increased, which results in a larger turn on voltage. Finally, the lowest currents were observed under the reverse bias condition V = −2.0 V and V_G = −1.4 V, as seen in inset (*iv*). The barriers for electron and hole transport into the corresponding conduction and valence bands are too large, forbidding such transport as indicated by the red X signs. Tunneling across the junction could lead to possible electron–hole recombination. The overall measured currents, however, are small under forward or reverse bias and are comparable to the gate leakage current in the nA range.

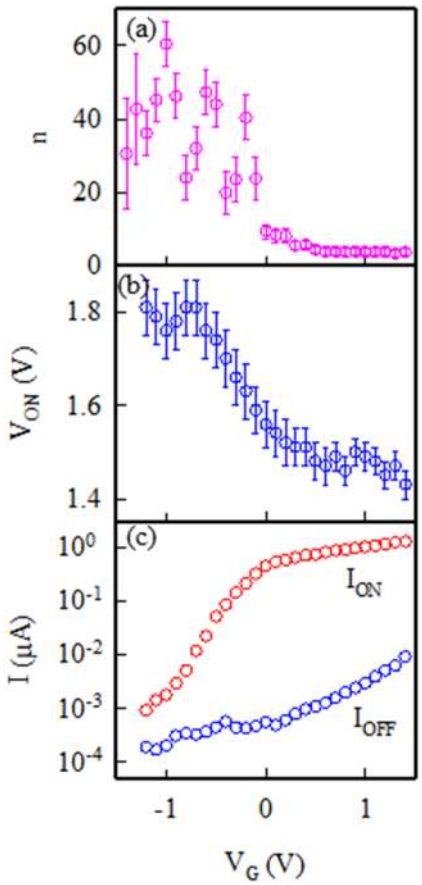

FIG. 5. (a) Diode ideality parameter as a function of V_G. (b) Diode turn-on voltage as a function of V_G. (c) Diode on/off state currents measured at V = +/−2 V, respectively, as a function of V_G.

Figures 4(a) and 4(b), and Fig. S2(a) were further examined using the diode equation to better visualize the effects of V_G on diode performance. Figures 5(a)–5(c) show the ideality parameter, turn-on voltage, and the "on" and "off" currents, respectively, of the diode as a function of V_G. For positive V_G, *n* stays relatively constant at ~3.5, suggesting diode operation that is stable. The diode turn-on voltage decreases while the throughput current increases up to three orders of magnitude as V_G increases. A gate tunable turn-on voltage with high throughput currents (≥~1 μA) also enhances the diode functionality. A noticeable change in the slope is observed for all the curves in Fig. 5 around a threshold voltage of V_G ~ 0 V. Since V_G has no effect on charge transport in *p*-Si, the observed changes arise from the gate control of the charge concentration in MoS_2. It is a change that is most likely associated with the Fermi energy adjustment within the MoS_2 bandgap. Charge transport in MoS_2 shifts from accumulation to depletion mode as V_G is reduced below a certain gate threshold. Once MoS_2 enters the depletion mode, it presents a high series resistance in the diode circuit, resulting in low throughput currents under forward and reverse bias conditions. This leads to large variations in determining the differential current necessary for calculating *n*. In the extreme case, V = −2 V and V_G = −1.4 V, there is a possibility of charge recombination that also leads to an increase in *n*. Above 0 V, however, V_G does control the diode current under forward bias, as seen in Figs. 4(a) and 4(b), and the *n* values are more reliable. This is the first report of electrostatic current control over a wide range and at low operating voltages using IL_{gel} gating in a *p*-Si/MoS_2 diode. A sensor-controlled diode is one application, where the sensing signal is applied to the gate that subsequently enhances, reduces, or completely shuts down diode operation. In addition, the multifunctionality offered by gating could transform the diode into a power saving device by sourcing the optimum current for specific applications.

IV. CONCLUSIONS

We present an easy method of fabricating a *p*-*n* diode using a *p*-Si substrate and *n*-type monolayer MoS_2 crystals. Gating with an ionic liquid gel permitted reversible control of the diode throughput current over several decades while maintaining a relatively constant ideality parameter. The gate voltage adjusts the Fermi energy within the MoS_2 bandgap and controlled the barrier height at the interface with *p*-Si. This consequently lowered the turn-on voltage and increased the current for $V_G > 0$ under forward bias, while suppressing diode operation for $V_G < 0$. Electrostatic current control at low voltages enhances the diodes' functionality, making it useful in other applications besides rectification. The ease of fabrication, low operating voltages (<±2 V), and moderately high throughput currents (~1 μA) are attractive features of this diode, especially for use in sensors and power saving electronics.

SUPPLEMENTARY MATERIAL

See the supplementary material for additional plots of the experimental results.

ACKNOWLEDGMENTS

This work was supported by the National Science Foundation (Grant Nos. DMR-PREM-1523463 and DMR-RUI-1800262).

M.Q.Z., C.W., and A.T.C.J. were supported by the NSF MRSEC (Grant No. DMR-1720530). The authors acknowledge the use of the Raman system supported by the NSF Major Research Instrumentation (Grant No. DMR-0923245). This work was carried out, in part, at the Singh Center for Nanotechnology, a part of the National Nanotechnology Coordinated Infrastructure Program, which is supported by the National Science Foundation (Grant No. NNCI-1542153).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, 1981), Chap. 1.
[2]E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances," Adv. Mater. **24**, 2945 (2012).
[3]D. A. Neamen, *Semiconductor Physics and Devices*, 3rd ed. (McGraw-Hill, 2003), Chap. 8.
[4]B. Oregan and M. Gratzel, "A low cost, high efficicency solar cell based on dye-sensitized colloidal TiO_2 films," Nature **353**, 737 (1991).
[5]S. Nakamura, "The roles of structural imperfections in InGaN-based blue light-emitting diodes and laser diodes," Science **281**, 956 (1998).
[6]J. H. Burroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R. H. Friend, P. L. Burns, and A. B. Holmes, "Light-emitting diodes based on conjugated polymers," Nature **347**, 539 (1990).
[7]K. S. Novoselov, A. Mishchenko, A. Carvalho, and A. H. Castro Neto, "2D materials and van der Waals heterostructures," Science **353**, aac9439 (2016).
[8]R. Ganatra and Q. Zhang, "Few-layer MoS_2: A promising layered semiconductor," ACS Nano **8**, 4074 (2014).
[9]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," Nat. Nanotechnol. **6**, 147 (2011).
[10]G. H. Han, N. J. Kybert, C. H. Naylor, B. S. Lee, J. Ping, J. H. Park, J. Kang, S. Y. Lee, Y. H. Lee, R. Agarwal, and A. T. Charlie Johnson, "Seeded growth of highly crystalline molybdenum disulphide monolayers at controlled locations," Nat. Commun. **6**, 6128 (2015).
[11]D. Jariwala, V. K. Sangwan, C.-C. Wu, P. L. Prabhumirashi, M. L. Geier, T. J. Marks, L. J. Lauhon, and M. C. Hersam, "Gate-tunable carbon nanotube–MoS_2 heterojunction p-n diode," Proc. Natl. Acad. Sci. U. S. A. **110**, 18076 (2013).
[12]Y. Deng, Z. Luo, N. J. Conrad, H. Liu, Y. Gong, S. Najmaei, P. M. Ajayan, J. Lou, X. Xu, and P. D. Ye, "Black phosphorus–monolayer MoS_2 van der Waals heterojunction p–n diode," ACS Nano **8**, 8292 (2014).
[13]C.-H. Lee, G.-H. Lee, A. M. van der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz, J. Guo, J. Hone, and P. Kim, "Atomically thin p–n junctions with van der Waals heterointerfaces," Nat. Nanotechnol. **9**, 676 (2014).
[14]B. W. H. Baugher, H. O. H. Churchill, Y. Yang, and P. Jarillo-Herrero, "Optoelectronics with electrically tunable p–n diodes in a monolayer dichalcogenide," Nat. Nanotechnol. **9**, 262 (2014).
[15]S. Lin, P. Wang, X. Li, Z. Wu, Z. Xu, S. Zhang, and W. Xu, "Gate tunable monolayer MoS_2/InP heterostructure solar cells," Appl. Phys. Lett. **107**, 153904 (2015).
[16]W. Serrano, N. J. Pinto, C. H. Naylor, N. J. Kybert, and A. T. C. Johnson, Jr., "Facile fabrication of a ultraviolet tunable MoS_2/*p*-Si junction diode," Appl. Phys. Lett. **106**, 193504 (2015).
[17]C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, and S. Ryu, "Anomalous lattice vibrations of single and few layer MoS_2," ACS Nano **4**, 2695 (2010).
[18]J. Lee, L. G. Kaake, J. H. Cho, X.-Y. Zhu, T. P. Lodge, and C. D. Frisbie, "Ion gel-gated polymer transistors: Operating mechanism and characterization of gate dielectric capacitance, switching speed and stability," J. Phys. Chem. C **113**, 8972 (2009).
[19]C.-H. Kim and C. D. Frisbie, "Determination of quantum capacitance and band filling potential in graphene transistors with dual electrochemical and field effect gates," J. Phys. Chem. C **118**, 21160 (2014).
[20]D. N. Ortiz and N. J. Pinto, "Ionic liquid gel gated electro-spun poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid) nano-ribbon," Thin Solid Films **636**, 737 (2017).
[21]J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge, and C. Daniel Frisbie, "Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic," Nat. Mater. **7**, 900 (2008).
[22]J. H. Cho, J. Lee, Y. He, B. S. Kim, T. P. Lodge, and C. D. Frisbie, "High-capacitance ion gel gate dielectrics with faster polarization response times for organic thin film transistors," Adv. Mater. **20**, 686 (2008).
[23]K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically thin MoS_2: A new direct-gap semiconductor," Phys. Rev. Lett. **105**, 136805 (2010).
[24]J. Pu, Y. Yomogida, K.-K. liu, L.-J. Li, Y. Iwasa, and T. Takenobu, "Highly flexible MoS_2 thin-film transistors with ion gel dielectrics," Nano Lett. **12**, 4013 (2012).
[25]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, 1981), Chap. 2.