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ORIGINAL ARTICLE

Isolated three-port DC–DC converter employing ESS to obtain voltage balancing capability for bipolar LVDC distribution system

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Abstract
A bipolar low-voltage DC (LVDC) distribution system used in residential and building applications requires AC–DC converters and voltage balancers that balance the two DC bus polarities. The bipolar DC bus voltage level only relies on the voltage balancer tied with the AC grid. An isolated DC–DC converter for an energy storage system (ESS) with the voltage balancing capability is proposed to prevent the bipolar voltage level collapse caused by the failure of the grid-tied voltage balancer. The proposed converter topology is an enhanced three-port dual-active-bridge (DAB) converter which can balance the bipolar DC voltage level without complex control. Furthermore, it has less current stress in power switches than that of the conventional three-port DAB converter. The effectiveness of the proposed converter is verified with a 3-kW prototype converter.

Keywords Bipolar LVDC distribution system · Voltage balancer · Three-port dual-active-bridge (DAB) converter

1 Introduction

DC distribution systems have a variety of attractions compared with the conventional AC distribution systems due to the development of power electronics technologies and the great connectivity of renewable energy sources [1–3]. As digital loads requiring DC power have become the majority in the modern society, low-voltage DC (LVDC) distribution systems are highlighted as a good alternative for residential and building applications. The LVDC distribution system can provide electricity with higher efficiency and less energy conversion stages, no AC resistance in the distribution lines and installation cost reduction [4, 5]. A bipolar LVDC distribution system brings more significant benefits than a unipolar DC distribution system [5, 6]. It gives three different voltage levels, which provides flexibility in connection and high safety with reduced voltage levels according to the ground. In addition, even if faults lie in one of the DC buses, the other can be still operating, which can guarantee the high reliability of the distribution system.

Without a voltage balancer, the bipolar DC buses cannot be kept at the same voltage level under unbalanced load conditions [7–10]. Various voltage balancers connected to the AC grid have been studied to solve the above problem. A simple buck-boost type voltage balancer with a half-bridge cell has been proposed [7]. It has high cost-effectiveness due to the small number of components used. A dual-buck type voltage balancer has been developed to remove the shoot-through issue that the bridge-type voltage balancer suffers from [8]. A three-level voltage balancer has been introduced to withstand high voltage stress for high voltage DC distribution systems [9].

The bipolar DC voltage level of the LVDC distribution system is regulated by the AC grid-tied voltage balancer. If there are failures in the grid-tied voltage balancer, the bipolar voltage level cannot be maintained. Therefore, several back-up voltage balancers are required to improve the system reliability [10]. An ESS charger with the bipolar voltage balancing capability has been proposed [11] as a back-up voltage balancer. It is a version of the improved three-level voltage balancer, which has a small quantity of components; however, it is a non-isolated type. The ESS adopted to the LVDC distribution system is mostly used for residential and building applications, which is highly accessible to people. It can cause a hazard to people who accidentally contact the ESS [6, 12]. Galvanic isolation between the ESS and the grid is recommended for the safety reason as well as

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for protecting operators during their maintenance [12, 13]. Therefore, the above-mentioned voltage balancers are not suitable for the ESS charger applied to the residential and building applications.

A three-port dual-active-bridge converter derived from the DAB converter can be used as a charger [14]. It has a galvanic isolation with a high-frequency transformer and bidirectional power transfer capability that is essential for charger applications. However, it has the power correlation among the three ports due to the cross-coupled loops made by its structure, which makes power unbalance between the two DC buses of the bipolar LVDC distribution system. To overcome the power coupling issue, power decoupling methods have been introduced [14, 15]. This method is implemented by composing a look-up table of decoupling matrices calculated and stored in advance at every operating point. Consequently, it brings high complexity in control.

In this paper, an enhanced three-port DAB converter is proposed with the advantages of the galvanic isolation and the bidirectional power control capability. The proposed converter can overcome the power coupling issue among the ports without any additional control. Therefore, using a simple control algorithm, the converter can regulate the bipolar DC bus voltage levels at the grid-tied voltage balancer failure condition. Furthermore, it has less current stress, which can improve overall power conversion efficiency comparing with the conventional converter. Using the proposed converter, the ESS can balance the bipolar DC voltage level for a longer time with the same amount of energy during the AC grid-tied voltage balancer failure.

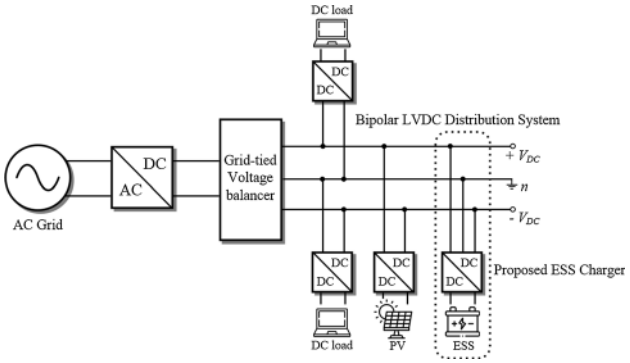

Fig. 1 Conceptual diagram of bipolar LVDC distribution system employing the proposed ESS charger with voltage balancing capability

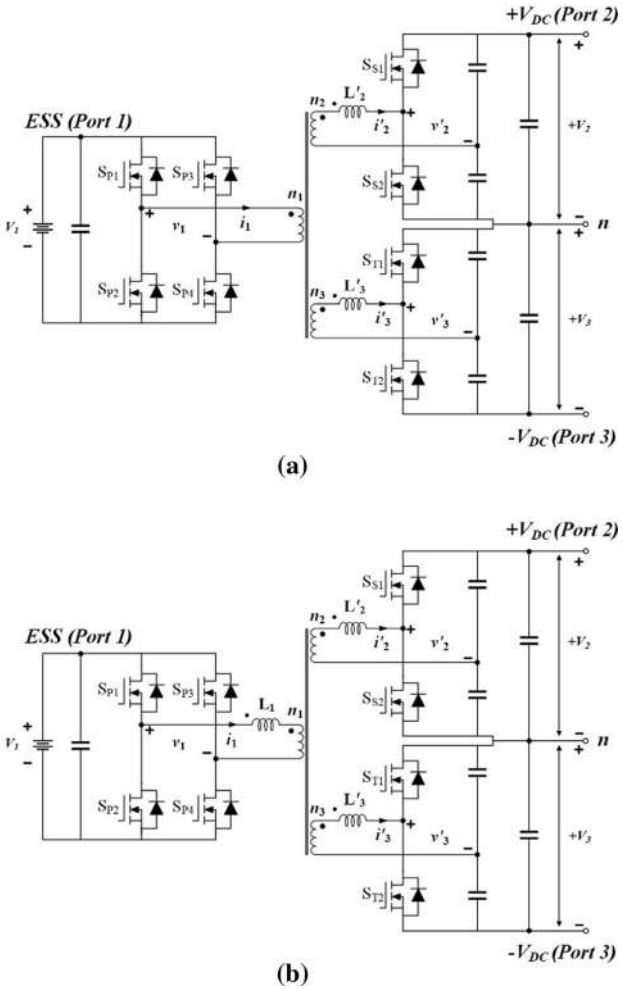

Fig. 2 Converter schematics: **a** the proposed three-port DAB converter with two inductors, **b** the conventional three-port DAB converter with three inductors

2 Analysis of converter structure

2.1 Structure of the proposed converter

Figure 1 shows a bipolar LVDC distribution system with the proposed ESS charger. As previously stated, to keep the same voltage level in both of the DC buses even during the faults of the grid-tied voltage balancer, the ESS must be connected to the DC bus pair. An enhanced three-port DAB converter connected to the bipolar DC bus lines is shown in Fig. 2a. Port 1 is the ESS port, and the other two ports, Port 2 and Port 3 linked in series are attached to the bipolar DC bus lines with the neutral point *n* in the middle.

A full-bridge is applied to the ESS port to cope with the electric power supplied to both the DC buses. A half-bridge is used for each DC bus port as they handle less power than the power that the ESS port takes. The three ports are magnetically coupled by a three-winding transformer. The transformer provides galvanic isolation between the ESS and the grid as well as adjusts voltage difference among the ports. An external power inductor is located at each DC bus port as a power transfer element. The external inductors can be integrated into the transformer, which requires large leakage

inductance. However, it is hard to design such integrated transformers because heat generated by high leakage flux is concentrated on the magnetic core. The external inductors are used in this research for the design simplicity.

The structure difference between the conventional and the proposed converters is the inductor placement as shown in Fig. 2b. The proposed converter has two inductors located in two DC bus ports except the ESS port, whereas the conventional three-port DAB converter has three inductors for every port [14, 15].

2.2 Structure of the proposed converter

The reduced-inductor structure brings the significant benefits stated earlier as the bipolar LVDC voltage balancer. The three-port transformer voltages in the proposed converter are represented as square-wave voltage sources, v_1, v_2' and v_3'. The voltage v_1 is generated by complementarily switching the diagonal switch pairs with 50% duty ratio. The voltage v_2' and v_3' are generated by switching the upper and the lower switches with 50% duty ratio.

Each port is connected to the three-winding transformer in series, which can be described as a wye connection [16]. As it is the extension of the conventional two-port DAB converter, the proposed three-port DAB converter fundamentally has the same power transfer principles determined by the voltage phase displacements of each port through the inductances [14, 15]. A tightly winded transformer has relatively small leakage inductance compared with those of the inductors. Therefore, the inductance of L_1 in the ESS port is negligible.

Delta-connected equivalent circuits are advantageous to analyze the relation between ports in the three-port DAB converter [14, 15]. The delta-connected equivalent circuit with the primary port referred parameters considering the transformer turns ratio can be as depicted in Fig. 3. The effective inductances of L_{12} [$=(L_1L_2+L_1L_3+L_2L_3)/L_3$], L_{13} [$=(L_1L_2+L_1L_3+L_2L_3)/L_2$], and L_{23} [$=(L_1L_2+L_1L_3+L_2L_3)/L_1$)] are derived as power transfer elements between each port. Since there is negligible inductance in the primary port, L_{23}, the effective inductance between Port 2 and Port 3 becomes infinite. It means that the impedance between the two ports is infinite. The proposed converter loses the direct power transfer path between two inductor-connected ports (Port 2 and 3), which is a demerit comparing with the conventional three-port DAB converter; however, power can be still transferred between the two ports by detouring around Port 1.

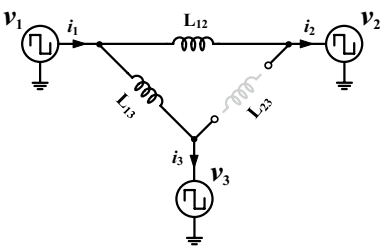

Fig. 3 Simplified delta-connected equivalent circuit of the proposed three-port DAB converter

3 Operational principles

3.1 Voltage balancing operation

The proposed converter can balance the bipolar voltage level by regulating each DC bus voltage since it can independently transfer the electric power to each DC bus without any interference among the ports. The power transfer of the proposed converter is determined by control variables that are the voltage phase shifts with respect to that of v_1. Each port power equation is described as follows [14, 15]:

$$P_{12} = \frac{V_1(0.5n_{12}V_2)}{2\pi^2 f_{sw} L_{12}}\phi_{12}(\pi - |\phi_{12}|) \tag{1}$$

$$P_{13} = \frac{V_1(0.5n_{13}V_3)}{2\pi^2 f_{sw} L_{13}}\phi_{13}(\pi - |\phi_{13}|) \tag{2}$$

$$P_{23} = \frac{(0.5n_{12}V_2)(0.5n_{13}V_3)}{2\pi^2 f_{sw} L_{23}}(\phi_{13} - \phi_{12})(\pi - |\phi_{13} - \phi_{12}|) \tag{3}$$

$$P_1 = P_{12} + P_{13}, \quad P_3 = -P_{13} - P_{23} \tag{4}$$

where P_1, P_2 and P_3 are Port 1, Port 2 and Port 3 power equations, respectively, n_{12} ($=n_1/n_2$) and n_{13} ($=n_1/n_3$) are the transformation turn ratio, V_1, V_2 and V_3 are the voltage magnitudes of each port, f_{sw} is the switching frequency, and ϕ_{12} and ϕ_{13} are the voltage phase shifts of Port 2 and Port 3 with respect to Port 1, which has the range from $-\pi/2$ to $\pi/2$, respectively. If the phase shifts are negative, the power can be transferred to the ESS, which is necessary for a DC–DC charger.

The effective inductance L_{23} is assumed to be infinite in the proposed converter, P_{23} can be considered as always be zero regardless of the control variables ϕ_{12} and ϕ_{13}. Therefore, the Eq. (4) can be simplified as below.

$$P_1 = P_{12} + P_{13}, \quad P_2 = -P_{12}, \quad P_3 = -P_{13} \tag{5}$$

If the system is ideal by ignoring power loss, theoretical operating waveforms can be drawn as Fig. 4. It shows that the voltages applied to the effective inductance network shown in Fig. 3 determine the inductor currents (i_1, i_2 and i_3). Since the current flowing through L_{23} is assumed to be zero, the current

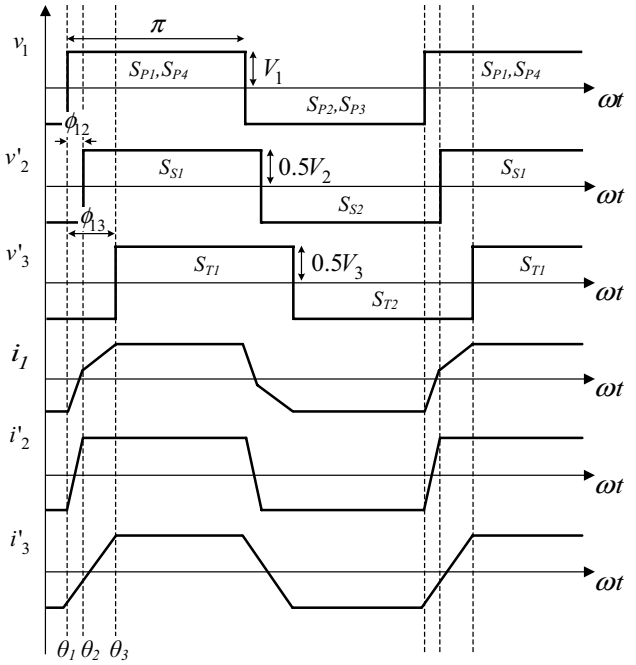

Fig. 4 Theoretical operating waveforms of the proposed three-port DAB converter

i_1 is sum of the current i_2 and i_3. Therefore, the two DC bus ports are seen as connected to the ESS port in parallel.

The proposed converter can independently control the two output voltage levels with a simple control method using two PI controllers. The proposed converter does not have the cross-coupled control loops that can unbalance the bipolar voltage level, which the conventional converter suffers from. It is automatically eliminated by the converter structure. Therefore, the two output voltage levels can be maintained even under different load conditions since the two PI controllers regulate the corresponding DC bus voltage without interference between each DC bus.

The elimination of the cross-coupled control loop can be shown by mathematical approach as follows. If the output voltage levels are assumed to be constant, power can be adjusted by the output currents I_1, I_2 and I_3. The proposed converter has only two control variables of ϕ_{12} and ϕ_{13} to regulate the three port powers. If the power loss is ignored, the sum of the three port power are zero. Therefore, the one port current is automatically determined when other two port currents are controlled by ϕ_{12} and ϕ_{13}. The port currents of I_2 and I_3 can be derived by dividing (1) and (2) according to the corresponding port voltage as follows:

$$I_2 = \frac{V_1}{2\pi^2 f_{sw} L_{12}} \phi_{12} \left(\pi - |\phi_{12}|\right) \tag{6}$$

$$I_3 = \frac{V_1}{2\pi^2 f_{sw} L_{13}} \phi_{13} \left(\pi - |\phi_{13}|\right) \tag{7}$$

The port current equations of (6) and (7) are non-linear, which are difficult to represent the converter operation using linear input–output relations. Therefore, a linearized modeling approach shown in [17] can be applied around its operating points. The linearized model of the proposed converter can be represented as follows:

$$I_2 = \frac{V_1}{2\pi^2 f_{sw} L_{12}} \left(1 - \frac{2}{\pi}\left|\phi_{op12}\right|\right) \phi_{12} \tag{8}$$

$$I_3 = \frac{V_1}{2\pi^2 f_{sw} L_{13}} \left(1 - \frac{2}{\pi}\left|\phi_{op13}\right|\right) \phi_{13} \tag{9}$$

where ϕ_{op12} and ϕ_{op13} are the converter operating points, which can vary from $-\pi/2$ to $\pi/2$ depending on the power, respectively. The linearized proposed converter system matrix can be described as follows:

$$\begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \phi_{12} \\ \phi_{13} \end{bmatrix} = G\vec{\phi} \tag{10}$$

where

$$G_{11} = \frac{V_1}{4\pi^2 f_{sw} L_{12}} \left(1 - \frac{2}{\pi}\left|\phi_{op12}\right|\right) \tag{11}$$

$$G_{22} = \frac{V_1}{4\pi^2 f_{sw} L_{13}} \left(1 - \frac{2}{\pi}\left|\phi_{op13}\right|\right) \tag{12}$$

$$G_{12} = G_{21} = 0 \tag{13}$$

The linearized system matrix G shown in (10) is a diagonal matrix, which shows that the proposed converter can independently control each port voltage level using the corresponding phase shift variables. The balancing control can be achieved by setting the reference voltage phase of the inductor-less port. Otherwise, the off-diagonal elements G_{12} and G_{21} cannot become zero, which brings difficulty in the control of the voltage balancing. Figure 5 shows the proposed converter control diagram of the voltage balancing operation. It only requires the two PI controllers since the coupling elements are removed due to the converter structure. Therefore, the proposed converter has the simple control mechanism to balance the DC bus voltages without additional control methods.

3.2 Current stress reduction

The proposed converter has lower current stress than that of the conventional converter. The reason why the conventional

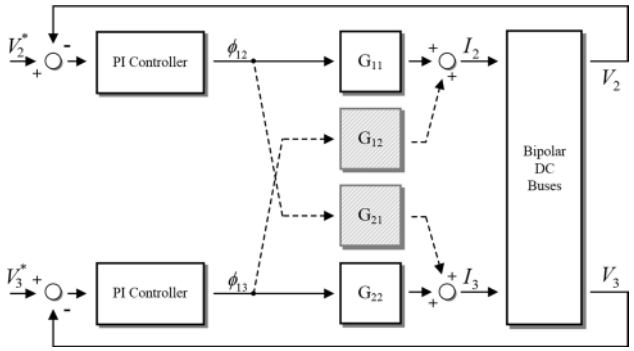

Fig. 5 Control block diagram of the proposed converter with balancing capability for bipolar DC bus voltage levels

converter has high current stress in a power path between Port 2 and Port 3, which does not exist in the proposed converter. It denotes that Port 2 power and Port 3 power are not only determined by their own corresponding voltage phase shift with respect to that of Port 1, but the leakage power also flows through the power path between them by their voltage phase difference. For example, for idling Port 2 at zero power requirement, P12 which is the power supplied from Port 1 to Port 2 has to be the same as P23, which is the power transferring from Port 2 to Port 3. The net power is zero, but high reactive power can be generated, which leads high current stresses in the DAB converters [14, 18].

Lower current rated power switches and magnetic components can be used in the proposed converter. Furthermore, the lower current stress brings the higher overall efficiency in the DAB converters [18, 19]. Therefore, the proposed converter can keep the DC bus voltages balanced for a longer time with the same amount of energy charged in the ESS. The current stress of the proposed converter, which is lower than that of the conventional converter can be derived by the inductor volt-second balance principle as follows [18]:

$$i_2(\theta_1) = -\frac{1}{4f_{sw}L_{12}}\left[(2d_2-1)(0.5n_{12}V_2)+V_1\right] \tag{14}$$

$$i_2(\theta_2) = \frac{1}{4f_{sw}L_{12}}\left[(2d_2-1)V_1+(0.5n_{12}V_2)\right] \tag{15}$$

$$i_2(\theta_3) = \frac{1}{4f_{sw}L_{12}}\left[(2d_3-1)V_1+(1+2d_2-2d_3)(0.5n_{12}V_2)\right] \tag{16}$$

$$i_3(\theta_1) = -\frac{1}{4f_{sw}L_{13}}\left[(2d_3-1)(0.5n_{13}V_3)+V_1\right] \tag{17}$$

$$i_3(\theta_2) = \frac{1}{4f_{sw}L_{13}}\left[(2d_3-2d_2-1)(0.5n_{13}V_3)+(1-2d_2)V_1\right] \tag{18}$$

$$i_3(\theta_3) = \frac{1}{4f_{sw}L_{13}}\left[(2d_3-1)V_1+(0.5n_{12}V_2)\right] \tag{19}$$

where d_2 ($=\phi_{12}/\pi$) and d_3 ($=\phi_{13}/\pi$) is where d_2 ($=\phi_{12}/\pi$) and d_3 ($=\phi_{13}/\pi$) are each DC bus port phase shift duty ratio corresponding to the reference voltage v_1, respectively.

As mentioned earlier, in the proposed converter structure, Port 2 and Port 3 are connected to Port 1 in parallel since there is no link between Port 2 and Port 3. Therefore, Port 1 transformer current is the sum of the other port inductor currents as follows:

$$i_1(\theta_x) = i_2(\theta_x) + i_3(\theta_x) \tag{20}$$

where $x=1$, 2 and 3. The current stress of the proposed converter in each port is defined as the peak current value. In order to simplify the analysis, equivalent voltages and inductances have same values: $V=V_1=0.5n_{12}V_2=0.5n_{13}V_3$, $L=L_2=L_3$ and $L_1=0$. The current stress for each port can be simplified, which appear at angle θ_1.

$$i_{1,\max,pr} = \left|i_1(\theta_1)\right| = \frac{V}{2f_{sw}L}\left(d_2+d_3\right) \tag{21}$$

$$i_{2,\max,pr} = \left|i_2(\theta_1)\right| = \frac{V}{2f_{sw}L}(d_2) \tag{22}$$

$$i_{3,\max,pr} = \left|i_3(\theta_1)\right| = \frac{V}{2f_{sw}L}(d_3) \tag{23}$$

To compare the current stress, the conventional converter current stresses can be derived by using $L_1=L$, which is the same manner above:

$$i_{1,\max,co} = \left|i_1(\theta_1)\right| = \frac{V}{2f_{sw}L}\left[(d_2+d_3)/3\right] \tag{24}$$

$$i_{2,\max,co} = \left|i_2(\theta_2)\right| = \frac{V}{2f_{sw}L}(d_3/3) \tag{25}$$

$$i_{3,\max,co} = \left|i_3(\theta_1)\right| = \frac{V}{2f_{sw}L}\left[(2d_3-d_2)/3\right] \tag{26}$$

In order to normalize the derived values, the normalized coefficients of the derived power and current can be defined as follows:

$$P_N = VI_N = \frac{V^2}{24f_{sw}L} \quad \text{where,} \quad I_N = \frac{V}{24f_{sw}L} \tag{27}$$

Figure 6 shows the comparison of each port current stress in the conventional and proposed converters at $P_3=1.0$ pu with Eqs. (4), (5) and (21–26) divided by P_N and I_N. It clearly shows the proposed converter has lower current stress than that of the conventional converter.

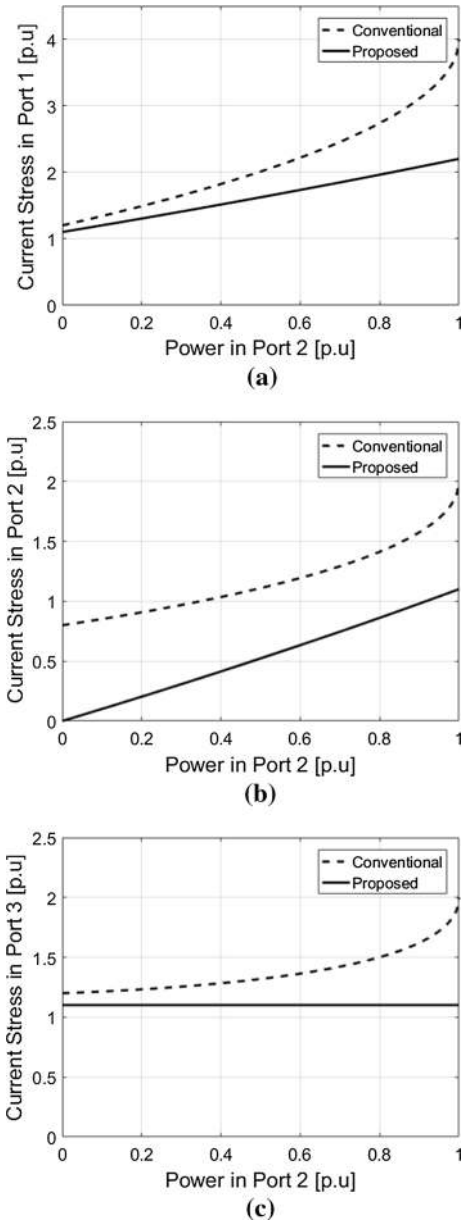

Fig. 6 Current stress comparison between the conventional converter and the proposed converter in each port at $P_3 = 1.0$ pu fixed: **a** Port 1, **b** Port 2, **c** Port 3

4 Experimental results

A 3-kW prototype voltage balancer shown in Fig. 7 is used to obtain experimental results to verify its validity and performance. The converter parameters and specifications are listed in Table 1. MOSFETs used as the power switching devices are installed at the three power bridges of the converter. The three-winding transformer is designed by using an EER6062S ferrite core. The two inductances are designed as the same inductance for the same power transfer capability in both the two DC buses. They are designed with

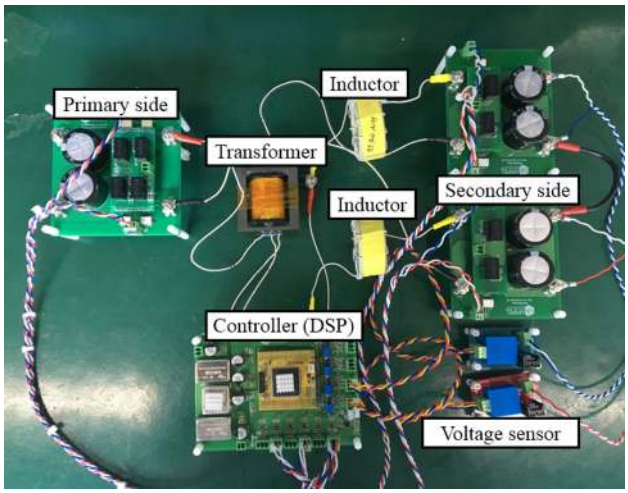

Fig. 7 Photograph of 3-kW prototype proposed converter

external inductors using CH610125 high flux cores. The control strategy is implemented by a TMS320F28335 DSP manufactured by Texas Instruments.

Figure 8 illustrates the steady state operations of the proposed converter to verify the voltage balancing capability. It depicts the proposed voltage balancer can balance the bipolar DC voltage level under both balanced and unbalanced load conditions. It can be achieved by individually transferring power to each bus with their corresponding voltage phase shifts of ϕ_{12} and ϕ_{13}. Figure 8a shows the steady state operating waveforms under the balanced full load condition supplying 1.5 kW for both the DC buses. The bipolar DC bus voltage levels of V_2 and V_3 are regulated to 380 V with around 20° of the voltage phase shifts of ϕ_{12} and ϕ_{13}. In Fig. 8b, one DC bus (Port 2) operates under the full load condition while the other DC bus (Port 3) is under the no load condition. The bipolar DC bus voltage levels are still balanced at 380 V. The phase shift of Port 2, ϕ_{12}, is 20° as same as the one in Fig. 8a, however, the other voltage phase

Table 1 Prototype converter specifications and parameters

Parameter	Symbol	Value (description)
Rated power	–	3 kW
Power MOSFET	–	IPW65R041
ESS voltage	V_1	200 V
Bipolar bus voltage	V_2	380 V
	V_3	380 V
Transformer turns ratio	n_{12} (n_1/n_2)	1
	n_{13} (n_1/n_3)	1
Power inductor	L_2'	33.7 μH
	L_3'	32.6 μH
Switching frequency	f_{sw}	25 kHz

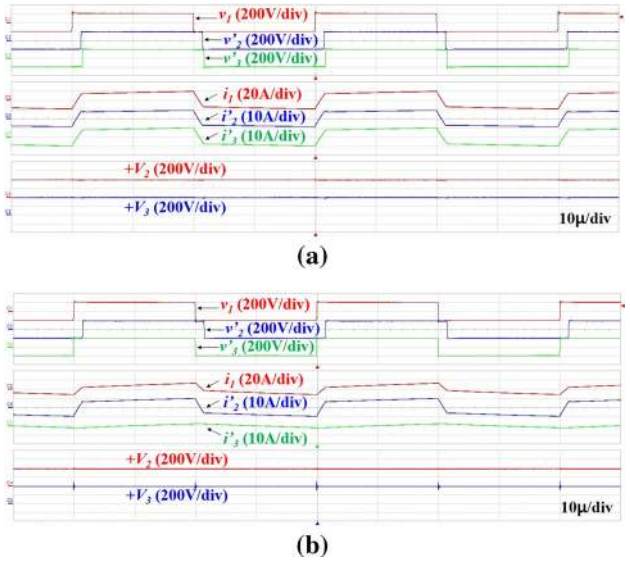

Fig. 8 Steady state experimental operating waveforms under **a** 3 kW ($P_2 = 1.5$ kW, $P_3 = 1.5$ kW), **b** 1.5 kW ($P_2 = 1.5$ kW, $P_3 = 0$ W)

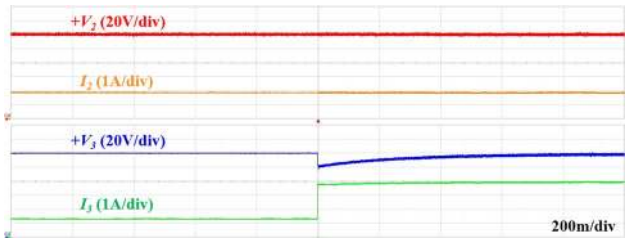

Fig. 9 Dynamic response experimental waveforms ($P_2 = 750$ W and $P_3 = 500$ W to 1.5 kW)

shift of Port 3, ϕ_{13}, is in phase (0°) with the reference voltage phase. Since the converter separately regulates the two bipolar DC buses, only ϕ_{13} is changed under the unbalance load condition.

Figure 9 shows the experimental waveforms of the dynamic response in the proposed voltage balancer. Port 3 power changes from 500 W to 1.5 kW while Port 2 keeps the output power to 750 W. Port 3 balances its bus voltage to 380 V with 200 ms settling time and Port 2 well sustains the same voltage level even under the load step-changes in Port 3. Consequently, there is no interference of the voltage regulation performance between the two DC buses. The step load response shows that the power change in one port does not influence the other port in power control manner. In other words, the two bipolar DC buses are effectively decoupled without any additional controls in the proposed voltage balancer.

Figure 10 shows the steady state operating waveforms of the proposed converter to compare the current stress between the conventional and proposed converters. In Fig. 10a, the

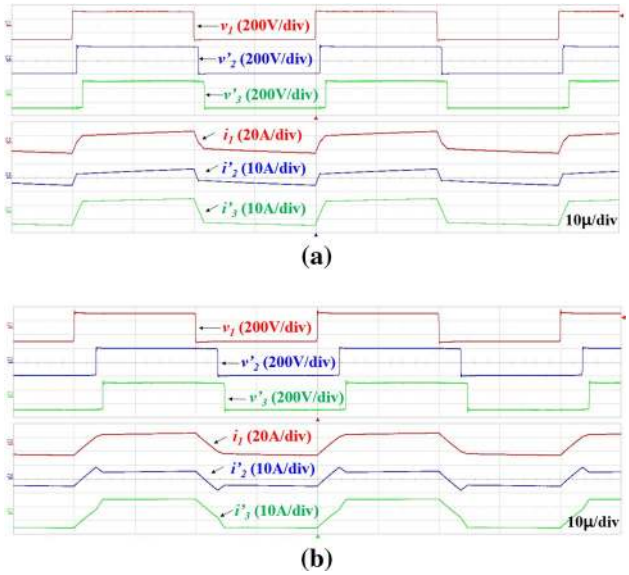

Fig. 10 Steady state operating waveforms under the power conditions of $P_2 = 750$ W and $P_3 = 1.5$ kW (**a**) in the proposed converter (**b**) in the conventional converter

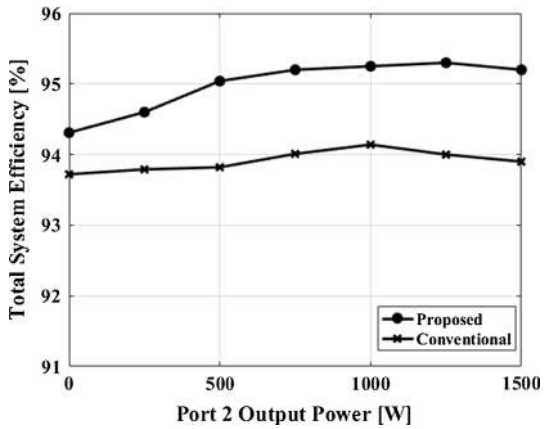

Fig. 11 Efficiency curves according to output power changes at Port 2 (Fixed $P_3 = 1.5$ kW)

peak current for each port is $i_{1,\max} = 15.6$ A, $i_{2,\max} = 5.9$ A and $i_{3,\max} = 9.5$ A, respectively, in the proposed converter. The conventional converter shows the peak current for each port of $i_{1,\max} = 16.7$ A, $i_{2,\max} = 8.5$ A and $i_{3,\max} = 10.5$ A, respectively, which are shown in Fig. 10b. The current stresses are reduced by 6.6%, 30.6% and 10.5% in Port 1, Port 2 and Port 3, respectively. The difference of the peak current comes from the leakage path constructed by L_{23} located in the conventional converter. It generates more reactive power than the proposed converter because of the additional leakage path.

Figure 11 illustrates the efficiency curves of the conventional and proposed converters according to output power

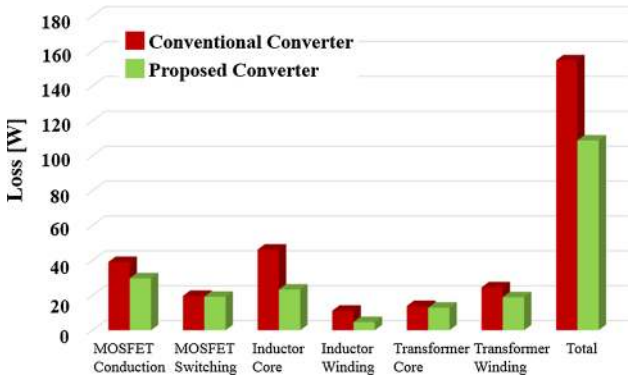

Fig. 12 Power loss breakdown comparison at full load condition

variations at Port 2 with a fixed power of 1.5 kW at Port 3. The proposed converter shows higher efficiency according to all the load ranges than that of the conventional converter due to the lower current stress and the smaller number of power transfer inductors. The proposed converter has more than 94% efficiency over entire load ranges. The biggest efficiency difference between the proposed and conventional converters is 1.4% at 1250 W in Port 2.

The efficiency difference is as shown in Fig. 12. The estimated total loss difference is 45.94 W, which is 1.5% power conversion difference. As the proposed converter has lower loss than that of the conventional converter, it has 9.38-W lower MOSFET conduction loss, 6.48-W lower inductor and 5.68-W lower transformer winding loss. In addition, it has 22.87-W lower core loss because it does not have a power inductor in Port 1 that handles two DC bus powers. As a result, the efficiency difference between the two converter mainly comes from lower conduction and core losses.

5 Conclusions

In this paper, a three-port DAB converter using two inductors is proposed as the voltage balancer for the bipolar DC bus system. The converter structure and operational principles have been explained. The benefits of the proposed converter, which are the simple control for the voltage balancing and the low current stress, are theoretically analyzed and discussed. In the experimental results, the bipolar voltage level is well balanced to 380 V under various load conditions. The dynamic response shows that Port 3 balances its pole voltage level to 380 V during the step load change while Port 2 voltage is balanced without any changes. In the current stress comparison, the largest reduction of the current stress is 30.6% in the proposed converter. Consequently, the proposed converter shows higher efficiency due to less current stress and only two inductors comparing with the conventional converter. The efficiency is 0.6% and 1.4% higher than those of the conventional converter at the low and high load conditions, respectively. The higher efficiency comes from lower current stress and the smaller number of inductors. The proposed converter has more than 94% power conversion efficiency over the entire load ranges. As a result, the proposed converter can be used as the voltage balancer employing the ESS with its multi-port function to back-up the main voltage balancer failures.

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