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Isotropic silicon etch characteristics in a purely inductively coupled SF_6 plasma

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The characteristics of isotropic etching of silicon in a purely inductively coupled SF_6 plasma are quantitatively studied. Since the etch results are strongly dependent on mask features, the authors investigated both large area and narrow trench etch characteristics. Circles of diameter 500 μm were used as a proxy for unpatterned surfaces and etched for different durations to establish the material etch rate and surface roughness. The average etch rate using the chosen recipe was found to be 2.27 μm/min. Arrays of narrow trenches ranging from 8 to 28 μm were also etched to analyze the effect of trench size on etch rate and degree of anisotropy. The etch rate of the trenches was found to strongly decrease with decreasing trench width. The results demonstrate that isotropic SF_6 etch can be readily used as a replacement for more exotic silicon vapor phase etch chemistries such as XeF_2. *Published by the AVS.* https://doi.org/10.1116/1.5116021

I. INTRODUCTION

A. Semiconductor etching

Etching is an integral component of microfabrication and nanofabrication processing, and is therefore attracting considerable attention in the semiconductor industry. As the scope of etching can be vast, ranging from the removal of entire layers from wafers to the etching of submicrometer features with high precision, developing an etching technique that is appropriate for the application is crucial. Specifically, dry etching methods have been extensively studied because of the rapidly reducing node sizes of semiconductor components. Initially developed to remove organic residue and for "ashing" photoresists,[1] dry etching techniques such as reactive ion etching (RIE) can be used to achieve very high selectivity (provided that the etching chemistry and the process parameters are well chosen). Such techniques can also be engineered to achieve the desired level of anisotropy, therefore enabling the fabrication of high aspect ratio trenches[1] and pillars.[2]

Isotropic etches, essential for removing sacrificial layers, releasing MEMS structures and isolating membranes, have been conventionally realized through wet etching techniques, using chemicals such as HNO_3:H_2O:NH_4F or KOH (Ref. 3) (to etch silicon) and HF (to etch silica). However, this approach can lead to problems as the surface tension of the wet etchants can damage delicate structures and membranes. Alternatively, vapor phase etching can be used to overcome the problems associated with wet etching. As in the case with wet etching, the etch is completely chemical in nature, and without a physical component, usually resulting in isotropic etch profiles. As the etching occurs in the vapor state, and the etchants react with the substrate readily, the etch takes place without the need to generate a plasma. Vapor phase etching of silicon can be performed using chemicals like xenon difluoride (XeF_2), bromine trifluoride (BrF_3), and chlorine trifluoride (ClF_3).[4,5] Since its synthesis in 1962,[6–8] and subsequent development as an isotropic etchant,[9] XeF_2 has been widely used as a vapor phase etchant, as it is highly selective to silicon with respect to aluminum, photoresist, and silica. Similarly, silica has been selectively etched using a similar process using HF vapor.

One unintended consequence of using the XeF_2 etch is that it reacts with moisture, forming HF, which in turn etches SiO_2.[10] This may lead to selectivity issues when using a silica mask . It also requires specialized equipment, and it is not integrated into conventional CMOS processes. Furthermore, both the equipment required for the etch and the chemical itself are niche and somewhat expensive, making the process less economically viable. To remedy this, alternative approaches using plasma etching have been explored, as described in Sec. I B.

B. The SF_6 isotropic inductively coupled plasma etch

It has been well established that silicon readily etches in fluorine-based gases and plasmas,[11] with chemical etching in these materials leading to large undercuts.[12] The exact chemical reaction that takes place during the etching process of silicon with fluorinated plasma is still not completely understood and is the subject of some debate.[13,14] As the F atoms are formed in the plasma by electron impact dissociations, they react with the surface silicon to form SiF_4. However, significant amounts of SiF_2 and SiF_3 are produced as primary and subsequent etch products. Though several fluorinated gases such as tetrafluoromethane (CF_4), fluoroform (CHF_3), ammonia (NF_3), boron trifluoride (BF_3), etc., have been used, sulfur hexafluoride (SF_6) is particularly useful, owing to its superior etch rate and inert nature.[15] SF_6 also does not contain carbon and hydrogen atoms, therefore having the advantage of not producing hydrocarbon by-products. By adjusting plasma etch parameters a high

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degree of isotropy can be achieved, along with other desirable properties such as selectivity. This is done by only applying an inductively coupled excitation in an inductively coupled plasma (ICP)-RIE etching chamber (i.e., setting the capacitive RF excitation to zero). Removal of the capacitive excitation avoids accelerated ions impacting on the substrate, since in an ICP-RIE system the inductive ionization of the gas takes place azimuthally and away from the substrate (Fig. 1). The possibility of generating a high density plasma without high ion energy can be an attractive proposition, as lower ion energy increases etch isotropy, improves the physical etch selectivity and also reduces the damage to the substrate caused by ion bombardment.

SF_6 plasma etching in an ICP-RIE reactor is also an effective method for the isotropic etching of silicon due to the higher density of radicals, as the radicals are responsible for the bulk of the etch. This particular etch is one part of the two step Bosch process, which involves consecutive steps of isotropic etching and passivation.[16,17] The Bosch process was developed to combine the advantages of the pure SF_6 ICP etch (high etch rates) while also achieving anisotropy and vertical sidewalls. In contrast, we investigate the utility and the characteristics of the ICP SF_6 etch in the isotropic etching of silicon.

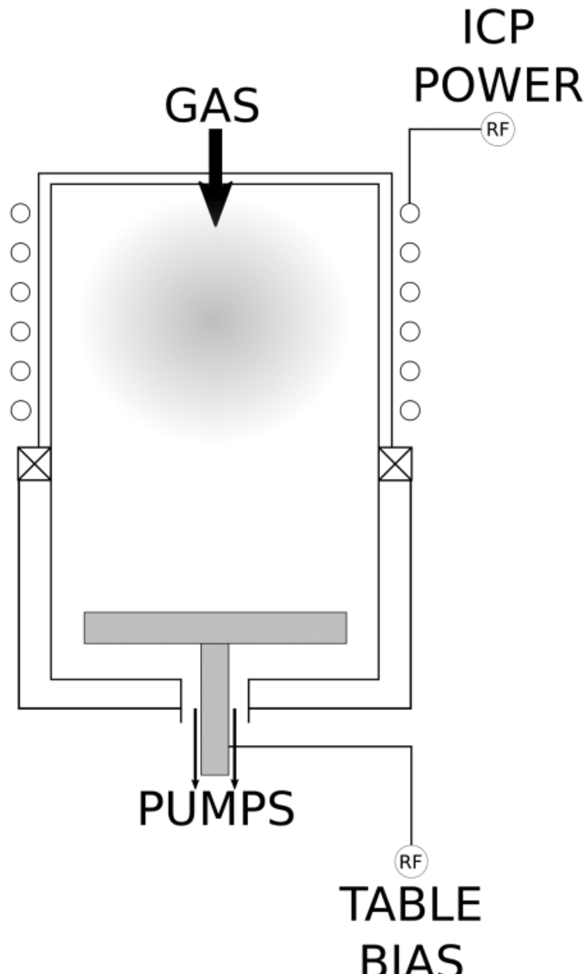

FIG. 1. Schematic layout of a generic ICP-RIE reactor.

C. Isotropic etching in photonic device fabrication

Etching, in general, plays a very important role in the fabrication of photonic devices. For example, anisotropic etching is crucial in creating the vertical and smooth sidewalls of waveguide structures.[18,19] Wet isotropic etching has been used not only to remove entire layers but also for the controlled removal of material. For example, HCl has been used to etch InP in the fabrication of photonic lasers,[20,21] and HF has been used as a wet etchant for the controlled removal of silica during the fabrication of pedestal waveguides.[22] As mentioned earlier, XeF_2 is a popular dry isotropic silicon etchant and has been used for the fabrication of silica microtoroid resonators.[23] We have earlier demonstrated the use of SF_6 isotropic etching to form suspended nanocrystalline diamond waveguides.[24]

Isotropic etching in SF_6 and a comparison of different fluorine-based etchants and their etch rates[15] have been reported. While the SF_6 isotropic etch has been investigated in regard to surface roughness in the presence of polymer masks[25] and for applications such as creating microlenses,[26] basic data on the effect of aperture size on the etch characteristics does not seem to be readily available. Given this, we have conducted a set of etching experiments on patterned and unpatterned silicon substrates in order to investigate the effect of mask feature size on the etch rate. We have also avoided the use of polymer masks, which may contribute to additional etch roughness, as pointed out in Larsen *et al.*[25] Note that the aim of this study is not to determine the effects of different etching parameters, but rather to better understand the etch characteristics, having arrived at a suitable recipe. Earlier studies have presented the ideal etching parameters for achieving the highest etch rates for bulk crystalline silicon substrates (unpatterned). We have found the behavior of these etches to be radically different for patterned substrates, with strong dependency on the pattern features and the substrate size.

II. EXPERIMENTAL METHODS

In order to quantify the etch itself, parameters such as etch rate, surface roughness, and anisotropy have to be considered. Anisotropy, which is the preferential removal of material in a specific direction, becomes a critical parameter, especially in the context of anisotropic etching of patterns. In KOH wet etching, anisotropy is achieved as a result of difference in etch rates due to the crystalline orientation. However, in dry etching, anisotropy is achieved because of preferential etching in the vertical direction due to ion bombardment or formation of inhibitors on the sidewalls to protect them. The penetration of the etchants as well as the mass removal of the etched by-products also has an affect on the anisotropy. Since the focus of this study is the isotropic etching of silicon, it is important to define an appropriate quantitative metric for isotropy. The degree of isotropy (I) can be defined as

$$I = \frac{H}{V}, \quad (1)$$

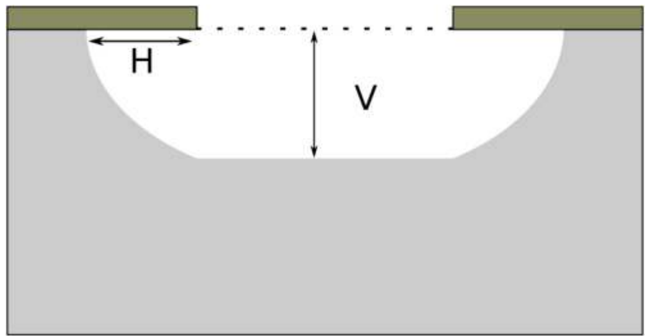

FIG. 2. Schematic of the definition of isotropy used, showing the location of the H and V measurements.

where H is the etch depth in the horizontal direction and V is the etch in the vertical direction (Fig. 2). Therefore, complete isotropic etches have $I = 1$, and complete vertical etches have $I = 0$.

A. Sample preparation

Thermally oxidized 4 in. silicon wafers with the oxide thickness of 290 nm were used to prepare the samples for this study. They were then diced into squares of approximately $1 \times 1\,\text{cm}^2$. All the samples were cleaned using the standard degrease cleaning process, which consists of 5 min of ultrasonic agitation in methanol, acetone, and isopropanol, followed by rinsing in flowing DI water for 2 min. The samples were then dried using a nitrogen gun. The final step was a 10 min dehydration bake at 250 °C in order to remove all the moisture from the substrate.

A 100 nm thick layer of chromium was deposited on the samples through sputtering (Fig. 3) for additional protection of the oxide mask. The etch rate and selectivity of thermal oxide to silicon was found to be 19.7 nm/min and 115:1, respectively. This etch rate predicted nearly complete erosion of the 290 nm oxide for some of the longer etch tests. To avoid this and to have a consistent set of samples, all chips were, therefore, coated with the chromium layer. The reason for choosing chromium-on-oxide over chromium as the mask material was that we found that the chromium layer on its own tends to sag or collapse during long isotropic etches (Fig. 4). The samples ($1 \times 1\,\text{cm}^2$ chips) were then spin coated with AZ-1505 photoresist and patterned using optical lithography using two sets of patterns. Pattern 1 consists of eight circles of diameter 500 μm arranged diagonally across the chip with a 990 μm gap separating them. Pattern 2 consists of four sets of lines, 1 cm in length. Each set is made up of individual lines ranging from 8 to 28 μm, the lines were separated by a distance of 200 μm. The patterns were then transferred to the chromium layer using a commercially available etchant (CR-7). Finally, buffered oxide etchant was used to etch the oxide layer in order to reveal the silicon layer underneath.

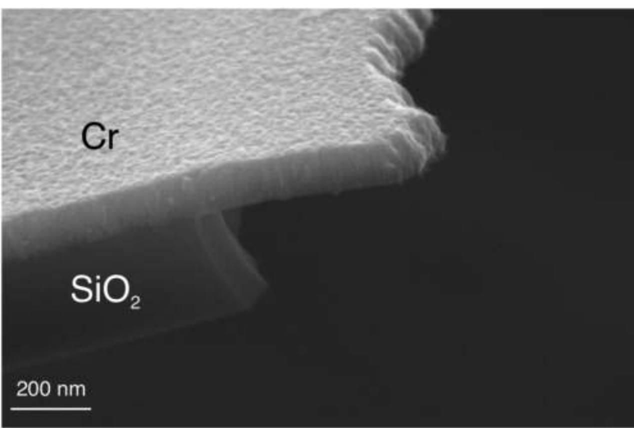

FIG. 3. Suspended edge of the chromium on silica mask, after isotropic removal of the underlying silicon in the SF_6 plasma. The undercut of the silica layer is due to the wet buffered oxide etching during the mask patterning step.

B. Experimental setup

The study was conducted in three parts:

- Part 1: This was conducted to measure the etch rate of the process in large area circles without the constraints of aspect ratio, micromasking and other etching phenomena that are dependent on the features, sample size, etc. Due to the relatively large size of the circles (500 μm), the etch rate and roughness at the center of the features can be approximately viewed as the etch rate of unpatterned silicon. All the samples were placed in similar areas of the chamber on a 4 in. silicon carrier wafer to ensure that loading and position effects are mitigated.
- Part 2: This part of the study was designed to investigate the effect of feature size on the etch. Samples patterned with the series of lines were chosen for this experiment and were etched for times ranging from 30 s to 15 min, resulting in semicircular or semiovoid channels (Fig. 5). As in part 1, the chips were placed in the same part of the chamber on a 4 in. silicon carrier wafer.
- Part 3: This was conducted to obtain the etch rate of the process without the balancing effect of the carrier wafer. Samples patterned with the circles were placed directly on a stainless steel carrier and etched without the presence of the silicon wafer. The reduced area of exposed silicon has a considerable effect on the etch rates.

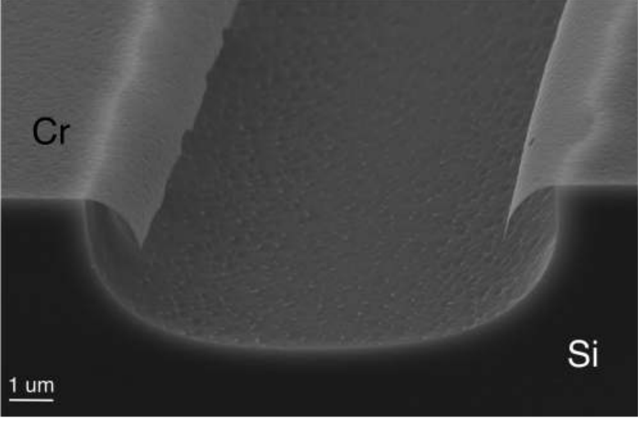

FIG. 4. Sag of the unsupported chromium mask layer during undercut.

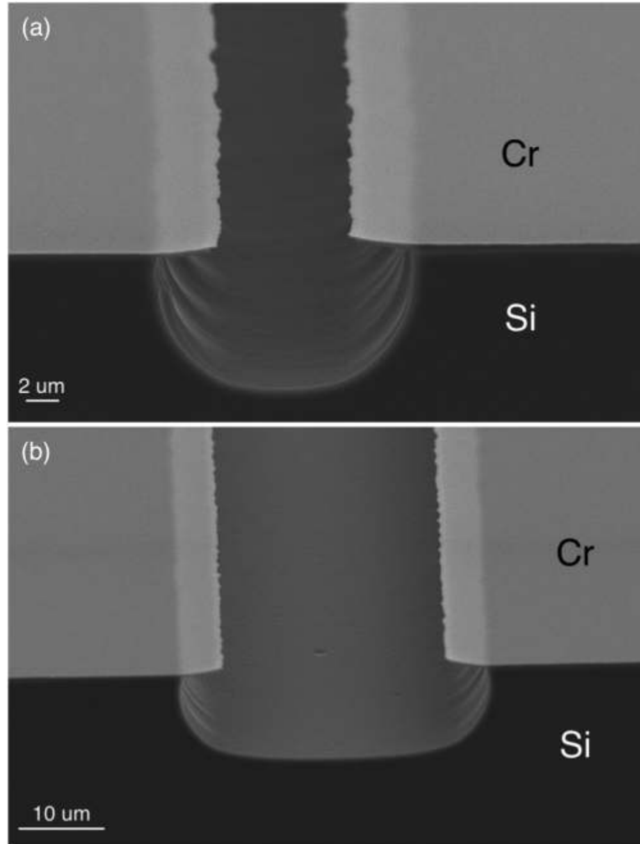

FIG. 5. SEM images of the (a) 8 and (b) 28 μ m lines after the isotropic etch (5 min).

All of the samples were etched using the same recipe in the same ICP-RIE system, an Oxford Instruments PlasmaPro 100 Cobra300. The chamber pressure was set to 30 mT, and the substrate temperature was set to 20 °C. The ICP power was 2000 W with a bias of 0 V. Finally, the SF_6 flow rate was set to 50 SCCM. The samples were fixed to the surface using a Teflon tape on the edges.

The width and depth of all the features were measured before the isotropic etch using a Bruker Dektak profilometer. After the etches were performed, the chromium and the oxide layers were completely stripped to reveal the entire silicon layer. The features were measured once again to obtain the postetch dimensions. The surface roughness measurements reported were conducted using a Veeco Atomic Force Microscope.

III. RESULTS AND ANALYSIS

The results from Part 1 of the study are tabulated in Table I and illustrated in Fig. 6. The etch rates are found to be in the range of 2.07 to 2.47 μm/min. This is similar to etch rates achieved through the conventional dry isotropic etching of silicon, i.e., the vapor phase etching using XeF_2.[27] Though higher etch rates around 10 μm/min have been reported,[10] the typical etch rates range from 1 to 3 μm/min.[27]

The surface roughness of the etch is presented in Table II. It is evident that against the baseline roughness of the silicon

TABLE I. Etch rates of the 500 μm circles.

Sample	Etch depth (nm)	Time (min)	Etch rate (nm/min)
Circle 1	4 399	2	2199
Circle 2	9 085	4	2271
Circle 3	12 474	6	2079
Circle 4	18 141	8	2267
Circle 5	21 461	10	2146
Circle 6	37 111	15	2474

(<1 nm), the roughness initially rises. However, from the initial high, it slowly reduces with time, reaching its minimum value at 4 min, before increasing again. From the AFM scans of the etch (Fig. 7), it can be seen that the initial roughness is evenly spread features with small amplitude. As the etch time increases, areas of these features consolidate into larger and smoother "scallops" of larger amplitude. The roughness associated with this etch is expected, due to its chemical nature, and can be undesirable in an optical context, for example, leading to scattering.

Figure 6 also presents the etch rate obtained without the balancing effect of the carrier wafer and shows that the etch rate without the presence of a silicon wafer is much higher than that seen in Part 1. This is a loading effect due to the decrease in the exposed silicon area. Though this offers higher etch rates, the presence of the wafer will ensure that the etch process is well defined and controllable, as the features on the chips will have a smaller overall impact on the etch.

In Part 2 of the study, the focus is on the effect of the feature geometry on parameters such as lag, aspect ratio dependent etching, and isotropy. The vertical etch rates are

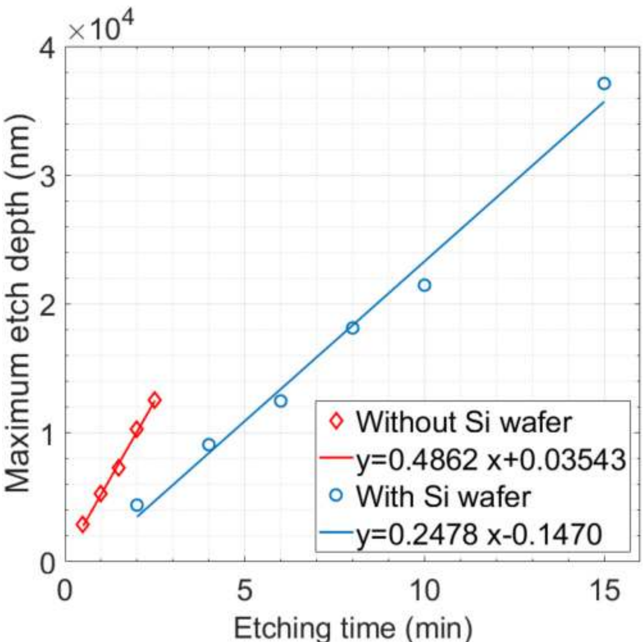

FIG. 6. Etch depth vs etch time with and without silicon carrier.

TABLE II. Surface roughness vs time.

Sample	Time (min)	RMS roughness (nm)
Circle 1	2	22.04
Circle 2	4	8.39
Circle 3	6	15.25
Circle 4	8	13.01
Circle 5	10	24.64
Circle 6	15	25.26

presented in Fig. 8, and the etch depth in the center of the feature is shown in Fig. 9. The etch rates range from 1.3 to 2.6 μm/min, and as expected, the etch rate increases with the linewidth, due to the increase in the flux entering and exiting the trench. As the etch time increases, the aspect ratio of the trench also increases, and it was found that the etch rate at the bottom of the features is much slower than the etch rate at the surface. This is due to the phenomenon generally referred to as "aspect ratio dependant etching" or "RIE lag". The etch rate (ER) at any point is given by[28]

$$ER_{total} = ER_{thermal} + ER_{physical} + ER_{ion}. \tag{2}$$

Since this etch is completely chemical, $ER_{physical} = ER_{ion} = 0$. Therefore, the total etch rate is equal to $ER_{thermal}$, which is the etch rate due to the spontaneous etching of silicon by fluorine atoms in the absence of ion bombardment and is given by[28]

$$ER_{thermal} = k_0 \cdot Q_F \cdot \exp\left(\frac{-E_a}{k_b T}\right), \tag{3}$$

where k_0 and k_b are constants, Q_F is the flux of the fluorine atoms, E_a is the activation energy, and T is the absolute temperature. Therefore, at constant temperature, the etch rate is directly proportional to Q_F. The etch rate at the bottom of a trench can be calculated using the following equation:

$$ER_{bottom} = \frac{Q_{F(bottom)}}{Q_{F(top)}} \times ER_{top}. \tag{4}$$

The relevant mechanisms that govern the flux at the bottom (in a completely chemical etch with bias = 0, i.e., no energy and ionic component to the etch) are[29]

1. transport of neutrals,
2. neutral shadowing,
3. surface diffusion, and
4. bulk diffusion.

At the pressure level reported in this study, the mean free path of the particles (l) is in the range of millimeters, whereas the feature dimensions (d) are in the micrometer range. Therefore, the Knudsen number ($Kn = l/d$) is larger than 1, indicating that particle-particle interactions are rare and can be ignored.

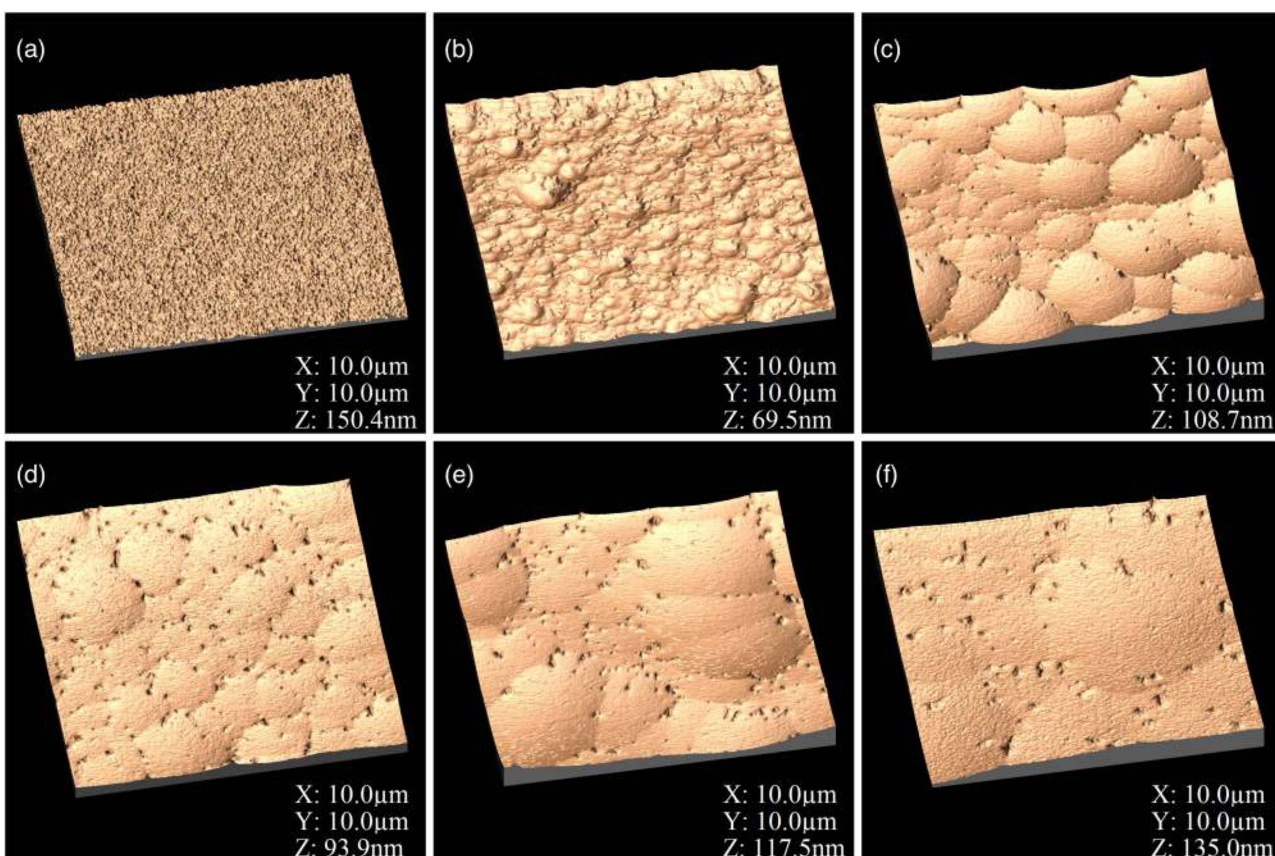

FIG. 7. AFM scans of the surface roughness for etch times of 2, 4, 6, 8, 10, and 15 min, respectively. "Z" is the maximum peak to valley measurement.

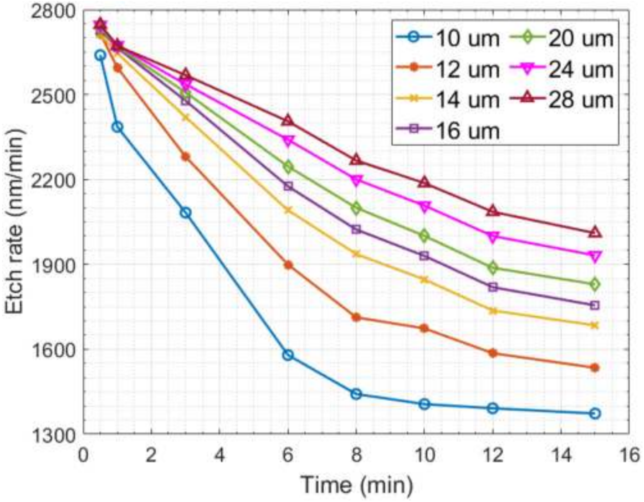

FIG. 8. Maximum etch rate vs etch time for pattern set 2.

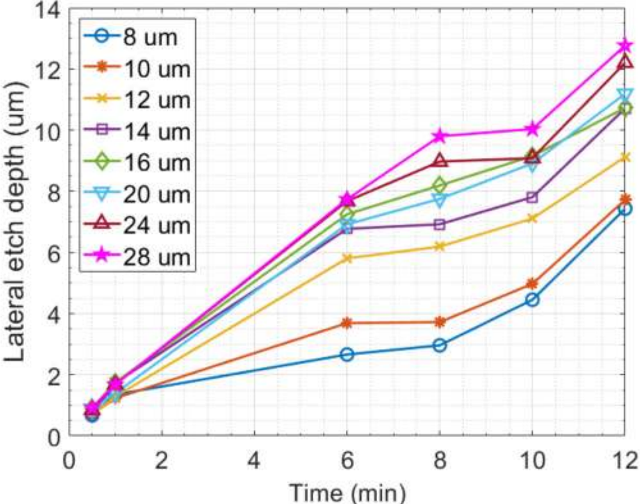

FIG. 10. Lateral etch depth vs etch time for pattern set 2.

The particle-surface interactions are the dominant mechanism, and this dictates the neutral transport inside a feature. The neutrals strike the surfaces inside a feature and are either scattered or react with the surface. The probability of this reaction S has been shown to be around 0.06 (for SF_6 in ICP plasma without a capacitive RF excitation).[13] When the neutrals impinge upon the surface inside a feature, they lose all the directional information they possess,[30] and the reflection angle follows the cosine law.[28] For example, in the case of deep RIE (with passivated sidewalls), the sidewall reactions with the neutral can be considered to be completely inert, and the etch rate at the bottom of the trench is given by[31]

$$ER_{bottom} = ER_{top} \times \frac{K}{K + S - KS}, \quad (5)$$

where K is the molecular flow transmission probability (dependent on the aspect ratio). However, since the sidewalls in our study react with the fluorine radicals, the above equation does not predict the etch rate accurately.

At the surface of the substrate, the neutrals are exposed to open field flux [which is the equal to the neutral angular distribution function (isotropic)]. However, this is restricted inside a feature, due to neutral shadowing. This causes the surfaces without an open line of sight to have lower neutral flux. The etch rate due to the neutral shadowing effect can be estimated by assuming that the radicals are completely lost when incident on the sidewall surface[29]

$$ER_{bottom} = v \cdot S \cdot Q_{F(top)} \cdot \sin\left[\arctan\frac{A}{2}\right], \quad (6)$$

where v is the volume removed per reacting neutral and A is the aspect ratio of the feature.

Surface diffusion is the phenomenon where the radicals are adsorbed on the upper sidewalls and diffuse along the surface of the etch profile.[28] This mechanism is not a prominent effect due to the geometry of the etch as well as the reactive sidewalls. Bulk diffusion is also a mechanism that can be ignored, due to the large mean free path and the dimensions of the etched features.[29]

Figure 10 presents the lateral etch depth measured. It can be seen that the lateral etch rate increases with linewidth.

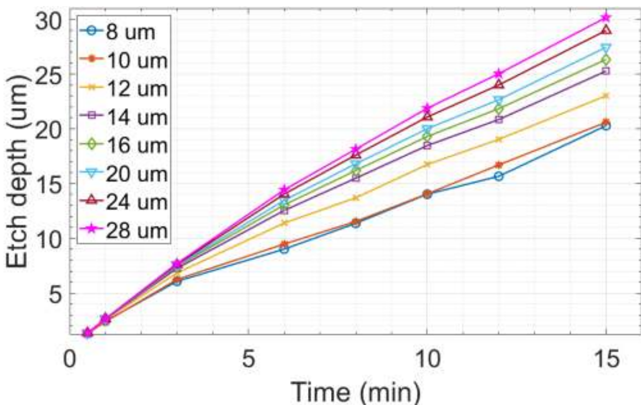

FIG. 9. Etch depth vs etch time for pattern set 2.

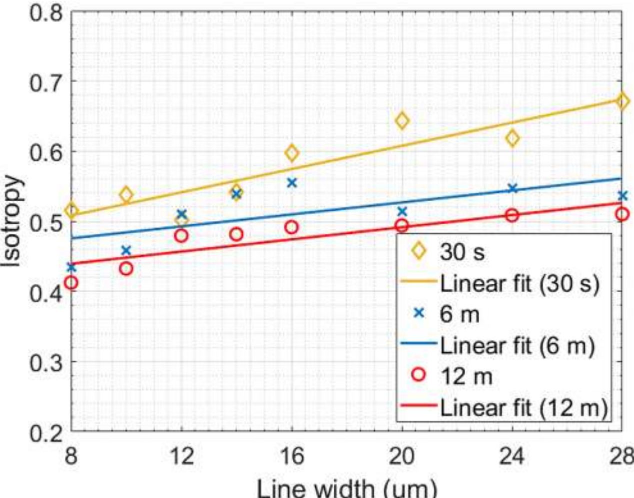

FIG. 11. Isotropy of the etch for a range of times vs linewidth.

The measurements in Fig. 10 are accompanied by some noise due to measurement inaccuracies mainly arising from the mask roughness. From Fig. 11, it can be seen that the degree of isotropy increases on the linewidth. This can be attributed to the fact that the amount of flux entering a trench is dependent on the trench width. As mentioned earlier, the neutrals that do not react with the bottom of the trench are reflected from the surface, therefore allowing them to react with the sidewalls. Hence, a larger volume of flux would lead to increased lateral etching, increasing the isotropy. The isotropy is also found to decrease with time due to the increase in the aspect ratio.

This indicates that the dominant etching mechanisms that determine the etch rate in the trenches are neutral transport and neutral shadowing. An exact prediction of the etch profile and rate could be attempted using the geometry of the structure and Monte Carlo simulations; however, this is outside the scope of this paper.

IV. CONCLUSION

It has been demonstrated that isotropic SF_6 etching of silicon is a viable alternative to other isotropic etch processes. As mentioned earlier, this method presents an opportunity to perform these etches to isolate membranes, release MEMS structures, etc., without the need for a specialized etching equipment. The absence of a liquid phase etch eliminates the need for critical phase drying and reduces the possibility of collapse and stiction. The etch rates achieved during the study demonstrate that the etch duration can be comparable or faster than the XeF_2 vapor etch process.

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