IST-LASAGNE: Towards All-Optical Label Swapping Employing Optical Logic Gates and Optical Flip-Flops

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***Abstract*—The Information Society Technologies—all-optical LAbel SwApping employing optical logic Gates in NEtwork nodes (IST-LASAGNE) project aims at designing and implementing the first, modular, scalable, and truly all-optical photonic router capable of operating at 40 Gb/s. The results of the first project year are presented in this paper, with emphasis on the implementation of network node functionalities employing optical logic gates and optical flip-flops, as well as the definition of the network architecture and migration scenarios.**

***Index Terms*—All-optical label swapping, all-optical logic gates, all-optical signal processing, Mach–Zehnder interferometer, optical flip-flops, optical packet switching, semiconductor optical amplifier, ultrafast nonlinear interferometer.**

I. Introduction

THE huge growth of Internet traffic during the last years is forcing next-generation Internet protocol (IP) networks to increase their capacity, performance, and packet forwarding rates. Future IP-based all-optical networks will require technologies to enable packet routing at terabit per second bit rates, supporting new streamlined IP routing protocols such as multiprotocol label swapping (MPLS) [1]. Optical network node implementations reported so far perform label packet processing in the electrical domain using alternative modulation formats or subcarrier multiplexing at lower bit rates (for example, IST-Switching Technologies for Optically LAbeled Signals (STOLAS) [2] or IST-Light wave Architectures for the processing of Broadband ELectronic Signals (LABELS) [3] projects) through hybrid optoelectronic node architectures. However, in order to achieve high data-rate operation [4], packet-format transparency [5], and high transmission efficiency, all network node functionalities such as switching, routing, and forwarding must be carried out directly in the physical layer. Likewise, the node optical layer needs to implement the required "intelligence" to look up the routing table and forward the packets.

All-optical label swapping (AOLS) has been proposed as a viable approach towards resolving the mismatch between fiber transmission capacity and router packet forwarding capacity [6]. In such an AOLS scenario, all packet-by-packet routing and forwarding functions of MPLS are implemented directly in the optical domain. By using optical labels, the IP packets are directed through the core optical network without requiring O/E/O conversions whenever a routing decision is necessary. The main advantage of this approach is the ability to route packets/bursts independently of bit rate, packet format, and packet length, increasing network flexibility and granularity, attributes highly desirable in broadband networks characterized by bandwidth-on-demand applications. In addition, compared to previous node implementations [2], [3], [7], the all-optical network node must be capable of operating with in-band serial-bit label signaling at the line rate, attaining high bandwidth utilization and simplified transmitter implementation. The ability to process labels at the line rate through all-optical techniques eliminates the necessity for O/E/O conversions and allows for high information capacity to be encapsulated in the labels compared to lower-bit rate approaches [6]. Further, the labels are generated with the same light sources and intensity modulators as the payload [8], a major requirement for implementation of next-generation truly all-optical networks.

In this paper, we present all-optical LAbel SwApping employing optical logic Gates in NEtwork nodes (LASAGNE), a novel node and network architecture based on AOLS scenario. The LASAGNE project aims at designing and implementing the first, modular, scalable, and truly all-optical photonic router capable of operating at 40 Gb/s. LASAGNE objectives include studying, proposing, and validating the use of all-optical logic gates based on commercially available technologies to

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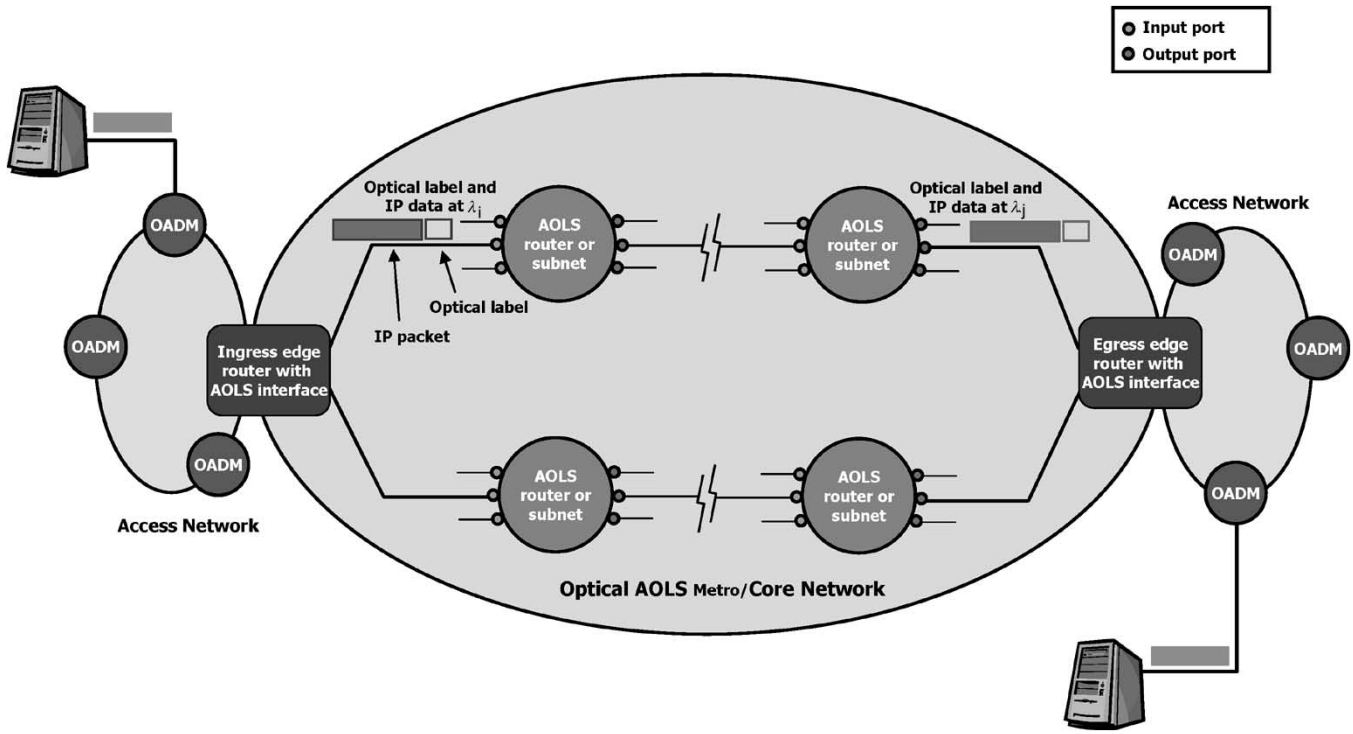

Fig. 1. LASAGNE AOLS network scenario.

implement network functionalities at the metro/core network nodes in AOLS networks. The optical logic gates are all designed to be implemented using the same fundamental building block: the semiconductor optical amplifier-based Mach–Zehnder interferometer (SOA-MZI), which results in a flexible and scalable approach in terms of manufacturing. Although the photonic prototype is currently designed as the interconnection of fiber-pigtailed SOA-MZI devices, it is envisaged that through the advent of photonic integration research, such a router could be potentially integrated in a single hybrid platform. For instance, the IST-MUlti-Functional integrated arrays of INterferometric Switches (MUFINS) project aims at monolithically integrating arrays of interferometric switches towards photonic very large scale integration (VLSI).

Furthermore, the definition of the architecture of the AOLS node must be consistent with the proposed network scenario and protocols used. An OPS network design based on the proposed AOLS node is also assessed together with the proposed migration scenario that would make feasible its deployment in European optical networks.

The remainder of the paper is organized as follows. Section II describes the LASAGNE network concept and the proposed design for the all-optical network nodes. The node synchronization issues are discussed in Section III, whereas the implementation of the main node functionalities employing optical logic gates and optical flip-flops is shown in Section IV. Finally, Section V describes the AOLS network architecture and migration scenarios.

II. Network Concept and Node Design

The LASAGNE network concept and the proposed architecture for the all-optical network nodes are described next.

A. Network Concept

An example of an AOLS network is shown in Fig. 1. The IP packets enter the AOLS network through the ingress node. There, these "low-bit-rate" packets ($\sim$ 10 Gb/s) are optically time domain multiplexed to form high-bit-rate packets or bursts ($\sim$ 40–80 Gb/s), encapsulated with an optical label, and retransmitted on a new wavelength if required. Once at the metropolitan area network (MAN)/wide area network (WAN), only the optical label is used to make routing decisions at the optical nodes, whereas the wavelength is used to dynamically redirect (forward) the high-bit-rate packets. Each AOLS router uses the content of the extracted labels to perform the forwarding decision and forward the packets toward the egress edge router (ER). An optical core router performs routing and forwarding operations together with wavelength conversion and label swapping. Throughout this process, the high-bit-rate packet is kept intact in the optical domain.

B. Node Design

Fig. 2 shows the proposed architecture of the node that is designed, studied, simulated, and implemented in LASAGNE. For the sake of directed focus on the all-optical functionalities and limited resources, the implementation and experimental validation is restricted, however, to the AOLS and packet router detailed in Fig. 3. The main functionalities required by the AOLS (label reading, new label insertion, and packet routing) are based on the use of all-optical logic gates and flip-flops. As shown in Fig. 2, the wavelengths entering the node are first demultiplexed and for each wavelength an AOLS block is implemented. An AOLS block comprehends the true forwarding functionality of incoming packets. Entering the AOLS

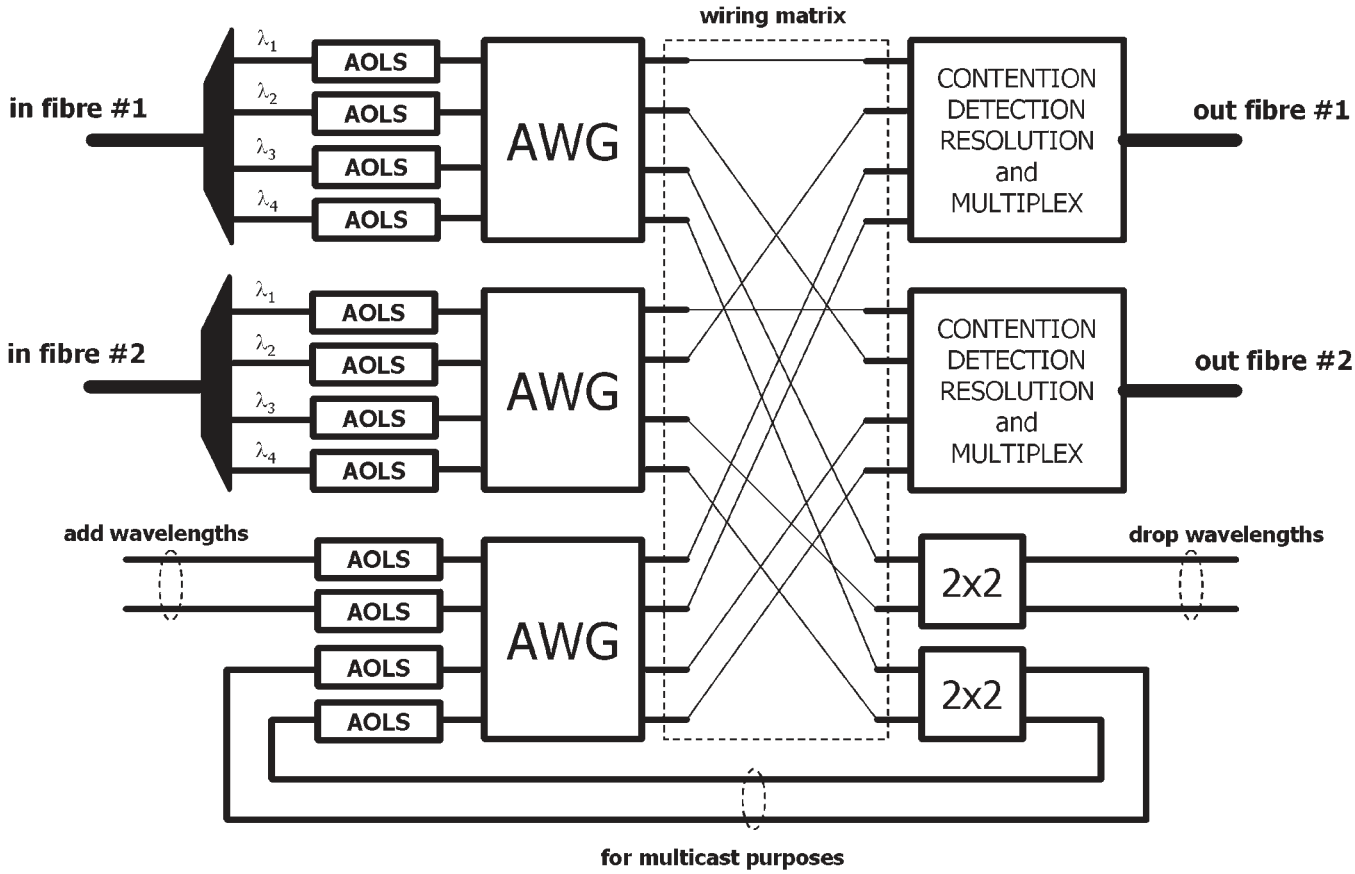

Fig. 2. Proposed photonic routing architecture.

module, the packet payload (40 Gb/s) and label (10 Gb/s) are separated [9], as shown in Fig. 3. The extracted optical label is fed to a bank of optical correlators based on all-optical logic XOR gates (AOLXGs) [10], where the comparison between the label and a set of local addresses is performed. These local addresses are generated using optical delay lines (ODLs). An ODL is comprised of a set of interconnected fiber delay lines, couplers, and splitters that generate a bit sequence out of one pulse. Thus, comparing the incoming label to the local addresses implies that for each possible incoming label a separate ODL and a correlator have to be installed in the AOLS block. After comparison, a high intensity pulse will appear at the output of the XOR correlator with the matching address. This pulse feeds a control block that drives a wavelength converter. The control block is made-up of all-optical flip-flops (AOFFs) [11]. Depending on the matching address (correlator output pulse), the appropriate flip-flop will emit a continuous wave (CW) signal at a certain wavelength. In this way, the internal wavelength is chosen. Meanwhile, a new label is generated in the appropriate ODL. The new label is inserted in front of the payload and both the payload and the new label are now converted to the wavelength generated by the flip-flop. The packet is then sent through an arrayed-waveguide grating (AWG); therefore, the wavelength on which the packet leaves the AOLS block determines the outgoing port on which the packet leaves the node. Two switches provide the flexibility to configure the assignments between the incoming labels and the outgoing labels and wavelengths. The size of the packet router (for example, number of optical correlators and flip-flops) is very dependent on the number of local addresses used in the routing table. The AOLS subsystem of Fig. 3 was depicted for the specific case of four different locally generated addresses (2-bit optical labels).

The synchronization between the optical subsystems employed in the AOLS routing node and the timing information of the incoming packet is of crucial importance for the proper operation of the node. The AOLS node requires timing extraction on a packet-by-packet basis and a packet arrival detection scheme. These functionalities are performed by a clock recovery circuit [12] and a single-pulse generator. The former is placed at the beginning of the router and is capable of handling high-bit-rate burst mode optical packets. The latter generates an optical pulse as a packet arrives to the AOLS. Therefore, the switches used for generating the reference addresses and the new label are controlled by a low-speed dynamically controlled network control plane (CP).

C. AOLS Contention Resolution Design

In Fig. 2, optical packet contention can happen near the output fiber ports of the AOLS packet switch when there is more than one optical packet trying to exit to one output fiber at the same time on the same wavelength or when there are more than four optical packets trying to exit to one output fiber at the same time. However, at the time of writing, there is no known solution for a complete all-optical contention

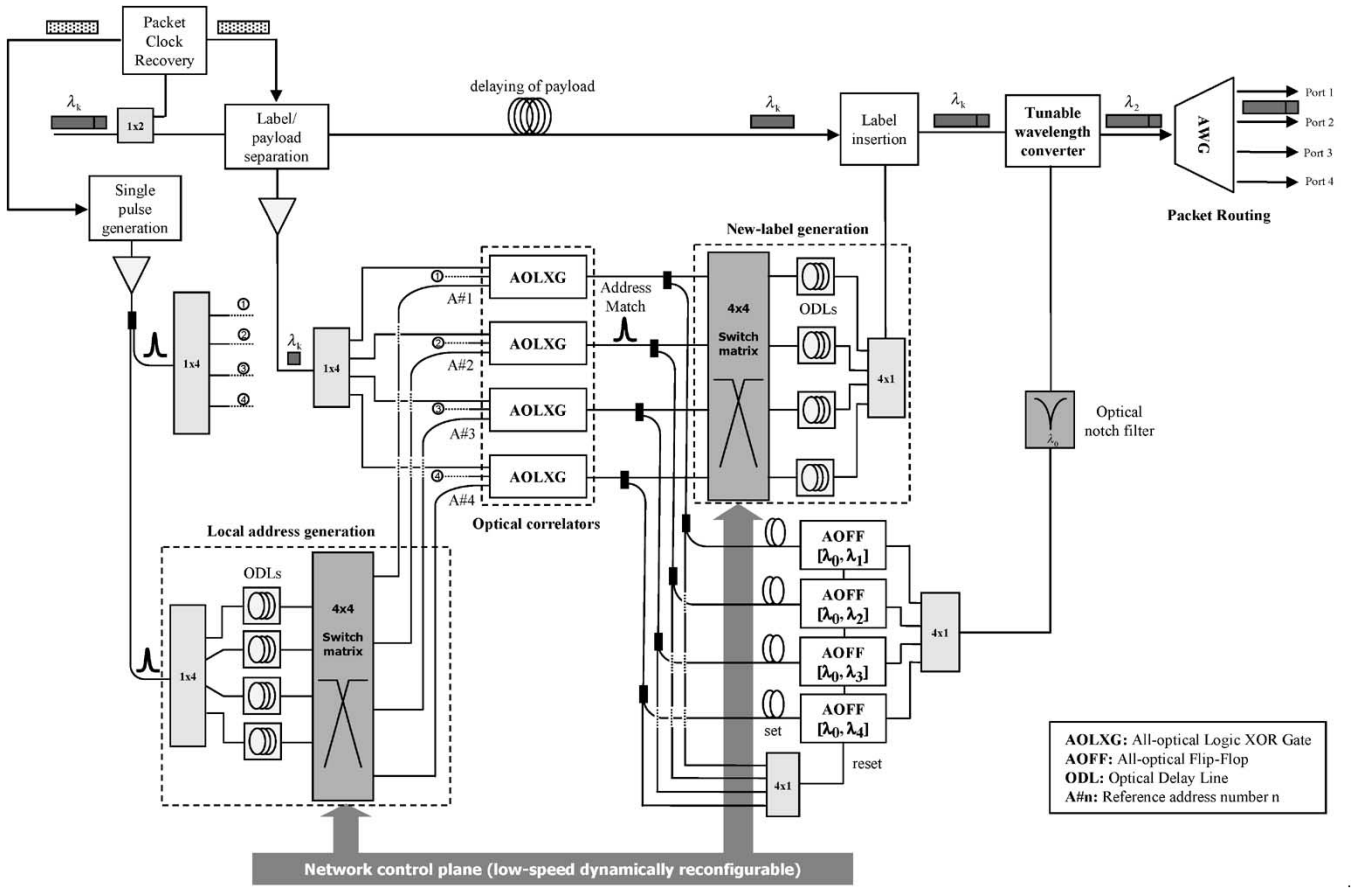

Fig. 3. Experimental verification of LASAGNE label swapper and packet router.

resolution block design for the output-buffered AOLS packet switch, which requires all-optical packet contention detection, all-optical control for the variable optical delay, and all-optical control of the tunable wavelength conversion. Electronic control is a requisite to realize the contention resolution for such an AOLS packet switch. Therefore, all-optical input-buffered contention resolution for the AOLS packet switch is presented in this section.

The layout of such a contention-free nonblocking AOLS packet switch design is shown in Fig. 4. The main principle of the contention resolution schemes is deploying more internal and external wavelengths in the AOLS systems and networks. In the example shown in Fig. 4, 16 wavelengths are used instead of four in Fig. 2. These 16 wavelengths $\{\lambda_1 - \lambda_{16}\}$ consist of four groups of four wavelengths that the 4×4 AWG will treat cyclically, which means that the 4×4 AWG routes the four wavelengths in the group $\{\lambda_1 - \lambda_4\}$, $\{\lambda_5 - \lambda_8\}$, $\{\lambda_9 - \lambda_{12}\}$, and $\{\lambda_{13} - \lambda_{16}\}$, respectively, the same way. This is referred to as the cyclic characteristic of an AWG [13]. Based on this characteristic, we configure the second wavelengths of the optical flip-flops in Fig. 4 in an ordinal way from λ_1 to λ_{16}, four as a group as explained earlier, so that the AWGs in Fig. 4 behave exactly the same way as in Fig. 2. Consequently, in Fig. 4, the optical packets coming out of the AWGs during the same period can have up to 16 different wavelengths, but there are never optical packets on the same wavelengths trying to exit to one output fiber at the same time. For example, in an extreme case where contention is most likely to happen, assuming at one time all the incoming optical packets entering the switch are destined to the same output fiber, in the AOLS packet switch in Fig. 4, these 16 optical packets will be converted, respectively, onto $\lambda_1 - \lambda_{16}$, so that they can be sent out to that output fiber contention free without delay after the AWGs.

As a result, the AOLS network of the AOLS packet switches in Fig. 4 employs 16-wavelength wavelength division multiplexing (WDM) instead of the four-wavelength WDM in Fig. 2. Therefore, at each input fiber, there are also possibly up to 16 wavelengths instead of four. Since the AOLS packet switch was originally designed for four-wavelength WDM and thus can only deal with four wavelength channels per fiber at a time, waveband demultiplexers are introduced here to separate the 16-channel WDM traffic into four groups of the four wavelengths that every AOLS array (per AWG) can process at the same time. Synchronization is still necessary after the waveband demultiplexers to keep the optical packets from the same input fiber port aligned. Fixed optical delay units (Δt) are deployed to allow for the processing time of the optical packets in different wavelength groups. Δt is determined by the AOLS processing duration for one optical packet, so its value is fixed and can be estimated beforehand.

The following preconditions exist and are satisfied: 1) AWGs have cyclic characteristics [13]; 2) the AOLS does not process the wavelength information of the incoming packets; 3) the

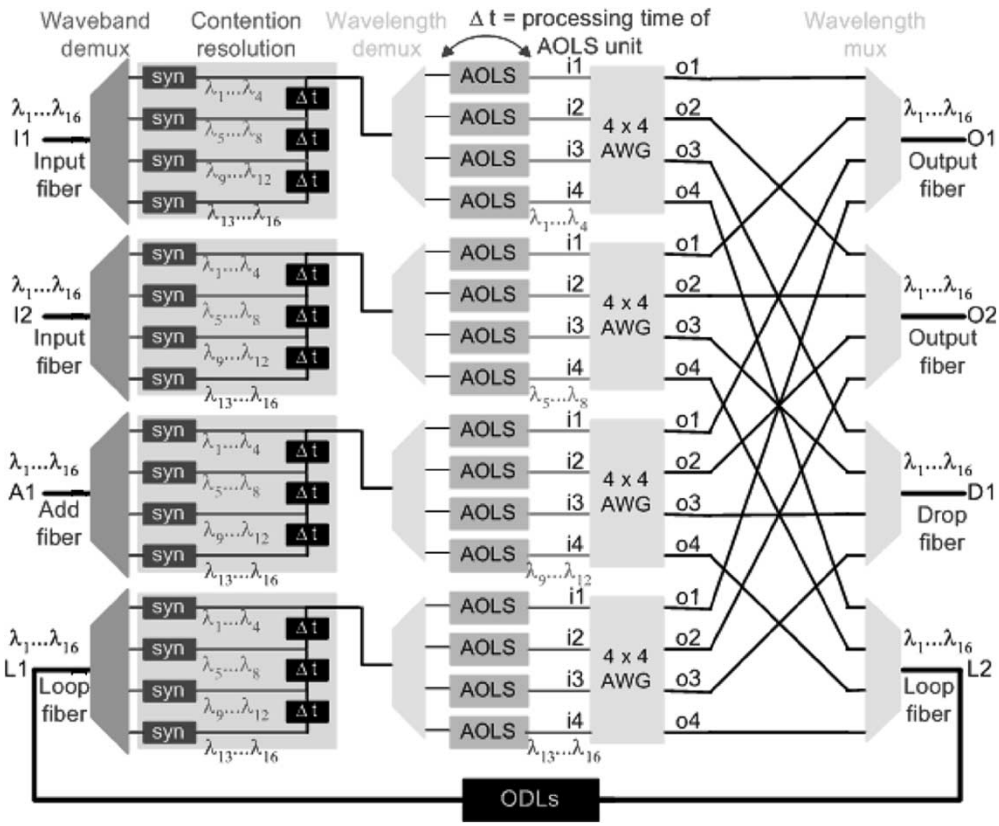

Fig. 4. Regular AOLS packet switch schematic configuration with contention resolution.

wavelength receiving and operation ranges of the AOLS are beyond $\{\lambda_1 - \lambda_{16}\}$; 4) WDM allows us to use the enormous fiber bandwidth; 5) for high data processing rate, negligible latency is caused by the queuing in different wavebands.

The advantages of the scheme include the following: 1) contention is completely solved; 2) it is at the moment, to our knowledge, the only all-optical contention resolution for this kind of AOLS packet switches; 3) apart from the wavelength resource, it technically does not add any more difficulty or complexity on the AOLS packet switch buildup; 4) the operation principle is simple and intelligible; 5) only input packet synchronization is required. The disadvantages include: 1) usage of more wavelength resource; 2) the queuing of the wavebands might introduce unnecessary delay; and 3) further investigation needs to be carried out concerning the all-optical synchronization of different wavebands.

III. All-Optical Node Self-Synchronization

The LASAGNE AOLS scenario involves the design and implementation of an all-optical node capable of receiving, processing, and routing packet traffic solely in the optical domain. Optical data processing, however, requires the presence of an all-optical synchronization stage at the input of the node that will be used to control or power-up subsequent node subsystems. Considering the defined AOLS scenario that blends a packet-switched network with all-optical signal processing, such a synchronization stage should be capable of operating at the line rate and on a packet-by-packet basis while maintaining high bandwidth utilization factors. The ability to perform with packets allows for bandwidth-on-demand use, whereas low overheads lead to effective processing of smaller packets that eventually define the granularity of the network. In this rationale, aside from the technological performance metrics, the most important attribute of such synchronization circuits is their capability to operate with packets, a fact that requires low lock-in time and low persistence time. In this rationale, two synchronization modules are reported and their proof-of-principle is experimentally verified: a packet clock recovery operating at 40 Gb/s capable of extracting the clock on a per-packet basis and a packet-rate clock recovery at 10 Gb/s capable of generating a single pulse per incoming packet. These self-synchronization modules were specifically designed so as not to require local signal generation and/or synchronization of incoming packets with local optical or electrical oscillators.

A. 40 Gb/s Packet Clock Recovery Circuit

In this section, the principle of operation and the experimental validation of the packet clock recovery circuit operating at 40 Gb/s are reported. In contrast to previously reported optical clock recovery circuits [14]–[16] comprising of high-Q cavities, the approach proposed here uses a low-Q passive filter in combination with a power-limiting optical gate to achieve instant locking and low clock persistence time, as described in [12]. Exploiting the memory effect of such a low-Q comb-generating filter, packet-to-packet processing is achievable due to the short

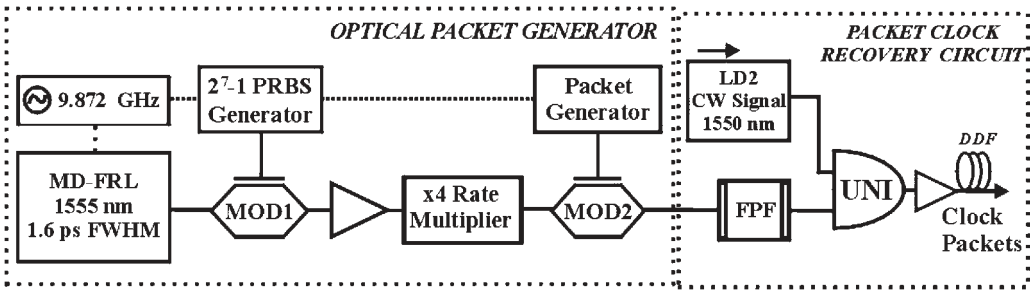

Fig. 5. Packet clock recovery experimental setup.

impulse response of the filter. The bit wise processing offered by optical gates is then used to produce high-quality recovered clock packets, where a cascaded optical gate plays the role of the power limiter.

The block diagram of the experimental setup is shown in Fig. 5 and consists of the optical packet generator and the clock recovery circuit. An actively mode-locked fiber ring laser (MD-FRL) provided a 9.872-GHz pulse train consisting of 1.6-ps pulses at 1555 nm. This pulse train was modulated to form a $2^7 - 1$ pseudo-random binary sequence (PRBS) signal using a PRBS generator and a Ti:$LiNbO_3$ modulator (MOD1) and was then rate upgraded in a fiber-based bit interleaver to generate 39.488 Gb/s pseudo-data stream. Data packets were then generated using a second electrooptic modulator (MOD2) driven by a programmable PRBS generator. The data packets were fed into the packet clock recovery circuit, consisting of a low-Q Fabry–Pérot filter (FPF) and an SOA-based ultrafast nonlinear interferometric (UNI) gate, powered by a CW signal at 1550 nm [laser diode 2 (LD2)]. The FPF played the role of the passive optical resonator that extracts the line rate spectral component. Exploiting the filter memory effect, the data packets are transformed into clock packets with intense amplitude modulation. The FPF used was a bulk micrometer-adjustable fused quartz substrate with free spectral range (FSR) equal to the line rate and finesse equal to 50. The output of the filter was amplified and inserted into the UNI gate as the control signal. The UNI gate was optimized for 40 Gb/s operation by using a polarization-maintaining (PM) fiber that induces 5 ps of birefringent delay in the two orthogonal polarization components of the input and output ports of the gate. As a result, an asymmetric switching window with respect to the bit slot is formed, relaxing the requirement for the SOA recovery time. The saturation of the gate by CW light injection close to the SOA material transparency results in a strongly nonlinear step-like transfer function [17]. This provides the intensity modulation reduction that is necessary for generating a packet-level clock signal from the amplitude-modulated Fabry–Pérot output. Finally, the self-extracted clock packets were amplified in an erbium-doped fiber amplifier (EDFA) and launched into a dispersion-decreasing fiber (DDF)-based pulse compressor used at the output of the UNI gate. The active element of the UNI gate was a 1.5-mm bulk InGaAsP/InP ridge waveguide SOA provided by OPTOSPEED S.A. with 27 dB of small signal gain at 1550 nm and a recovery time of 80 ps when driven with 700 mA.

Fig. 6 shows a sequence of four 40-bit-long packets separated by 750 ps at 40 Gb/s. The FPF partially fills the zeros within the packet due to its low finesse so that deeply amplitude-modulated but clock-resembling packets are obtained as shown in Fig. 6(b). When this signal is fed as control into the saturated UNI gate, clock packets with very short rise and fall times are generated and depicted in Fig. 6(c). Fig. 6(d)–(f) provides a more detailed view of a single packet, its form after passing through the FPF and its transformation to an amplitude-equalized packet clock signal at the output of the gate. Fig. 6(f) shows that the clock is captured from the first bit and exhibits a fall time of 16 bits, whereas the amplitude modulation (highest to lowest pulse ratio) within the 40 clock pulses is below 1 dB. The sharp rise time is a result of the heavy saturation of the SOA and determines the lock acquisition time of the circuit, whereas the fall time is due to the lifetime of the filter and determines the minimum intrapacket guardbands. The circuit was operated by injecting 1 mW of optical power from the CW signal and 80 fJ pulse from the data signal.

The timing jitter performance of the circuit was measured using a continuous PRBS signal at 40 Gb/s with the precision time base option of an Agilent/HP 86100A Infinium digital sampling oscilloscope. Fig. 7(a) shows the eye diagram obtained for the input signal at 40 Gb/s with a root mean square (rms) timing jitter of 450 fs. The reshaping properties of the power-limiting gate are shown in Fig. 7(b) through the eye diagram of the recovered clock at 40 GHz with a measured timing jitter of 580 fs. The slight increase in rms jitter was due to the difficulty of precisely aligning the bulk FPF used, resulting in small line rate detuning. This effect can be eliminated by using fiber-based FPFs.

Using two preamble bits, the clock is captured from the first bit (instantaneous locking) and persists for the duration of the data packet increase by an exponential decaying tail of only 16 bits. Although the experimental data presented use a $2^7 - 1$ PRBS, the clock recovery circuit can be designed according to the requirements of the network traffic by tailoring the finesse of the FPF. For instance, if a PRBS of $2^{31} - 1$ is required, the filter should be designed to have a finesse of 80 [12]. In this case, the recovered clock packet would exhibit less than 150 ps lock-in time and a decay time of approximately 2 ns. Also, since FPF has over 50 nm of optical bandwidth, the clock recovery circuit is only limited by the gain bandwidth of the SOA used, making the scheme broadband and insensitive to laser source wavelength instabilities.

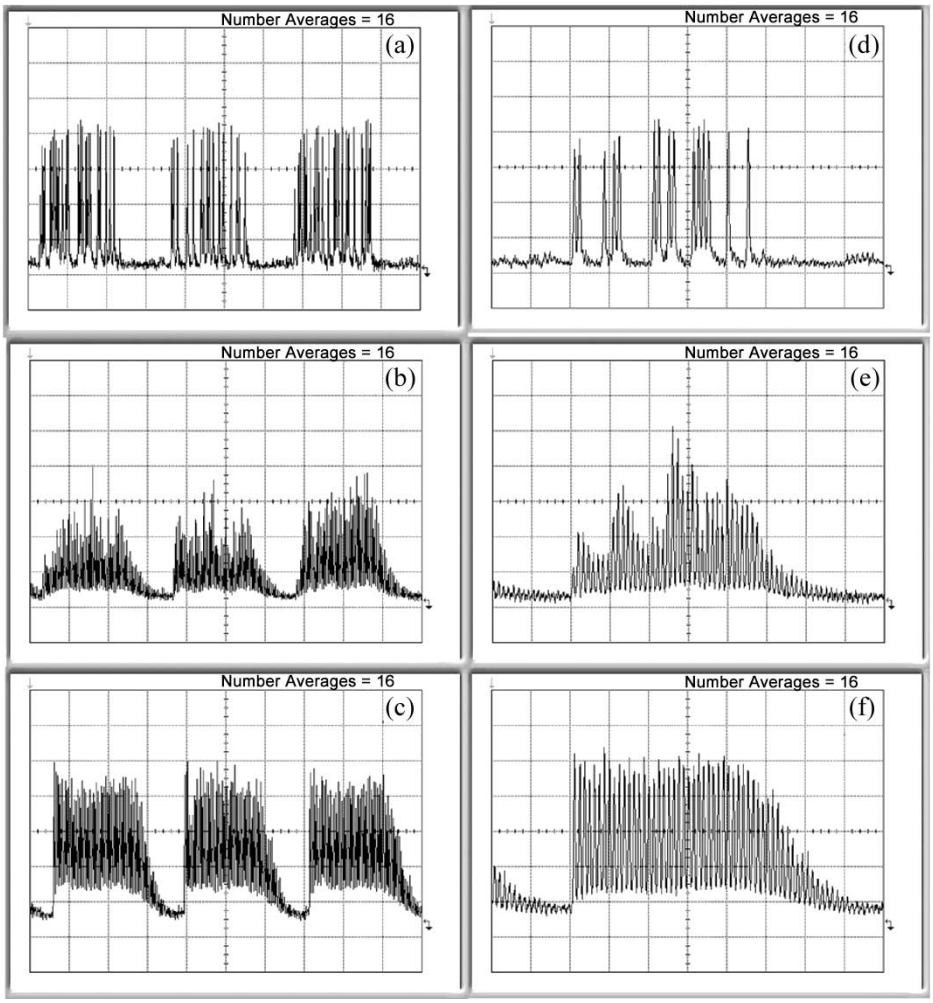

Fig. 6. (a), (b), and (c) input data packets, FPF output, and recovered clock packets at 500 ps/division time base. (d), (e), and (f) single packet, FPF output, and recovered clock at 200 ps/division time base.

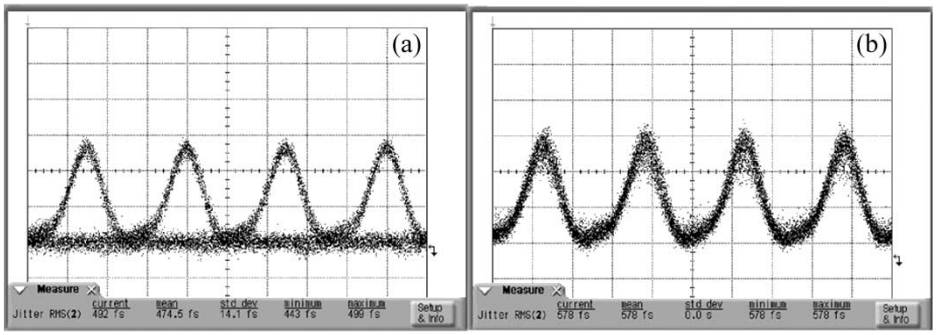

Fig. 7. Eye diagrams of (a) input data packets and (b) recovered clock packets. The time base is 10 ps/division.

B. Packet-Rate Clock Recovery Circuit

This subsection is concerned with the design and experimental validation of the packet-rate clock recovery circuit that is necessary for powering and controlling the LASAGNE optical gates as described in Section II. The circuit is responsible for generating a single pulse per incoming packet analogous to the frame synchronization pulse in traditional synchronous optical network (SONET)/synchronous digital hierarchy (SDH) systems. Specifically, for the design of LASAGNE node, the packet-rate clock recovery circuit is interconnected with the local address generation and the optical correlator blocks, as shown in Fig. 3.

Previous implementations of single-pulse extraction techniques involve a marker pulse at the beginning of the packet at a different state relative to the rest of the packet in terms of either wavelength [18], polarization [19], bit period [20], or amplitude [21], resulting in increased complexity to the generation and transmission of packets. More recently, experiments have been reported where all the pulses of the packet

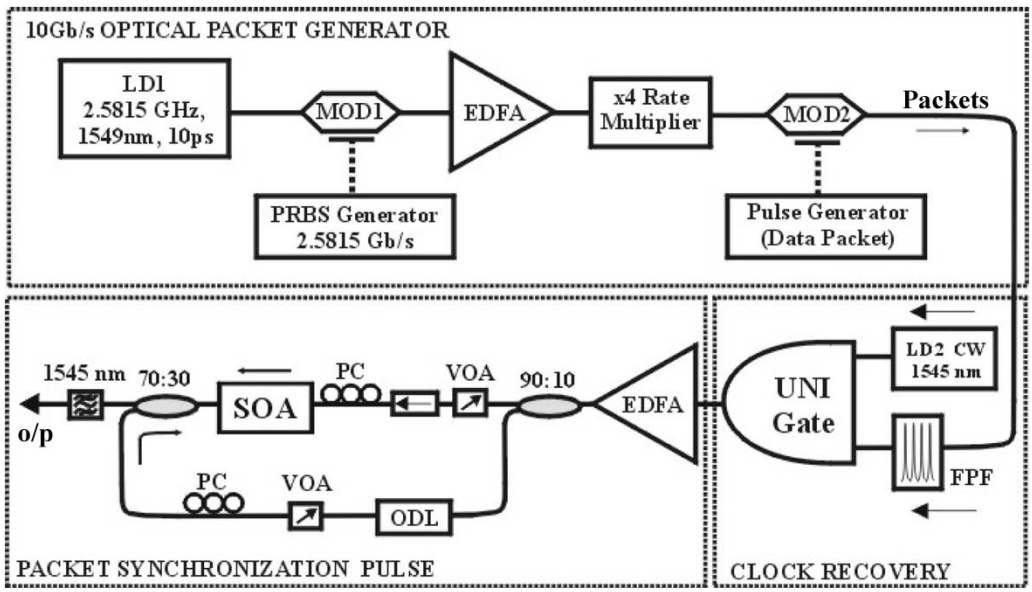

Fig. 8. Experimental setup of packet-rate clock recovery at 10 Gb/s.

share the same physical state [22], [23]. In these approaches, an SOA with a very long recovery time is required [22], which in turn introduces very long guard bands between the transmitted packets or specific coding techniques [23]. The packet-rate clock recovery proposed here only requires the clock recovery circuit described in the previous section and a single SOA to extract a single pulse from each incoming data packet without additional signaling or guard-band requirements.

The block diagram of the experimental setup is depicted in Fig. 8 and consists of the data packet generator, the packet clock recovery circuit, and an additional SOA device. To generate the data packets, a distributed feedback (DFB) LD1 emitting at 1549 nm was gain switched at 2.5815 GHz, providing 10-ps full-width at half-maximum (FWHM) pulses after linear compression. This pulse train was modulated with a $2^7 - 1$ PRBS in a Ti:$LiNbO_3$ modulator (MOD1) and was inserted in a fiber-based bit interleaver to generate a pseudo-data pattern at 10.326 Gb/s. A second Ti:$LiNbO_3$ modulator (MOD2), driven by a programmable pulse generator, modulated this PRBS data stream into packets of 4-ns length at 80.672 MHz, which then entered the clock recovery circuit. In accordance with the previous section, a clock packet is self-extracted from each corresponding data packet entering the clock recovery circuit. After amplification through an EDFA, the extracted clock packets were split and inserted into a 1.5-mm SOA in a counter-propagating fashion, synchronized with 1-bit offset. The operation of the circuit relies on cross-gain modulation (XGM) and the specific temporal synchronization of the involved signals within the amplifier. Due to the single-bit delay induced, only the first clock pulse experiences amplification, whereas subsequent probe pulses are suppressed through the interaction with the counter-propagating strong pump signal incident on the SOA. Fine synchronization of the signals was achieved using ODL1 and both signal polarization states needed adjustments due to the polarization dependence of the SOA used.

Fig. 9 shows typical oscilloscope traces verifying the circuit principle of operation. More specific, Fig. 9(a) and (d) shows the 4-ns optical packets separated by 8.4 ns and Fig. 9(b) and (e) shows the recovered clock packets exhibiting a 2-bit rise time and an 8-bit fall time. This signal is then split and inserted into the SOA responsible for the single-pulse extraction. The recovered clock packet acting as the probe signal is within the small-signal-gain region of the amplifier, and the first preamble pulse enters the SOA that is fully unsaturated. After experiencing full amplification, it exits the SOA. The remaining clock pulses are suppressed through gain saturation induced by the counter-propagating strong recovered clock signal, acting as the pump. As a result, a single pulse is allowed to exit the SOA, and this is shown in the oscilloscope traces of Fig. 9(c) and (f). The switching power/energies used in the UNI gate were 0.8 mW for the CW power and 110 fJ for the control input. The single-pulse extraction required 300 and 15 fJ for the pump and probe signals, respectively, in order to invoke XGM within the amplifier. Since the circuit relies on saturation effects within an SOA, the operational speed of the circuit is dictated only by the packet clock recovery circuit, making the scheme upgradeable to 40 Gb/s. The proposed circuit will be experimentally verified using 40 Gb/s packets combined with an SOA-MZI-based packet clock recovery during the second phase of the project.

IV. Node Functionalities Employing All-Optical Logic Gates and Optical Flip-Flops

All-optical logic gates and optical flip-flops are considered as the basic functional block for implementing the key functionalities required at the optical node: label and payload separation, label reading, tunable wavelength conversion, and packet routing. Detailed structure and performance results for these subsystems are provided in this section.

A. Label/Payload Separation Circuit

The optical circuit responsible for separating the label from the payload [9] of incoming data packets is presented in this

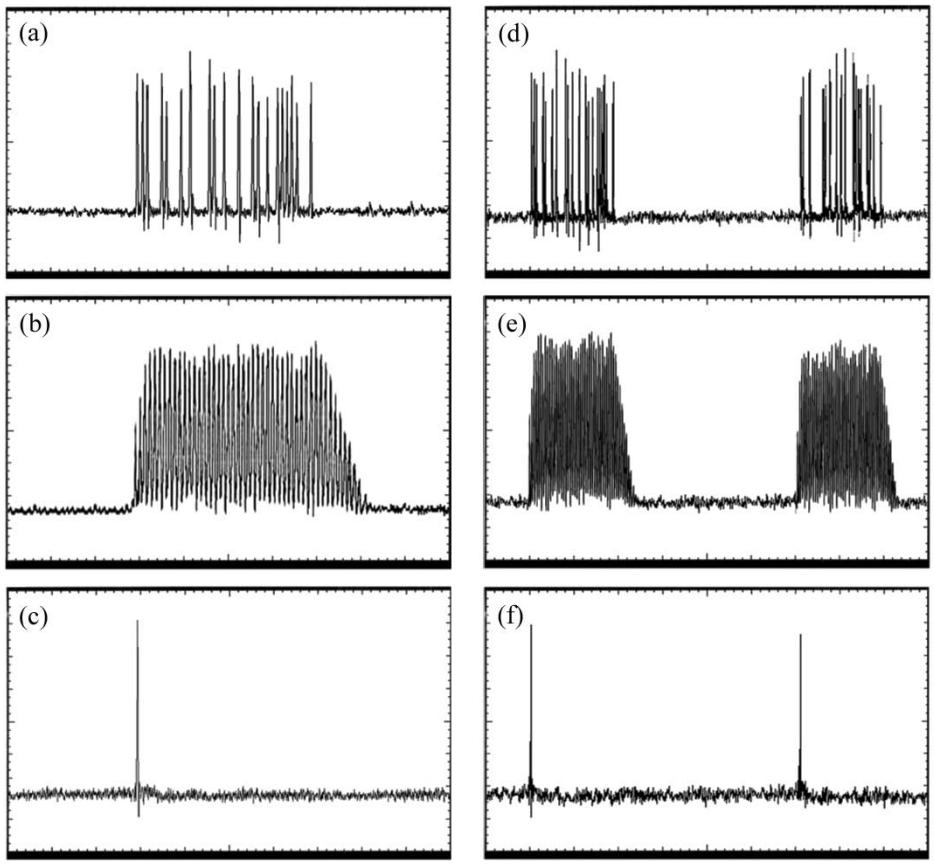

Fig. 9. (a) and (d): Input data packets; (b) and (c): Generated clock packets; (c) and (f): Output pulses at packet rate. Time base in (a), (b), and (c) is 200 ps/division and in (d), (e), and (f) 400 ps/division.

subsection and the principle of operation is verified through simulation studies using the commercially available simulation tool VPI TransmissionMaker at 40 Gb/s. Fig. 10(a) shows a schematic diagram of the label/payload separation circuit along with its principle of operation. The circuit consists of two subunits: the previously described optical packet clock recovery circuit and an additional high-speed optical gate, both simulated here as SOA-MZI gates operable at 40 Gb/s. The incoming data packets are split into two parts, one used as input in the clock recovery circuit (MZI1) and one to enter as data signal in MZI2. The extracted optical packet clock signal persists for the duration of the original data packet and is used as the control signal in MZI2. For label separation, MZI2 is configured to perform a simple Boolean AND operation between the original incoming packet stream and a delayed version of the recovered packet clock after optical filtering. Successful label/payload separation is obtained if the original packet and the extracted clock are temporally delayed by an amount equal to the packet label length increased by the rise time required for clock acquisition. As such, the packet clock is delayed in an ODL so that only the payload bits of the original packet fall within the switching window of the recovered clock and are therefore switched at the gate output. Fig. 10(b) shows the packet format chosen for the experimental validation of the LASAGNE node consisting of the optical header and payload sections. The optical header contains two preamble and one stuffed bit to assist the clock extraction process and two label bits separated by 100 ps. The specific format was chosen to guarantee successful clock recovery and to relax the SOA recovery time requirements in the all-optical XOR correlators described in the next subsection. The payload of the data packet was a $2^7 - 1$ PRBS with 1.5-ns duration.

Fig. 11 shows typical simulation results of the 40 Gb/s label/payload separation circuit obtained using the commercial simulation tool. Fig. 11(a) shows the incoming data packet having an optical header "11010100" with an embedded optical label "01." Fig. 11(b) shows the recovered packet clock with instantaneous locking and 12 bits 1/e fall time. Fig. 11(c) and (d) shows the extracted label and payload, respectively, whereas the insets depict eye diagrams of four packets containing all possible 2-bit label combinations. Analysis of the simulation results reveals an extinction ratio of 13 dB for the extracted label and 11 dB for the extracted payload, whereas both pulse traces have less than 0.7 dB of pulse-to-pulse amplitude modulation.

B. All-Optical Correlators Based on Logic XOR *Gates*

In order to take the packet routing decisions inside the LASAGNE node, the labels of the incoming packets need to be compared with specific address keywords. One common way to perform this optical bit pattern recognition is through the use of a time-domain optical correlator to match a series of bits to an optical look-up table. The way to implement this

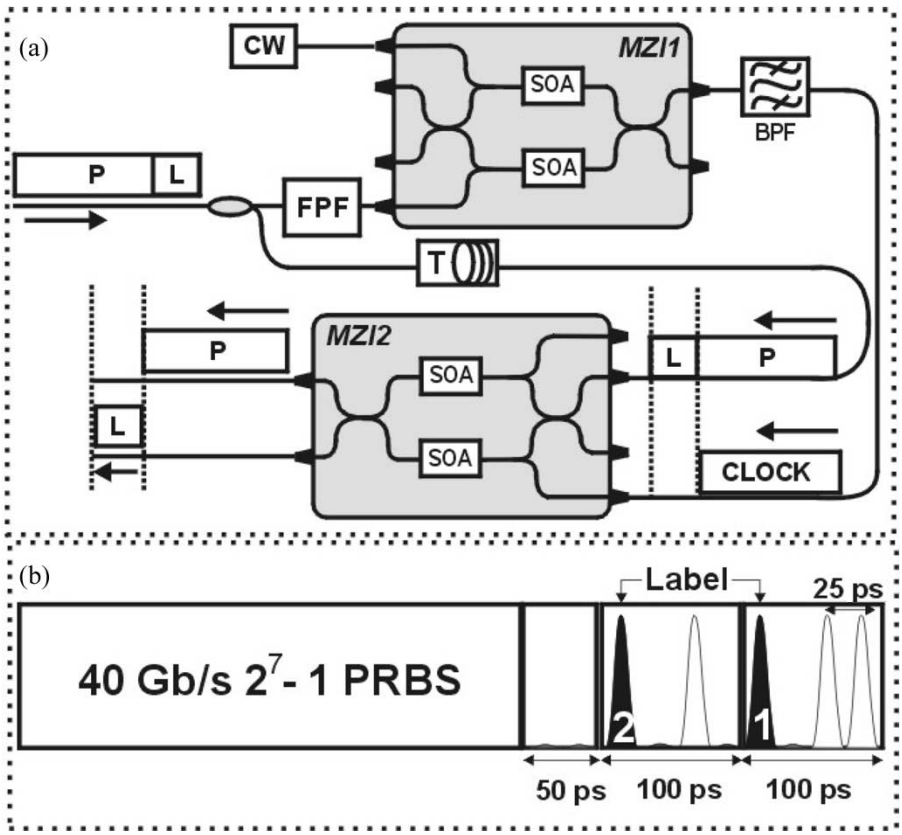

Fig. 10. Schematic diagram showing (a) principle of operation of label/payload separation circuit using two SOA-MZI gates and (b) optical packet format.

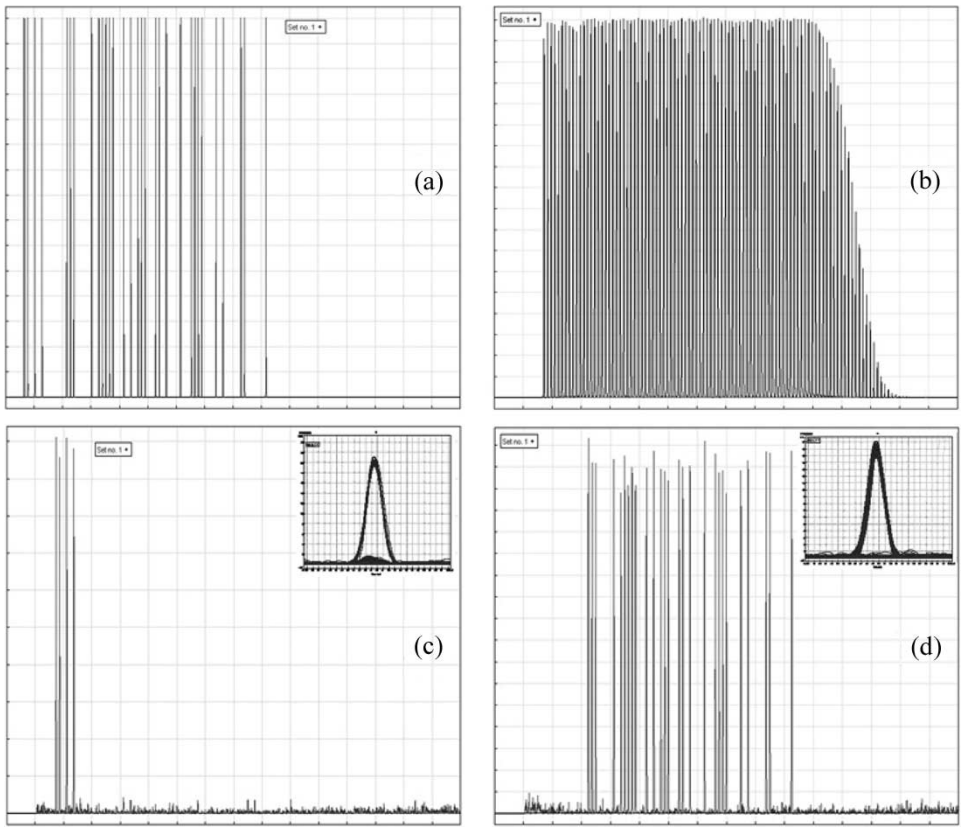

Fig. 11. Simulation results of label/payload separation circuit at 40 Gb/s showing pulse traces of (a) incoming data, (b) recovered packet clock, (c) extracted label, and (d) extracted payload with insets showing eye diagrams of four packets containing all possible 2-bit label combinations. Time base is 200 ps/division.

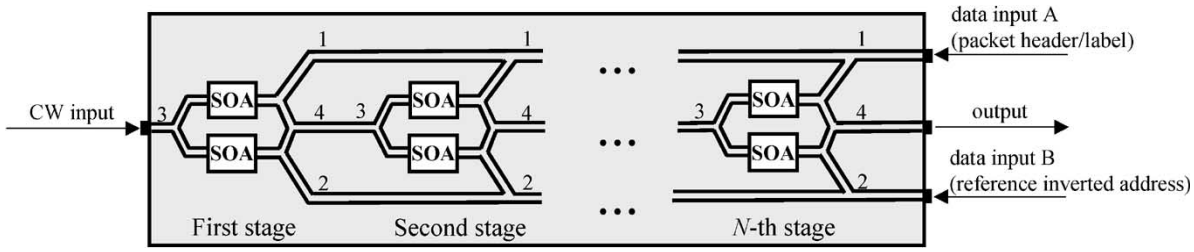

Fig. 12. Proposed architecture for the all-optical label processor or optical correlator.

functionality in LASAGNE is by means of AOLXG based on SOA-MZI devices. However, the implementation of this subsystem is limited to four correlators (e.g., four output ports or wavelengths in the node), which gives rise to 2-bit optical labels (Fig. 3).

The proposed architecture for the all-optical label processor (optical correlator) is shown in Fig. 12 [24]. It is mainly based on a cascade of photonic-integrated SOA-MZIs. Each one of these SOA-MZIs is configured to operate as a logic XOR gate as in [25], but using a counter-propagating scheme to avoid optical filtering between different stages. The two input data streams are coupled into ports 1 and 2 of the MZI, while a CW light is coupled into port 3. The output signal at port 4 of the first SOA-MZI is the result of a logic XOR operation of both data streams. This output signal, after proper optical attenuation and delay, is launched into port 3 of the second SOA-MZI synchronized with the second bit of the data patterns. The main difference between the first stage and the second and further stages is that the input signal at port 3 is not a CW signal, but a pulsed one, which acts as an enabling signal as in [10]. Although it is not directly shown in the schematic diagram of Fig. 12, the optical lengths of the waveguides transporting both data signals need to be carefully adjusted to assure that each bit of the data patterns is perfectly synchronized between them and the control signal. By cascading the different SOA-MZI structures, we obtain the logic function

$$S_i^{(j)} = S_{i-1}^{(j-1)} C_i \tag{1}$$

where $S_i^{(j)}$ is the ith bit of the signal at the output of the jth stage and C_i is given by

$$C_i = A_i \oplus B_i \tag{2}$$

where A_i and B_i are the ith bits of the input data signals to the optical correlator. $S_i^{(0)} = 1$ represents the CW input signal to stage 1. By considering that the bit length of the data inputs and the number of stages is equal to N, the output of the whole device would be

$$S_i^{(N)} = 0, \quad i < N; \qquad S_N^{(N)} = \begin{cases} 0, & \text{if } A \neq \overline{B} \\ 1, & \text{if } A = \overline{B}. \end{cases} \tag{3}$$

Therefore, the device can be employed as an all-optical correlator for bit-pattern matching applications by introducing the one's complement of one of both data signals or addresses to be compared.

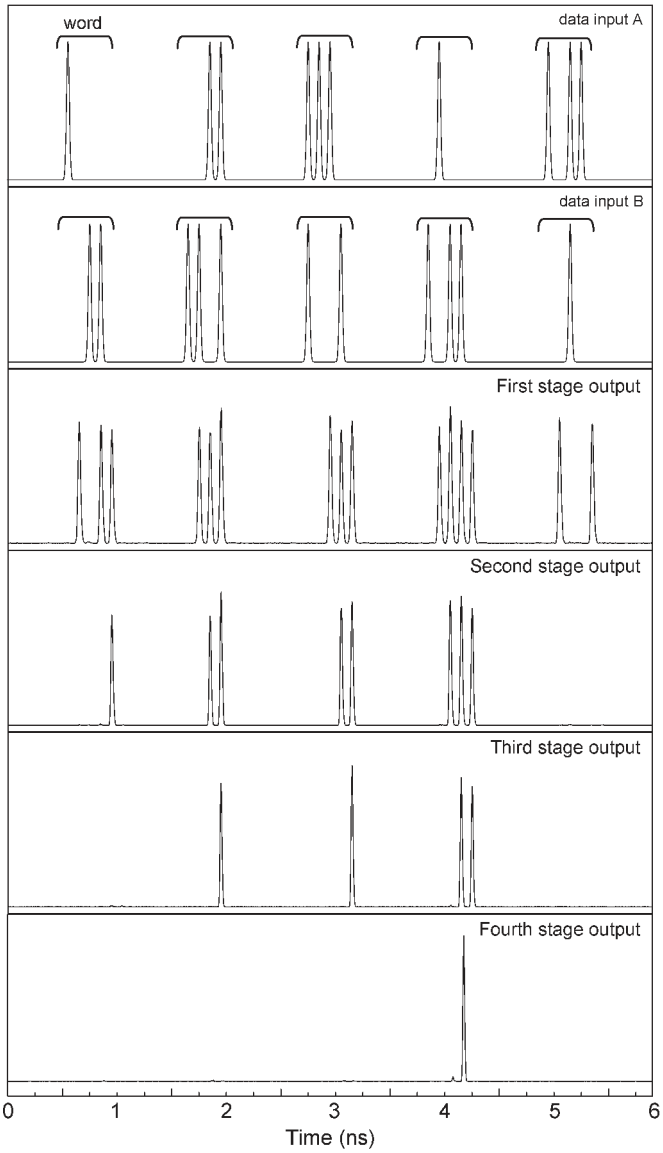

Fig. 13. Simulation results of bit-pattern matching (label/address recognition).

In order to validate by simulation the architecture operation, the Virtual Photonics Inc. software was used. A transmission line laser model technique has been applied to model the SOAs [26]. The SOAs in the MZIs are characterized by a length of 500 μm, a linewidth enhancement factor of 8.0, a confinement factor of 0.3, a carrier lifetime of 16.3 ns, a spontaneous emission factor of 1.5, and a drive current of 250 mA. The simulation results are shown in Fig. 13 for 4-bit words. Two 10 Gb/s

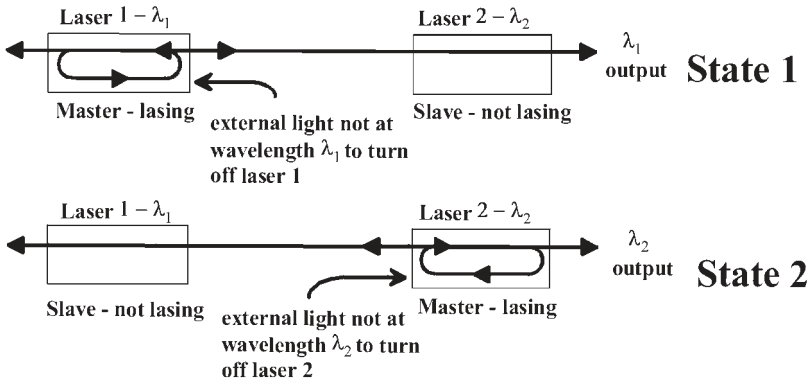

Fig. 14. Arrangement of two coupled identical lasing cavities showing the possible states. In State 1, light from Laser 1 suppresses lasing in Laser 2. In State 2, light from Laser 2 suppresses lasing in Laser 1. To change states, lasing in the master is stopped by injecting light not at the lasing wavelength.

data inputs [30-ps FWHM return to zero (RZ) Gaussian pulses at 1553.6 nm] comprised of several bit patterns were applied to the correlator: $\mathrm{A} = [1000, 0011, 1110, 0100, 1011]$ and $\mathrm{B} = [0011, 1101, 1001, 1011, 0010]$. Only the fourth word in data input B is exactly the one's complement of the fourth word in data input A. Therefore, only an address matching signal is expected for this word at the output of the whole architecture. The output signals from each SOA-MZI stage are shown in Fig. 13, where it can be seen that only an optical pulse is obtained at the output of the device (fourth stage output) for the fourth data word that validates its header/address recognition functionality. The extinction ratio of the output signal was found to be higher than 15 dB.

Although the architecture has been simulated at 10 Gb/s, this can be extended to 40 Gb/s optical labels by employing a differential scheme at the SOA-MZI inputs [27].

C. Optical Flip-Flops

The AOFF memory that we use is based on two coupled lasers with separate laser cavities. A schematic of the flip-flop is depicted in Fig. 14. The system can have two states. In State 1, light from Laser 1 suppresses lasing in Laser 2. In this state, the optical flip-flop memory emits CW light at wavelength λ_1. Conversely, in State 2, light from Laser 2 suppresses lasing in Laser 1. In state 2, the optical flip-flop memory emits CW light at wavelength λ_2. To change states, lasing in the dominant laser can be stopped by injecting an external light at the dominant laser's lasing wavelength. A critical issue is the amount of coupling between the two lasers. The minimum amount of coupling between the lasers that is required to obtain bistable operation depends on the implementation, but the coupling should be strong (typically 40% or larger) [28].

An asymmetrically biased system of two coupled lasers (by setting the bias current differently for Laser 1 as for Laser 2) can also form an all-optical threshold function. As a result of this, Laser 1 injects a different amount of light into Laser 2 than the amount of light that Laser 2 injects into Laser 1. We assume that the amount of light that Laser 1 injects into Laser 2 is sufficient to suppress lasing of Laser 2. Hence, Laser 1 is the dominant laser. On the other hand, we assume that the amount of light that Laser 2 injects into Laser 1 is not sufficient to suppress lasing of Laser 1. If an additional amount of external light is injected into Laser 1, so that the combined power injected into Laser 1 exceeds the power required to suppress lasing, Laser 1 can be temporarily switched off. Hence, Laser 2 becomes the dominant laser as long as the external light is injected into Laser 1. As soon as injection of external light stops, the system switches back and hence Laser 1 becomes the dominant laser again. The system of two coupled lasers is now an optical threshold function (OTF) instead of an optical flip-flop memory.

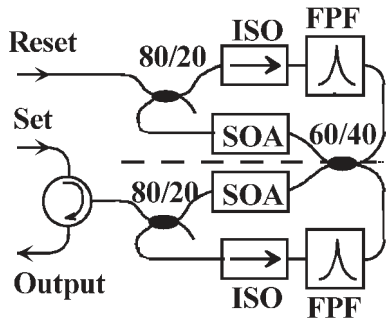

Fig. 15. Ring laser implementation of the optical flip-flop memory. SOA: semiconductor optical amplifier, ISO: isolator, FPF: Fabry–Pérot filter.

Fig. 15 shows the experimental set-up for an experiment to demonstrate the operation of the optical flip-flop memory. The two SOAs act as the lasers' gain media. In this particular set-up, a ring laser configuration is used. We have used FPFs with a bandwidth of 0.18 nm as wavelength selective elements. SOA 1 was pumped with 168 mA of current and SOA 2 was pumped with 190 mA of current. The pulses that were used to set and reset the flip-flop had a power of 2 mW. The optical spectrum of the flip-flops' output states is presented in Fig. 16. It is clearly visible that the difference in output power between the two states is over 45 dB. The switching characteristics of the optical flip-flop are presented in Fig. 17. It can be observed from Fig. 17 that if a sufficient external pulse is coupled in the flip-flop, the system changes states.

It should be noted that it is also possible to realize optical flip-flops by coupling other optical nonlinear elements than lasers. Examples are given in [29]–[31], in which flip-flop operation

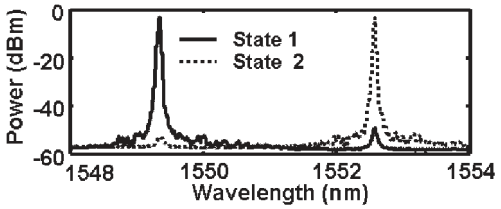

Fig. 16. Spectral output of two states of the optical flip-flop memory is presented. The solid curve represents the state in which laser 1 is lasing, and the dotted curve represents the state in which laser 2 is lasing.

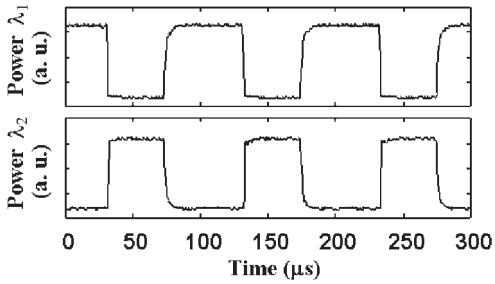

Fig. 17. Oscilloscope traces showing power of laser 1 and laser 2. Regular toggling between the states can be clearly observed.

is demonstrated by using coupled nonlinear Mach–Zehnder interferometers and coupled nonlinear polarization switches.

Photonic integration of optical flip-flops is essential for applications in optical networks. Integrated optical flip-flop memories should have fast (optical) set and reset times, operate at low power, have a high contrast ratio, and should have sufficiently small dimensions. An integrated optical flip-flop memory based on laser operation is presented in [32], but the power consumption, the size, and the switching speed of these devices remain an issue, which makes it difficult to couple them in large quantities as required in optical shift registers. A more promising AOFF concept based on two coupled microlasers is presented in [33]. This flip-flop concept has the potential to have the dimensions in the order of the wavelength of light, a switching speed of a picosecond, and a switching energy below a femtojoule. If one succeeds to interconnect these flip-flops, densely integrated digital optical logic operating at high speed and low power can be realized.

D. Tunable Wavelength Conversion and Packet Routing

In the LASAGNE node, a tunable wavelength converter receives the incoming optical packets and converts them onto the new wavelength channel set by the optical flip-flop blocks. With an AWG wavelength demultiplexer, routing of the optical packets can be further implemented. General system requirements on the optical wavelength converters include polarization insensitivity, broadband operating wavelength range, etc. More specifically, in LASAGNE node, two challenges are present for the SOA-MZI wavelength converters. First, the SOA-MZI is required have a large modulation bandwidth to perform the wavelength conversion of the RZ signals at 40 Gb/s or higher bit rate. Second, fast wavelength tunability requires the wavelength converter to have a tunable-filter-free configuration. In the node, the wavelength of the probe light is changing fast within several nanoseconds. A tunable filter cannot be optically controlled and tuned at such a high speed.

To fulfill the above system requirements, SOAs with fast gain recovery time are required and the configuration scheme of SOA-MZI also needs to be optimized. Generally, a single SOA-MZI can be dual-arm driven or single-arm driven by the modulating signals; it can also be configured to operate with either co-propagating or counter-propagating probe and modulating signals. The combinations of these operating modes result in various configuration schemes.

The differential driving scheme with co-propagating signals has the best modulation performance. Fig. 18 shows the calculated eye-opening penalty of a converted 40 Gb/s RZ signal in single-arm-driven and differential-driven modes. With the gain recovery time increasing beyond 30 ps, the SOA-MZI in the standard mode outputs nonreturn to zero (NRZ)-like eye diagrams and exhibits severe intersymbol interference (ISI). On the other hand, the eye opening of the output signal is generally acceptable as long as the gain recovery time is limited below 100 ps. Compared to the single-arm-driven mode, the differential mode greatly relaxes the requirements on the SOA's gain recovery time. However, the co-propagating configuration requires special waveguide design to realize the filter-free configuration [34].

The counter-propagation scheme is simpler to implement. More importantly, it is a filter-free configuration. However, the switching performance of the SOA-MZI is very sensitive to the SOA chip length in this scheme, and severe ISIs may be observed for high SOA lengths. Therefore, such a scheme requires the use of short chip length SOAs. Compared with the co-propagating case, this scheme has the same requirement on the SOA gain recovery time and has further requirements on the chip length, implying more challenges to fabrications of fast gain response SOA chips.

Another scheme is to construct the wavelength converter module using two cascaded SOA-MZIs, as shown in Fig. 19. This scheme features a tunable-filter-free configuration. The incoming 40 Gb/s pulses modulate the first SOA-MZI stage, transferring the incoming data onto the wavelength set by an internal CW laser. Then, the wavelength-converted signal is injected into the second SOA-MZI as the modulating signal. The second SOA-MZI also receives the CW signal generated by the optical flip-flops and transfers the modulating data onto it. At the output, a notch filter is used to filter out the light generated by the internal laser. In this way, the incoming 40 Gb/s pulses are finally converted onto the wavelength set by the optical flip-flop. Through using the filters with fixed center wavelength, this module is able to achieve fast tunable wavelength conversion. Due to the cascading configuration, the main disadvantage of this scheme is that the modulation bandwidth of the wavelength module is further degraded compared to that consisting of single SOA-MZI.

Each configuration has its own advantages and constraints concerning the network performance and functionalities. The above schemes of the SOA-MZI will be experimentally investigated with respect to its wavelength conversion performance in the LASAGNE network node.

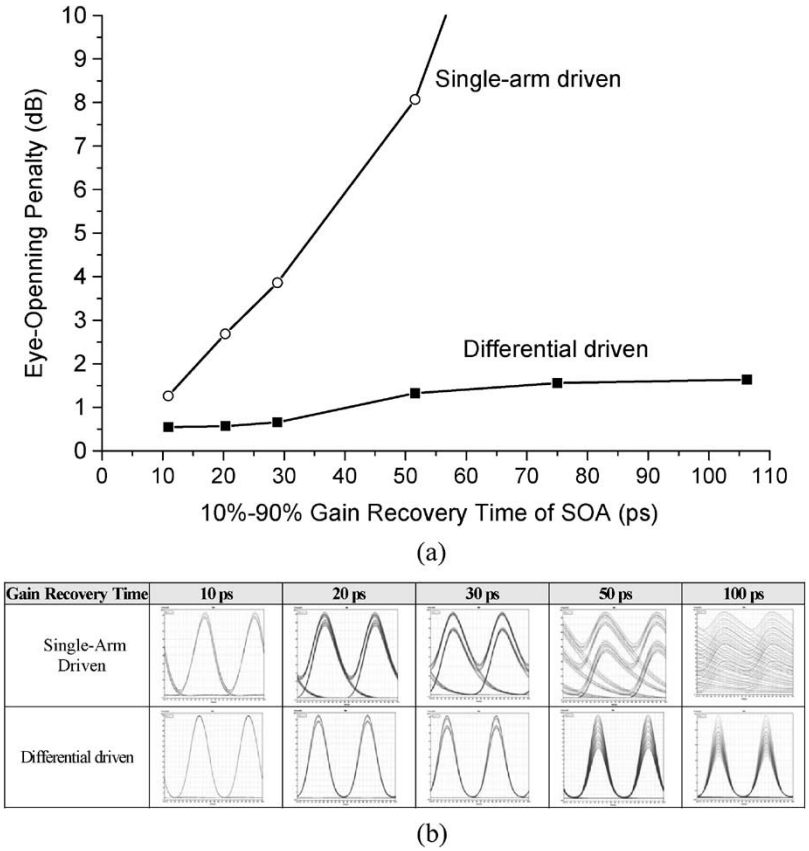

Fig. 18. (a) SOA 10%–90% gain recovery time versus eye-opening penalty. (b) Eye diagrams of a 40 Gb/s RZ signal.

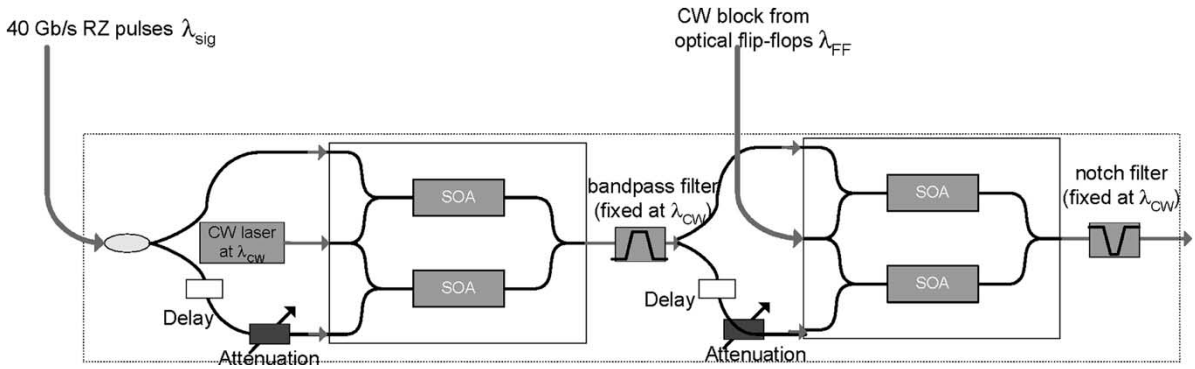

Fig. 19. Wavelength converter consisting of two cascaded SOA-MZIs. The two SOA-MZIs operate in the differential mode to achieve the optimum switching performance. The scheme features by a tunable-filter-free configuration.

V. LASAGNE AOLS Network

A. The Network Architecture

The AOLS solution proposed in LASAGNE is compatible with a number of different optical packet switching network architectures. In other words, the node design described in previous sections does not impose critical constraints to the network design. So the results of networking studies have a twofold impact: on one side they depict a "preferred embodiment" of the LASAGNE network; on the other side they may give a general contribution to the OPS research community.

The LASAGNE network is proposed as a single multiservice convergence technology in the core section of a European operator network. The preferred architecture is a connection-oriented solution with label swapping performed at every node. The basic forwarding entity is a virtual connection, named OPS label switched path (LSP), that is an optical analogy of an MPLS LSP or an asynchronous transfer mode (ATM) virtual circuit (VC). The basic data plane functionalities are label processing, label swapping, and packet routing. The optical header contains a label field used for forwarding purposes. A priority field has also been considered in order to accommodate contention resolution techniques that manage different priority levels. The use of optical label swapping in an all-optical packet switching network creates some challenges and opportunities from the networking point of view. On one hand, to lower the

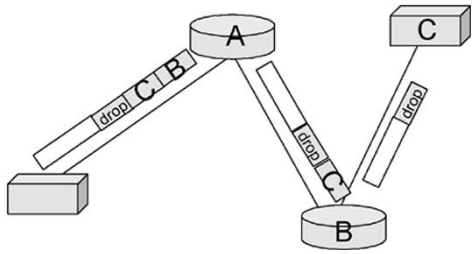

Fig. 20. Label stripping strategy.

cost of the AOLS node, it may be beneficial to reduce the number of different labels used throughout the network and hence the number of bits occupied by the label. Together with a reduction of the number of labels (or components), the project also targets to reduce the label length and thus the complexity of individual components. On the other hand, whereas an electronically implemented look-up table was easy to adapt to changing routing demands (i.e., LSPs are set up, broken down at all possible moments in the network), the number of all-optical components and how they are designed will be directly related to the dimensions of the routers (and thus the ability to accept more or fewer LSPs). Thus, the use of an all-optical packet switching poses restraints on the flexibility in routing and labeling the packets that should be well dimensioned. To this end, different label switching strategies are compared. The first label switching strategy proposed is based on the MPLS routing scheme. In an AOLS block, decisions are taken based on an incoming label and the incoming port. These are swapped into an outgoing label and an outgoing port. In the second label switching strategy (Fig. 20), a packet is switched through the network based on an end-to-end label. This label consists of multiple local labels. In each intermediate node, the AOLS block strips off the first bits of the end-to-end label (this is the local label) and makes a switching decision (i.e., to which output port the packet will be forwarded).

Both switching strategies are compared from a node dimensioning point of view. The dimension indicators that largely define the physical dimensions and implementation difficulty of the node are the following: 1) number of correlators: the number of correlators needed to distinguish the different possible incoming labels, counted per incoming port; 2) length of incoming ODL: the total number of ODLs needed to provide the local addresses multiplied by the delay line length of 1 bit and the number of bits in the incoming label. The node architecture requires for each possible incoming label a correlator and an incoming ODL. It is obvious that the more bits in a label and the more different labels a node has to distinguish, the more (and longer) ODLs and correlators have to be implemented. This makes the label stripping strategy less demanding on resources than label swapping because for label stripping the possible incoming labels are restricted to the number of outgoing ports in the node. This is confirmed by the dimensioning study, as can be seen from Fig. 21. Also, since the length of the labels can be shorter (fewer number of bits), the length of the incoming ODLs is much smaller, greatly reducing the amount of ODLs installed in the node. In Fig. 21, the results from the dimensioning study are depicted as a proportion of both switching strategies. We see clearly that label stripping needs fewer resources than label swapping. Although label swapping seems to be inferior to label stripping from a dimensioning point of view, we should take into account that the end-to-end label of label stripping induces much more overhead than the label swapping label [e.g., end-to-end label for label stripping $=$ 3 bits(local label) $\times$ 8 hops = 32 bits, instead of an 8-bit label for label swapping].

What has been described up to now is the "core part" of the OPS architecture. In order to accommodate client signals, a number of operations must be performed at the edge of an OPS network. We refer to these edge functionalities as "adaptation layer." The basic operation at the ingress/egress side is the insertion/extraction of client information in/from optical packets that implies the definition of a mapping procedure: client protocol data units (PDUs) are inserted on the payload of the optical packet together with some mapping information that allows the receiving node to extract the correct client PDUs. We refer to this kind of information as "edge header" or, because the insertion/extraction is supposed to be performed electronically, "electronic header."

Another important function that should be defined at the edge of the network when designing the interworking between client protocols and OPS is the translation of addressing information of client signals into addressing information of OPS network. The last consists of the LSP and the related label. So, basically, the said translation procedure is a table containing the relationship between data flow of incoming client signals and OPS LSP.

Two alternatives exist to implement edge functionality. The first one consists of the design of an edge node (see Fig. 1) that would basically be a core node with some client card added. This card is supposed to be an electronic card, and mapping, stuffing, and edge header generation are supposed to be realized there. Their outputs are OPS packets that are sent to the "core portion" of the node. Dense WDM (DWDM) interfaces in the edge node are used to connect it to core devices or to other edge devices. Interworking with client signals may be based on one of the two approaches depicted in Fig. 22, with reference to IP clients.

1) *Port-based mapping*: All traffic incoming from a client port is sent to the same OPS LSP. Note that this means that every IP router must have a dedicated connection to the OPS node for every other IP router that it is connected to. So the major drawback is that this approach is not optimal in terms of number of client interfaces.
2) *Client logic in the OPS node*: In this case, the OPS node has the capability of reading IP addresses of incoming packets and selecting different LSPs depending on them. The edge node becomes more complicated (please note that the same intelligence would be necessary for all client types) but this allows to reduce the number of router–OPS connections.

The second alternative is the definition of OPS interfaces in client equipment (Fig. 23). The feasibility of this approach would be constrained to the willingness of client equipment vendor to modify their devices, and it would strongly depend

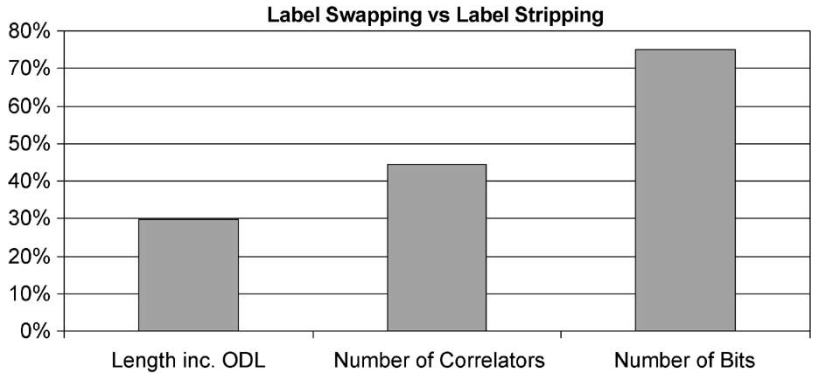

Fig. 21. Label swapping versus label stripping.

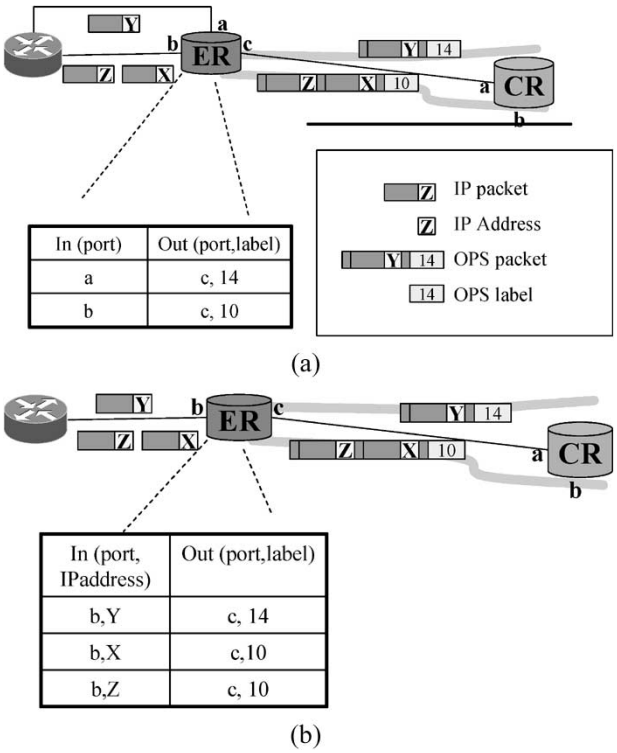

Fig. 22. OPS/client interworking with ERs. (a) Port-based mapping and (b) address-based mapping with client protocols logic in the edge device. ER: edge router, CR: core router.

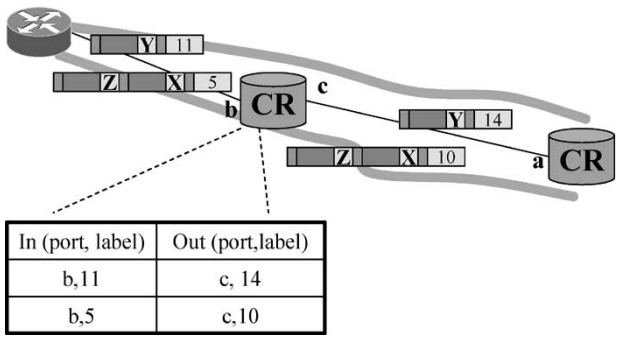

Fig. 23. Alternative approach: OPS interfaces in client equipment that implement adaptation layer functionalities.

on the success of the OPS technology and on its advance in standardization. From a technical point of view, the solution would have the following consequences.

1) OPS nodes would not care about mapping upper layer protocol addressing OPS virtual connections (OPS LSP).
2) The OPS node could definitely be an all-optical device, without the need of expensive electric client line cards.
3) Interaction between client and OPS devices would be required in terms of signaling for an OPS LSP setup.
4) Client/OPS interworking would be simplified, because client nodes would be able to forward packets on different LSPs depending on the IP addresses.

The establishment and the maintaining of OPS LSP require control intelligence in every node. This leads to the definition of an OPS CP. Through signaling protocols, CP instances of involved nodes communicate in order to manage the LSPs. Basic functionalities that would be needed are discovery, in order to allow every node to know its neighbors; routing, in order to make one node capable to choose the most convenient path for LSPs; and signaling for label distribution, in order to exchange information related to which label to use for a given LSP and to manage LSPs. Due to the high similarity between MPLS and OPS networks, approaches used in the MPLS world can be reused. In order to allow CP instances to communicate, an out-of-band approach, where CP messages use an independent network infrastructure, is preferred in an OPS framework due to the low bandwidth requirements of CP connections and to the drawback of the alternative in-band solution that would imply electrooptic conversion of OPS control packet.

In a more general network vision, it is straightforward to propose the integration of the OPS CP within the generalized multiprotocol label switching (GMPLS) framework [35], which would consist of the definition of a new switching capability [optical packet switching (OPSC)].

B. Migration Scenarios

In this section, we will discuss the benefits of using all-optical packet switching in mixed packet/circuit network architectures. In the following, three approaches are described. The former is a transitional stage, the latter two form a solution to combine the benefits of both packet switching and circuit switching.

The first examined migration scenario is the one depicted in Fig. 24. Even if the OPS network is supposed to carry every type of client traffic, the connection of client equipment to OPS

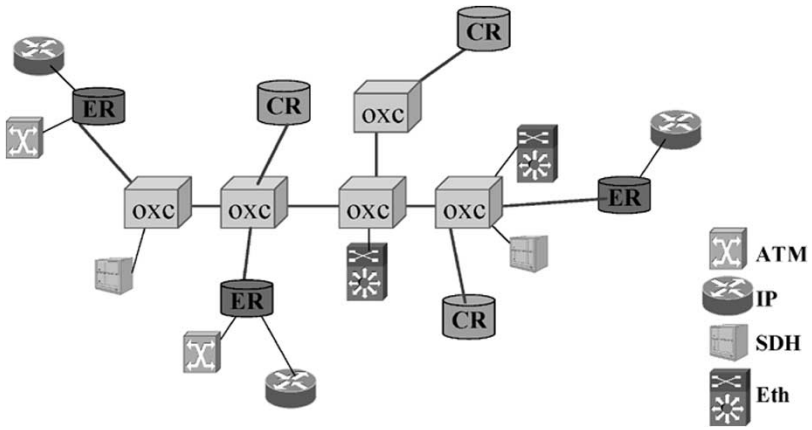

Fig. 24. Example of a migration scenario where some clients have migrated in the OPS network while others are still connected through a circuit network.

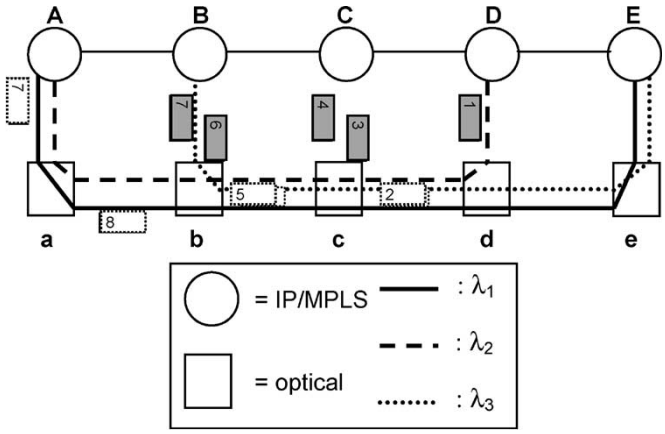

Fig. 25. Example wavelength-switched network to demonstrate the ORION functionality. Capital letters denote IP/MPLS routers, while small letters denote the OXCs. Packet flow is indicated by the numbers in the packets.

ERs would need a certain amount of time and the definition of a migration policy while migrating from a truly circuit switched network to a purely OPS network. In this transient, there would be some clients that would already use the OPS network while some others would still be connected through a circuit-based backbone. For example, in Fig. 24, a migration scenario is depicted, where ATM and IP client equipment are connected through the OPS network (ER, CR) while SDH and gigabit Ethernet client equipment are connected through an optical cross-connect (OXC)-based network.

The second mixed scenario is somewhat the same as the previous one. A separate OPS and wavelength-switched network uses separate wavelengths, but on the same physical network infrastructure. The basic idea is that traffic gets sent over the wavelength-switched network if capacity is available. If there is a shortage on the wavelength-switched network, the surplus traffic gets sent over the OPS network. This would allow the wavelength-switched network to carry at least very static traffic, while if there are variations and burstiness the OPS network can handle it. Meanwhile, it would lower the size requirements of the OPS nodes, but still improve efficiency a great deal.

Based on the previous scenario, a hybrid approach called ORION is proposed as the third migration scenario. Basically, this takes the previous one step further, allowing the (O)PS network and the wavelength-switched network to share resources at wavelength level. We will explain the core features of the ORION network concept (for a more detailed description of the design, we refer to [36]). The basic idea in ORION is to start from a wavelength-switched WDM network, where some wavelength paths are established. In a normal wavelength-switched network, a lightpath passes some node transparently, i.e., the node cannot access the data in the passing wavelength. In the example of Fig. 25, node D has no access to the IP packets traveling in wavelength λ_1. Only wavelengths starting or terminating in that node can be accessed. Suppose we have the connections A-a-b-c-d-D on λ_2, B-b-c-d-e-E on λ_3, and A-a-b-c-d-e-E on λ_1, established as indicated in Fig. 25. The basic problem with wavelength switching occurs in the following scenario: when the capacity of the lightpath AD is fully used, and there is some temporary overload for this connection, the wavelength λ_1 cannot be used to carry some of its traffic, as it is dedicated for connection AE. It is, however, perfectly possible that the lightpath AE (on λ_1) is only carrying a low traffic load, so that in fact at some moments in time it is empty (assuming IP directly over WDM). Thus, while connection AD has a capacity shortage, AE has capacity in abundance. While ordinary wavelength-switched WDM networks cannot solve this type of situation instantly, ORION enables the network to use this capacity on λ_1 (normally dedicated to the connection AE) for the connection AD by switching to the so-called overspill mode, which essentially is an operation of the network as if it is a point to point WDM network. This is implemented as follows: packets (belonging to connection AD) are inserted in λ_1 (normally dedicated to connection AE). We call this overspilling, hence the name Overspill Routing In Optical Networks (ORION). Thus, packets inserted in a wavelength different from the lightpath of the connection are called overspill packets. Packets that are sent on their correct lightpath are lightpath packets. When packets of connection AD are inserted in λ_1, node b has to be able to detect these, get them out, and let B handle them. They have to be routed further to their destination, which, in this case, is possible by sending them out again as overspill packets on λ_3 (or again λ_1). At node c, they need to get lifted out again and be handed over to C, which does the same. In our case, they are sent out again

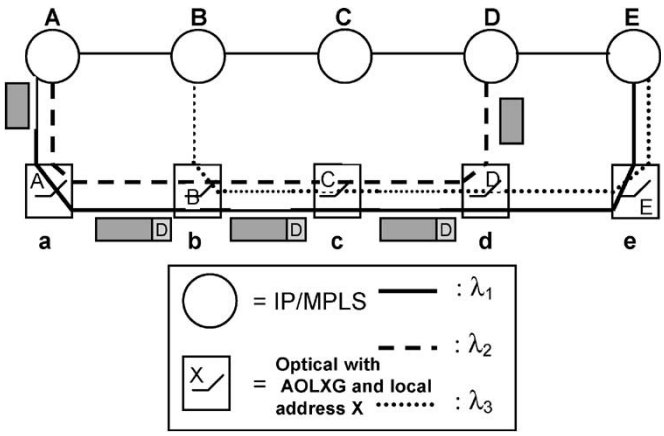

Fig. 26. ORION approach, developed with all-optical switching functionality.

as overspill packets, again on λ_3 or λ_1. The packet flow can be seen in Fig. 25. Packets in gray travel on an ORION interface (see further) between the OXC (b) and the IP/MPLS router (B).

By using all-optical packet switches, we could improve this concept. For now, the overspill packets are brought to the IP routers in each intermediate node of their overspill itinerary. However, when a packet is put on an overspill mode, the destination address is known and the IP router often decides to put the overspill packet again on the same lambda. Beneficial to the concept of overspill routing would be to avoid the intermediate optical–electrical–optical (O/E/O) conversions and to keep the overspill packets optical during their overspill itinerary. To this end, we propose to add an all-optical label in front of the IP packets. In each intermediate node, an AOLXG checks this label. A label match with the local address for the intermediate node sends the packet to the IP layer where the IP router is responsible for the further routing. Fig. 26 visualizes this and we retake the above example. λ_1, dedicated to lightpath AE only, carries low traffic load, while $\lambda_{2,}$, connected to AD, is overloaded. Some of the packets on AD go in overspill on λ_1 and get an optical label with the destination address (D). In b, the label is checked. Since B is not the destination address of the overspill packet, the packet is all-optically switched to c. In d, the label and the local address of d (D) match, and the packet is taken from λ_1 to the IP router. To check the label all-optically, an AOLXG containing the local address of the IP router attached to the optical switch is implemented.

VI. Summary

The main results obtained during the first year of the all-optical LAbel SwApping employing optical logic Gates in NEtwork nodes (LASAGNE) project were shown in this paper. This project aims at designing and implementing the first, modular, scalable, and truly all-optical photonic router capable of operating at 40 Gb/s in an all-optical label swapping (AOLS) network. To implement the AOLS node functionalities, the use of all-optical logic gates and optical flip-flops was proposed. Simulation and experimental results on all-optical packet clock recovery, packet-rate clock recovery, label and payload separation, label comparison, and tunable wavelength conversion were obtained, showing that semiconductor optical amplifier-based Mach–Zehnder interferometer (SOA-MZI) can be employed as a basic functional block to achieve a flexible and scalable approach in terms of manufacturing. Furthermore, an appropriate network architecture for this AOLS scenario was proposed, as well as adequate migration scenarios from current circuit-switched networks towards the LASAGNE scenario.

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