Iterative Built-In Testing and Tuning of Mixed-Signal/RF Systems

Invited Paper

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Abstract—**Design and test of high-speed mixed-signal/RF circuits and systems is undergoing a transformation due to the effects of process variations stemming from the use of scaled CMOS technologies that result in significant yield loss. To this effect, post-manufacture tuning for yield recovery is now a necessity for many high-speed electronic circuits and systems and is typically driven by iterative test-and-tune procedures. Such procedures create new challenges for manufacturing test and built-in self-test of advanced mixed-signal/RF systems. In this paper, key test challenges are discussed and promising solutions are presented in the hope that it will be possible to design, manufacture and test "*truly self-healing*" systems in the near future.**

I. INTRODUCTION

The use of scaled CMOS technologies for high speed wireless and wired communications devices running at speeds of 10-100 GHz is posing daunting technological challenges both in design and manufacturing test (necessary for reduced product cost). A key problem is that the circuits concerned are increasingly susceptible to manufacturing process variations [1] resulting in *loss of manufacturing yield.* The effects of such process variations on the performance of high speed mixed-signal/RF circuitry manufactured using deeply scaled (60nm and below) CMOS technology is particularly severe, requiring the use of post-manufacture tuning for yield recovery.

In general, negative feedback is used as standard practice in the design of analog circuits to provide stability and resilience to process variability effects [2, 3]. However, in RF circuit's continuous feedback based stabilization techniques generally result in a compromise of available device bandwidth. One way to resolve this issue is to run iterative tests on the device under test (DUT) and to use the results of the applied tests to determine the best way to "tune" the DUT under the assumption that special hardware "tuning knobs" are designed into the DUT specifically for tuning purposes. After the best settings of all the tuning knob values are determined, these are programmed into the hardware on a permanent basis (e.g. via use of fuses) or can be reset via digital mechanisms to allow field calibration of the DUT. In the recent past, *digitally assisted* test and tuning techniques have been applied to a variety of mixed-signal/RF circuits. In this design paradigm, on-chip digital logic is used to intelligently compensate for loss of mixed-signal/RF performance due to process variations. In this context, there has been significant work in the area of digitally-assisted tuning of analog circuits including PLLs, frequency synthesizers, and digital radio [4-7]. In [8], a digitally-assisted algorithm for testing the IIR spec of a Weaver image-rejection receiver is presented. In [9], algorithms are used to perform digitally-assisted ENOB test of pipelined data converters. In [10], digitally assisted data converter architectures are discussed. As evident from the above discussion, most of this research focuses primarily on testing and tuning of *specific* (or few) analog/RF/ADC specs. This requires the design of on-chip circuitry that is *specific to the targeted performance metrics* of the device under test (DUT). In general, the larger the number of specifications to be measured on-chip, the larger the amount of on-chip circuitry needed to support the associated test measurements. Solutions need to be found that are *scalable across a multitude of (complex) specifications* without incurring additional hardware cost. In the following, key test challenges and potential solutions are discussed.

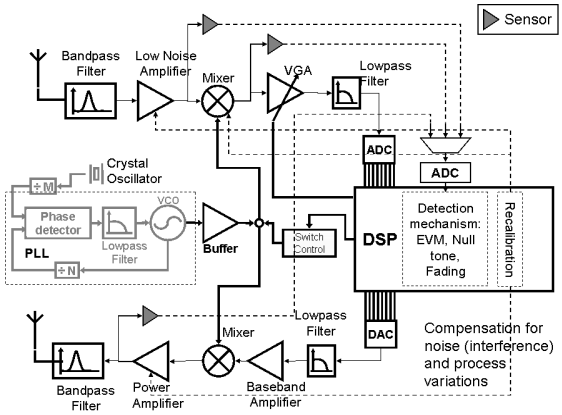

Figure 1. Test and tuning architecture.

II. KEY CHALLENGES

In order for post-manufacture tuning of mixed-signal SoCs to be economically feasible, it is necessary that *testing and tuning* of the same be accomplished in an amount of time not much larger than the time taken

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to just *test* the system as per current practice. Figure 1 shows a proposed [11] testing and tuning architecture for an OFDM transceiver.

The test architecture of Figure 1 consists of sensors designed into the RF signal path to monitor the quality of signals at different internal test points in response to test stimulus applied from the baseband DSP. The sensors used include envelope, peak or rms detectors and other special test response feature extractors [11]. In test mode, either OFDM-modulated signals or carefully designed multi-tones are applied to the transmitter and the signals "looped back" to the input of the receiver to be analyzed by the baseband digital signal processor (DSP). Figure 1 does not show the loop-back path, but such loop-back may be performed via an external frequency translation circuit (mixer) located on the tester load-board or integrated into the device package. Algorithms running on the DSP are used to analyze the looped-back test response from the receiver as well as data from all the embedded sensors to tune the individual circuit components using an iterative test-tune-test procedure. Tuning consists of adjusting the bias currents/voltages of the mixers, power amplifier (PA) and low noise amplifier (LNA) among other tuning parameters so that transmitter and receiver noise and linearity specifications are met. In order to minimize test and tuning time the following characteristics of the test and tuning infrastructure are desirable.

(a) The ability to measure *multiple RF specifications* of embedded devices using a *single* data acquisition (or few acquisitions).

(b) The ability to perform test and tuning autonomously with little or no external RF test equipment support and *minimal on-chip hardware overhead* (and consequently *minimal impact on device performance).*

(c) The ability to ensure near-optimal tuning avoiding local minima (with regard to a performance based cost function) with the *least (negative) impact on device power consumption*.

With regard to (a), it is worthwhile to point out that existing tuning techniques generally support testing/tuning of *a design specification at a time*. For each such tested specification, dedicated on-chip hardware or external RF test equipment with appropriate test access is used. To complicate matters, tuning is usually accomplished using *iterative procedures* that need *repeated test measurement* of multiple specifications across as many as 50 tuning iterations. Through each iteration, *multiple design specifications must be monitored* as it is not possible, in general, to control multiple design specifications *independently* with a limited number of design tuning parameters. Hence, *tradeoffs between design specifications must be considered* during the tuning procedure.

With regard to *manufacturing yield enhancement,* it is important to point out that it is *not necessary* to ensure that every time tuning is performed, the *exact globally optimum design specifications are achieved*. It is only necessary to ensure that *in the majority of cases*, the design specifications are *significantly improved* to enable large yield recovery. Of course, the more accurate the test and tuning procedure, the higher the resulting yield.

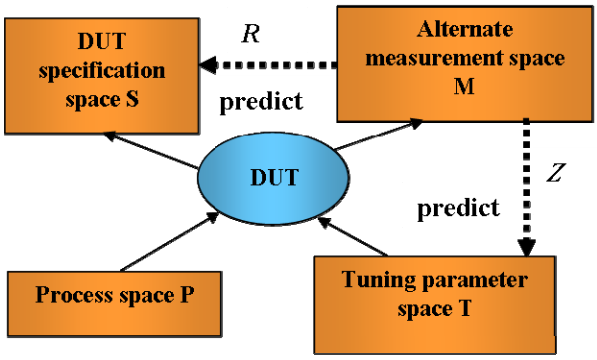

Figure 2. Tuning via supervised learning.

III. PROMISING SOLUTIONS

A. Learning Driven Tuning Algorithms

Consider process variations in the process parameter space **P** of Fig. 2 that affect the specifications of the DUT. In the *alternate test methodology* [12], a measurement space is defined in such a way that any perturbation in **P** that affects the specifications of the DUT in its specification space **S,** also affects a set of alternate measurements **M** (that are easier to make than measurement of the original specifications **S)**. In general, this can be ensured only in a *statistical sense*, hence a *high correlation* between the alternate test measurements **M** and the DUT specifications **S** is desired under stated process variations **P**. If such high correlation is achieved, then the specifications **S** can be predicted from the (low cost) measurements **M** using nonlinear regression based mapping functions ***R*** derived using *training* [12] algorithms. Note that with regard to the architecture of Figure 1, the measurements **M** consist of the loop-back received data in response to an applied test as well as data from all the embedded sensors designed into the various test nodes.

Now consider a statistically significant number of samples of the DUT across the entire range of process variations that are tuned accurately in a power-conscious manner using a known tuning algorithm that effectively avoids local minima. For each device in the process space **P**, there exists an alternate measurement

M for the untuned DUT. If each such DUT is tuned using the above tuning algorithm, then a set of tuning parameter values **T** is obtained corresponding to each alternate measurement **M** of the untuned device. Consequently, a regression mapping ***Z*** is built using training algorithms that is used to directly predict the best tuning parameter values **T** for each DUT directly from the alternate test measurements **M** made on the untuned device. The alternate test applied must satisfy certain mathematical conditions for the mappings ***R*** and ***Z*** to be feasible. A detailed discussion of this is beyond the scope of this paper but some results are shown below for an LNA. Note that the tuning procedure is not iterative and can be performed via *single* test application [13].

1) Learning Driven Tuning: Test Case: A CMOS LNA with folded PMOS IMD sinker [14] was used as a test vehicle and was designed in TSMC 0.25um CMOS technology. Its simplified schematic is shown in Fig. 3. Two tuning knobs were employed to control the programmable bias of the transistor M_1 and M_p. A fabricated self-tuning chip (different design, TSMC 0.25um CMOS) is shown in Figure 3 as well.

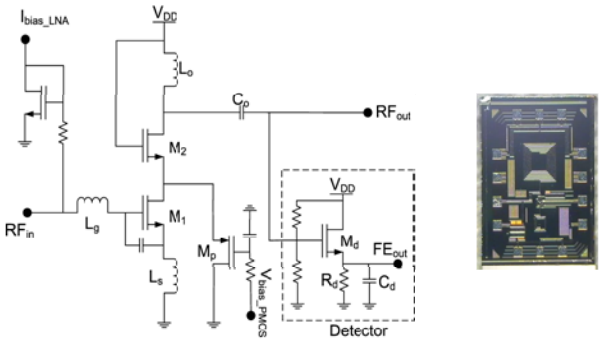

Figure 3. CMOS LNA test vehicle.

A two-tone sinusoidal waveform was utilized as the test stimulus (-20dBm at ± 5MHz offset from the center frequency 1.9GHz). Hence, the fundamental frequency of the envelope response of the envelope detector sensor at the output of the LNA as shown in Figure 3 was placed at 10MHz. The specifications of the LNA were extracted from the envelope detector output. Figure 4 shows the histograms for NF and Idd of the LNA before and after tuning. It is seen that across multiple specifications (NF, TOI, S21, Idd), yield is improved from 41.8% to 93.3%.

B. Implicit Tuning Using Golden Signatures

In the implicit tuning methodology, a "golden" signature [15] is determined in such a way that the signature is maximally sensitive to *any perturbation in the process or the tuning knob values that also affect the DUT's specifications*. The signature above consists of the DUT response to the applied test stimulus as well as the response obtained from any sensors inserted at internal test points of the DUT. Once such a signature is determined (via simulation and hardware calibration), *no training algorithms are needed* (in contrast to the discussion of Section 3.1). Tuning is performed to *minimize the difference* between the golden and observed signatures and when this difference is minimized, the tuning procedure terminates. Figure 5 shows error count (error count = difference between golden and observed signature) vs. no of iterations of a modified SS-LMS algorithm used for tuning a transmitter on the left. An envelope detector at the output of the transmitter is used to generate the test response signature (down-convert from RF to baseband). On the right, improvement in IIP3 is shown as a function of the number of tuning iterations. The mixer and PA bias currents were used as tuning knobs in this experiment.

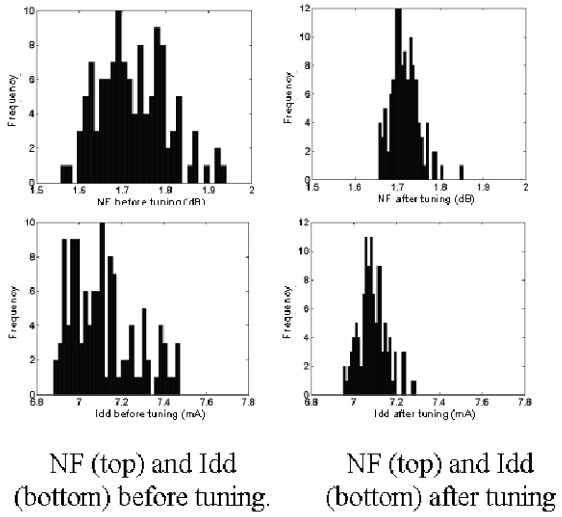

Figure 4. Yield histograms for NF and Idd.

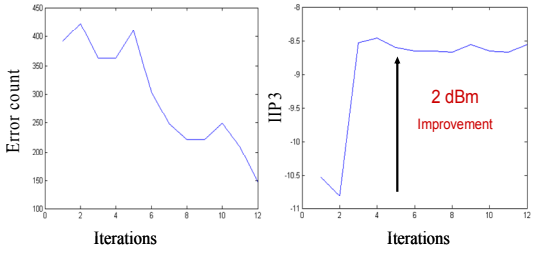

Figure 5. Implicit tuning of transmitter for IIP3.

C. Concurrent Tuning Using Specification Prediction

1) Tuning of Narrow Band Systems: For a given RF system, let $K = [K_1, K_2 \ldots K_N]$ be a vector describing the values of N control knobs. These control knobs may include *digital predistortion* parameters in the

baseband also. For a process-perturbed device, the tuning algorithm first makes a *power-aware intelligent initial guess of the value of K* using the learning based tuning technique of Section 3.1. The complexity of the training procedure here is traded off for simplicity allowing an approximate solution to be generated that is close to the global minimum. Then, starting from this initial guess, a *steepest descent gradient search algorithm* [16] is used to minimize a cost function that represents the difference between the desired and the observed performance specifications of the RF system. This cost function requires the use of alternate test based specification prediction using the mapping ***R*** of Figure 2. Training algorithms are needed to generate this mapping as discussed before. The search algorithm is used to determine the "next" tuning knob values at each iteration of the tuning procedure. For these tuning knob values, the alternative tests are rerun, the cost function recomputed and the procedure repeated until convergence is achieved. As an example, the cost function may be implemented as a weighted sum of the performance metrics along with their guard bands (Gb). In Equation 1, S^j_i denotes the 'i^{th}' specification for the j^{th} control knob setting; Snom denotes the nominal specification value; W denotes the weight assignments for individual performance metrics. By assigning appropriate weights, the proposed cost can be manipulated to achieve different trade-offs between multiple performance metrics for overall yield improvement.

$$\sum_{i=1}^{K} W_i * \left(1 - \frac{S_i^j}{Snom_i - Gb_i}\right) * \left(1 - \frac{S_i^j}{Snom_i + Gb_i}\right) \quad (1)$$

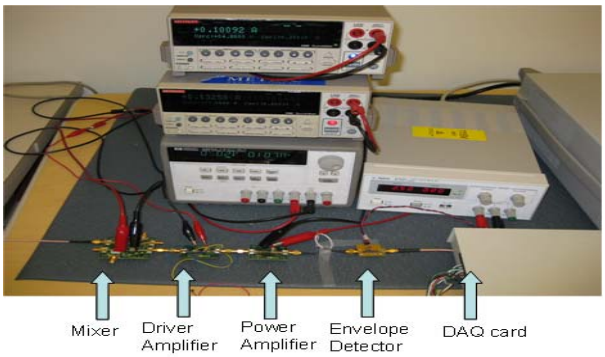

Figure 6. Self-tuning receiver prototype.

Alternatively, gradient descent search (converges in 5-10 iterations) may be performed from randomly selected starting points to avoid local minima in a probabilistic sense. The cost function computation and the execution of the search algorithm are performed by the baseband DSP of Figure 1 and the best solution obtained is used to determine the final value of the tuning parameters. Note that for several performance-equivalent solutions that are computed, the most power-optimal solution is selected. This is possible by a computing a power cost (different from Equation 1) from knowledge of power consumption of all the RF modules as a function of their tuning knob values. Note that this methodology meets all the objectives (a), (b) and (c) discussed in Section 2. Particularly, since multiple specifications can be computed rapidly and accurately through the tuning procedure, the latter is fast and the specifications themselves can be *traded off against one another* through the tuning process.

TABLE 1	Gain	IIP2	IIP3
Nominal	29dB	-12dBm	-16 dBm
Upper bnd	31dB	-10dBm	-14dBm
Lower bnd	27dB	-14dBm	-18dBm
Before	36dB	-18dBm	-21dBm
After	28dB	-12dBm	-15.9dBm

Table 1 shows Gain, IIP2 and IIP3 specifications for a 2.4 GHz receiver and values before and after tuning. Figure 6 shows the experimental setup. Figure 7 below shows yield histograms for a selected population of transmitter devices across the Gain, IIP2 and IIP3 specifications.

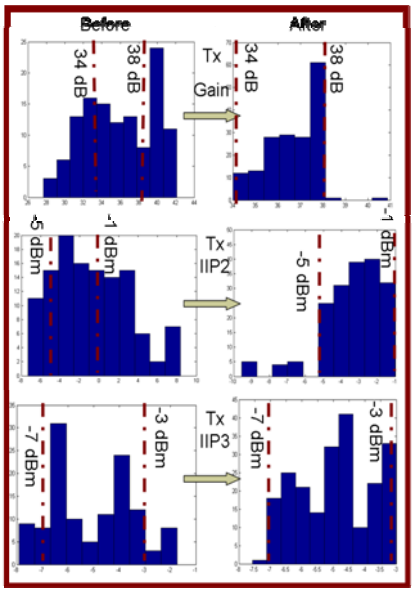

Figure 7. Transmitter Gain, IIP2 and IIP3 histograms (top to bottom), with (left) and without (right) post manufacture tuning.

2) Digital Compensation of Wide Band Systems: In [17], a methodology for tuning wideband RF devices employed in UWB systems is developed. The proposed transmitter architecture of MB-OFDM UWB systems is shown in Fig 8. The ECMA 368 standard defines the

physical and the medium access layers of the MB-OFDM UWB system. The frequency spectrum of 3.1-10.6 GHz is divided into 14 bands consisting of 6 Band groups. The bandwidth of each band is 528 MHz. Time–frequency coding with time-frequency interleaving determines the manner of frequency hopping from one band to the other. To transmit data in each band, OFDM modulation consisting of a 128 point IFFT is employed using 100 data carriers, 10 guard tones, 12 pilot tones and 6 NULL tones. The implementation of MB-OFDM UWB front end necessitates that the devices work over several GHz of frequencies. Some companies have started providing complete RF front-end solutions covering the complete UWB band of 3.1 to 10.6 GHz. Present day wideband design capabilities provide for in-band variations (528 MHz) to lie within certain tolerance limits. Nevertheless, due to power consumption constraints there is always significant inter-band variation. In MB-OFDM the Local Oscillator (LO) sweeps between any two specified frequency bands within a short interval of time ranging in nanoseconds. So the baseband signal experiences different transfer characteristics if the inter-band variation is significant, which in turn increases the effective non-linearity of the system. This end to end nonlinearity can be reduced if the inter-band variation is reduced by intelligent frequency dependent compensation.

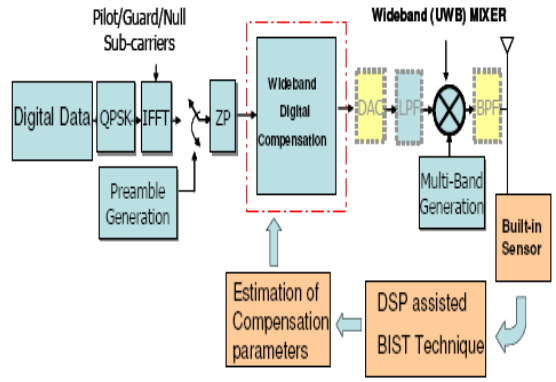

Figure 8. MB-UWB system with digital compensation.

Since UWB devices have low output power, the primary device in a UWB transmitter is the up-conversion mixer. Digital compensation can be performed in two ways. First, a different predistorter synchronized with the local oscillator can be used to provide transfer function linearization at different frequency bands (called *multi-way* compensation). To implement this, a multi-tone signal is fed to the transmitter from the baseband and the response from the envelope detector (built-in sensor of Figure 8) is analyzed in the baseband to predict the transfer function of the mixer (Gain, IIP3) at the different UWB frequencies of interest (3 – 7 GHz), This is used to design a predistorter for each corresponding frequency band that predistorts the baseband signal by the inverse of the predicted transfer function of the mixer. As discussed before, the resulting predistorters are synchronized with the LO signal to provide transmitter linearity across a wide frequency range. A second approach is to use a single predistorter that reduces worst case nonlinearity at one frequency at the cost of marginally increasing the nonlinearity at another. The latter is called *unified* compensation. Figure 9 shows EVM improvements due to multi-way compensation and Figure 10 compares EVM values without digital predistortion compensation, with multi-way compensation and unified compensation.

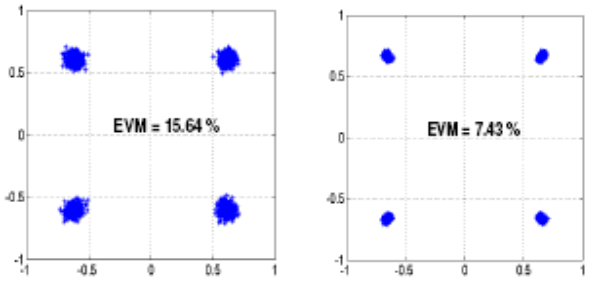

Figure 9. EVM with (left) and without (right) multi-way compensation for QPSK modulation.

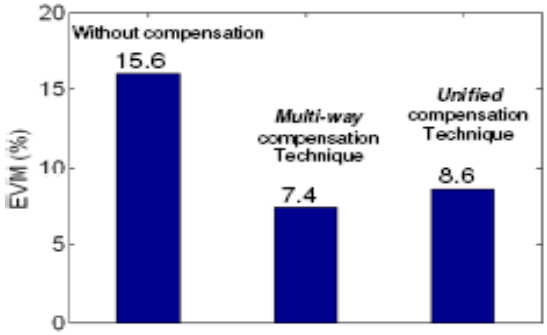

Figure 10. EVM values with and without different compensation schemes.

D. Self-Tuning Based on Oscillation Principles

This methodology is proposed to overcome the need for external RF test stimulus because the stimulus is generated by the DUT itself with the help of additional circuitry [18]. This additional circuitry is a feedback loop that causes the DUT to oscillate resulting in a signal whose frequency is related to the performance of the DUT. The value of this frequency is correlated with the specifications of the device such as Gain and IIP3 and is used to accurately predict the same. Subsequently, compensation for loss of DUT performance due to process variations is performed by adjusting calibration/tuning knobs designed into the DUT from knowledge of its specification values using either an iterative procedure or one that involves solving a system of equations. This calibration knob

manipulation is driven by analysis of the self-generated output (referred to as the DUT *signature*) from the DUT as shown in Figure 11. The output signature of the DUT is analyzed with on-chip available resources (RF mixer, ADC and DSP) enabling self-test as well as self-correction of the embedded LNA. Note that the frequency of oscillation of the LNA is downconverted from RF to baseband using a mixer for analysis. A distribution of such frequencies for a set of sample DUTs is shown in Figure 12.

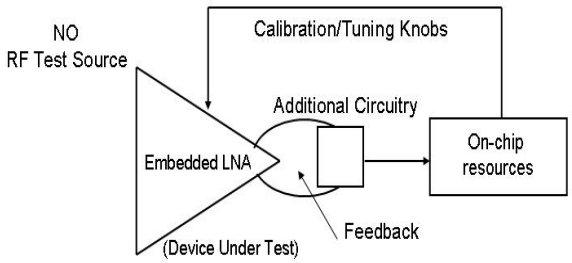

Figure 11. Proposed self-healing architecture based on oscillation principles.

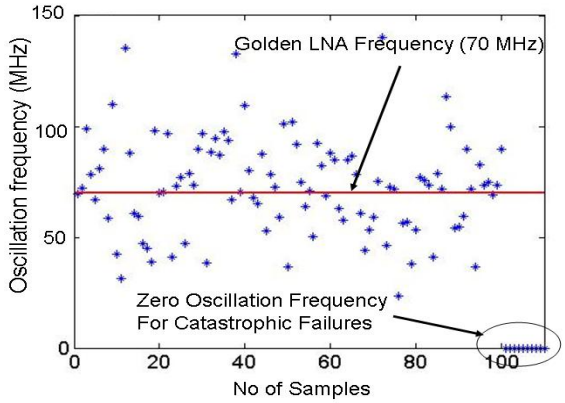

Figure 12. Oscillation frequency of various LNA samples.

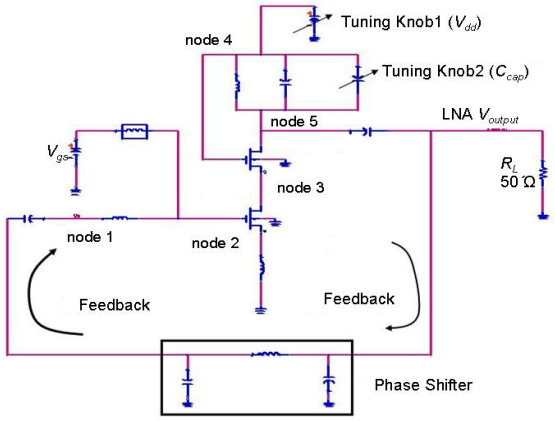

Figure 13. LNA Model.

1) RF LNA: Test Case: To demonstrate the proposed self-healing methodology based on oscillation principles, a 900 MHz cascode LNA (Gain = 9.5 dB, P1dB = -3.38 dBm) with source degeneration was designed in a CMOS 0.18 um process. In this LNA, two tuning knobs were used - one to change the capacitance (C_{cap}) in the LC tank and the other to change the power supply (V_{dd}). Figure 13 shows the simulation setup for the LNA using a phase shifter to enable the LNA to oscillate. This enables the generation of a test signature without any input test stimulus. Figure 14 shows the histograms for P1dB and Gain of the LNA before and after tuning. It is seen that individual yield for Gain improves from 91% to 100% and individual yield for P1dB improves from 92% to 99%.

As a proof of concept, a hardware prototype of the proposed self-correcting LNA was built using commercially available LNA as shown in Figure 15 [18].

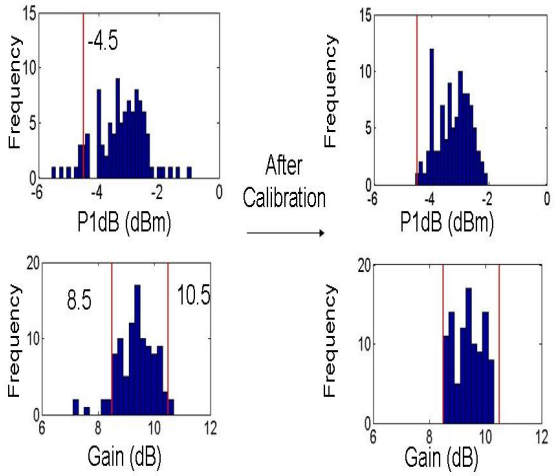

Figure 14. Specification distribution before and after calibration using Knob1and Knob2.

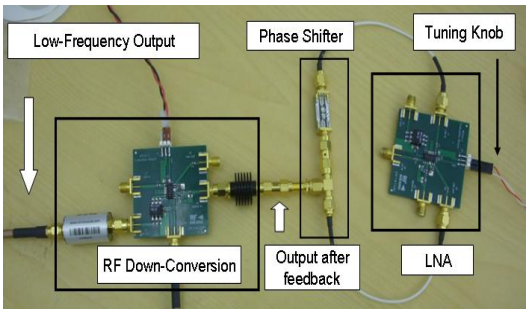

Figure 15. A hardware prototype of the proposed self-healing LNA based on oscillation principles.

IV. A NOTE ON SENSORS AND SPECIFICATION PREDICTION

The above discussion is predicated on the fact that a multitude of complex test specifications of the DUT can be predicted by analysis of the response of the DUT to a suite of carefully determined multi-tone signals using training algorithms. A test generator is used to determine the multi-tone signals in such a way that the response obtained from the envelope detection or other sensors shows *strong correlation* with the specifications of the DUT. Various algorithms have been investigated for this purpose: genetic, gradient search, etc, algorithms [12,19,20]. Once regression models are constructed using the training algorithms, it is not necessary to run the original specification tests on the DUTs but rather the optimized multi-sine *alternate tests* and directly predict all the DUT specifications from the resulting *single* data acquisition. To prove this, a hardware prototype of the transceiver of Figure 1 was built and is shown in Figures 16 below.

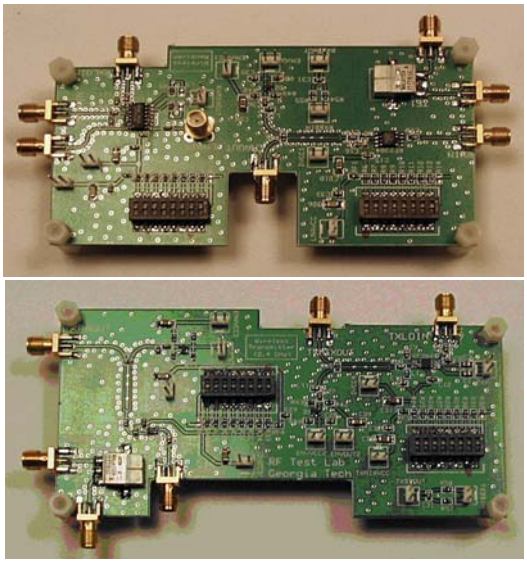

Figure 16. 1.575 GHz transceiver with receiver (top) and transmitter (below).

Envelope detection sensors were designed [21] into the output nodes of the mixers, LNA and PA and data from these sensors were used to predict transmitter, receiver and module specifications. Mechanisms for degrading the performances of all the RF modules using Vdd control were designed into the board (see DIP switches in Figure 16. Figure 17 shows the envelope detector output for various DUTs with different specifications.

Figures 18 and 19, show predicted (y-axis) vs. measured (x-axis) OIP3 for the transmitter subsystem and the receiver LNA. The targeted specifications for the transceiver included the OIP3, S21 and P1dB specifications. In other experiments, tracking for complex specifications such as EVM, ACPR, modulation SNR, etc., has also been demonstrated [22].

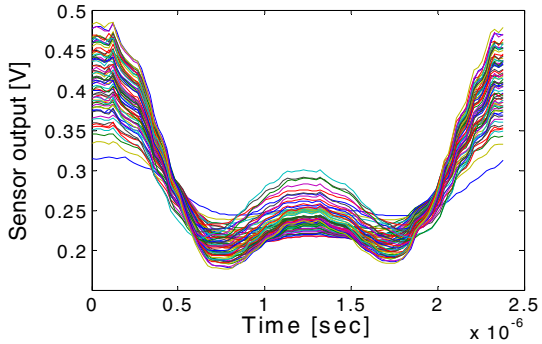

Figure 17. Response of envelope detector.

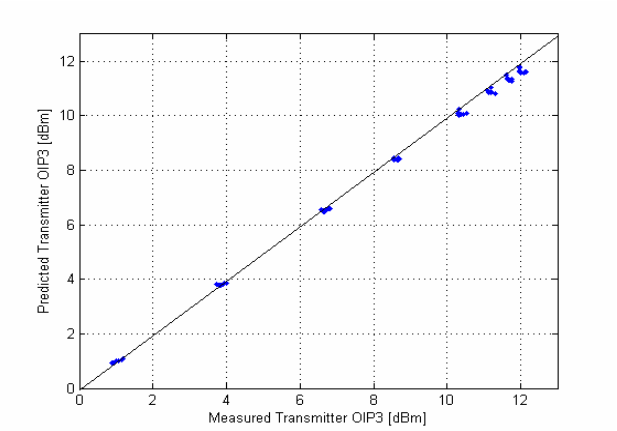

Figure 18. Predicted vs. measured transmitter OIP3.

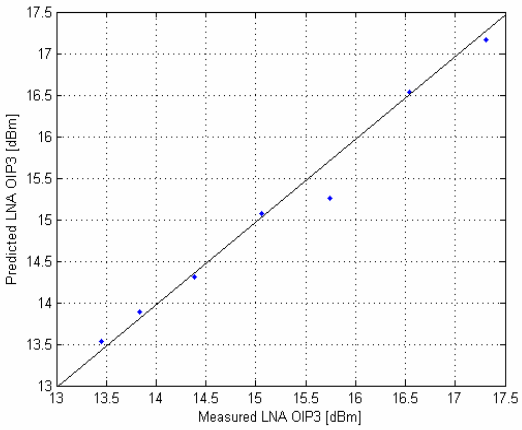

Figure 19. Predicted vs. measured LNA OIP3.

V. FUTURE DIRECTION AND CONCLUSIONS

The techniques described in Section 3.1, 3.2 and 3.3 can be "mixed and matched" to solve different

variations of the iterative testing and tuning problem for mixed-signal/RF systems. Regardless of the specific tuning algorithm used, a key issue is that it must be made immune to sensor and feedback circuit nonidealities. For DUTs with field tuning capabilities the verification and test algorithms must ensure that not only are all the DUT's specifications met after manufacture but also that tuning procedures react appropriately to failures/parametric deviations as they happen in the field.

ACKNOWLEDGEMENT

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