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Research Article

Keywords: Junctionless, GAA nanowire FET, Spacer length, ION/IOFF, SS

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Junctionless Gate-All-Around Nanowire FET with Asymmetric Spacer for Continued Scaling

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Abstract:

In this paper we have performed scaling performance of asymmetric junctionless (JL) SOI nanowire FET at 10 nm gate length (L_G). To study the device electrical performance various DC metrics like SS, DIBL, I_{ON}/I_{OFF} ratio are performed. Even at 5 nm, the device has good electrical properties with subthreshold swing (SS) = 64 mV/dec, drain induced barrier lowering (DIBL) = 45 mV/V, and switching ratio (I_{ON}/I_{OFF}) = 10^6 shows a higher level of electrostatic integrity. Moreover, to study scaling flexibility towards analog/RF applications various parameters like transconductance (g_m), transconductance generation factor (TGF), total gate capacitance (C_{gg}), and cutoff frequency (f_T) are determined. Furthermore, the dynamic power (DP) and static power (SP) consumption of the device with scaling is also presented. The findings of the study show that asymmetric JL nanowire FET is one of the scaling possibilities.

Keywords: Junctionless, GAA nanowire FET, Spacer length, I_{ON}/I_{OFF}, SS.

1 Introduction:

The use of stacked nanowire field-effect transistors (NW-FETs) as a scaling alternative for CMOS technology has been proposed [1]. The Gate-All-Around construction provides minimal OFF-current (I_{OFF}) and a sharp subthreshold slope, while multiple wires stacking results in high drive current (I_D) with a footprint equivalent to FinFET [2]. By arranging transistors and selectors vertically, vertical NW-FETs have the potential to greatly enhance device density [3]. Stacking nanowires present a number of technical obstacles. The manufacturing of inner spacers, in particular, has been identified as a possible stumbling point for the technology. To decrease parasitic capacitances, these spacers divide the gate stack between the nanowires and the highly doped source/drain regions. In critical VLSI system manufacturing [4], NW-FETs could be made in high yield, and nanosheet and NW thickness can be scaled down to sub-10 nm [5]. So that even with the most aggressive node scaling, the electrical characteristics may be maintained. Inner spacers are now being used in NW-FETs, according to recent research [6]. Moreover, in recent times much attention is kept on junctionless (JL) FETs to continue scaling for the sub-10 nm domain. Compared to conventional inversion mode FETs the JL FETs have the following advantages: (a) It alleviates the thermal budget constraint imposed by the absence of source/drain junctions. (b) Because lateral diffused drain, pocket implantation, and shallow junction are no longer required, the manufacturing flow is simplified. (c) Because the major conducting path is through the highly doped silicon bulk, the interface between the oxide and the semiconductor channel has high immunity to surface scattering [7-9].

The need for a spacer between source and drain terminals is fundamental for sub-10 nm technology nodes to overcome SCEs. However, the introduction of spacer raises the series resistance between potentials terminals resulting in increased I_{ON}. Hence to achieve high performance of a device spacer dielectrics are introduced which boosts I_{ON} and improves subthreshold performance. Moreover, to boost DC, analog/RF metrics i.e., for mixed signal design applications the asymmetric spacer is studied. The introduction of asymmetric spacer leads to the reduction of I_{OFF} by 57% [10]. Moreover, the asymmetric spacer also reduces direct tunneling

between channel and drain and also reduces the feedback miller capacitance effect. By adding extra photolithographic process phases to current technologies asymmetrical devices are developed. Additional photolithographic techniques need more photomasks and exposure equipment, as well as more time in the manufacturing process, raising costs and lowering yield. On the other hand, Cheng et al., developed a method for producing asymmetrical structures that do not require photolithographic steps, thus saving time and money [11].

The following is an analysis of the paper's content. The paper's technique and important technological characteristics are described in Section 2. Section 3 discusses the effects of electrical performance on an asymmetric spacer. Section 4 explains how L_G scaling affects electrical properties.

2. Device structure and simulation details:

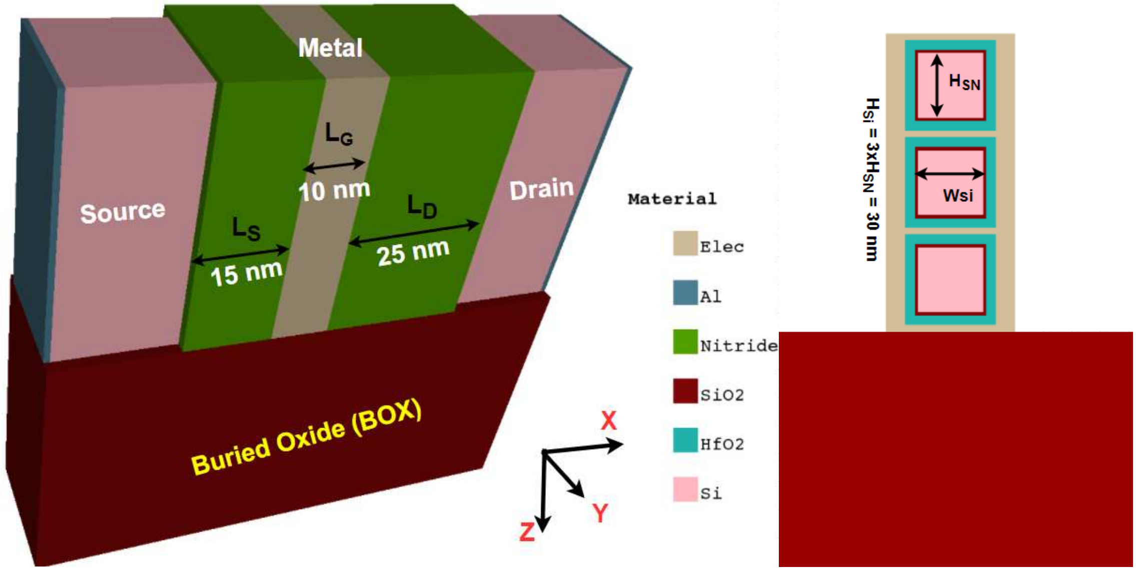


Fig. 1. 3-D n-Channel SOI JL Nanosheet (b) 2-D cross section view at Centre of fin.

The 3-D and 2-D view of JL SOI nanosheet FET is depicted in Fig.1. The nanosheet FET with gate length, width, and height of 10 nm is considered. The source and drain pad lengths are 20 nm. The SiO_2 with 0.5 nm is considered as interfacial oxide and HfO_2 is 3 nm with EOT of 0.75 nm is maintained. The doping for the whole Si bar is 1×10^{19} cm^{-3} is considered. The gate metal work function of 4.8 eV is maintained. The source side fin extension of 15 and drain side fin extension of 25 nm are maintained to form an optimized asymmetric spacer. The buried oxide is maintained with SiO_2 material. The spacer is maintained with Air, SiO_2, Si_3N_4, and HfO_2 materials.

Drift–diffusion model was used to simulate the proposed devices, and the following equations were produced by solving the drift–diffusion model, current density expressions, and Poisson equation. These are referred to as

$$\nabla . \varepsilon \nabla \Psi = -q(p - n + NA = ND^{+} + NA^{+}) \quad (1)$$

The electron and hole concentrations are denoted by n and p, respectively, Ψ is the electrostatic potential of the vacuum level, the ionized doping concentrations are given by ND^{+} and NA^{+}, and the electron charge is given by q. The temperature of the lattice should be consistent throughout the Drift–diffusion scenario.

$$\frac{1}{\mu_t} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \quad (2)$$

To accommodate for doping dependent mobility (mobility deterioration owing to surface rough scattering) and acoustic phonon in silicon lattice, the Lombardi unified mobility model was utilized.

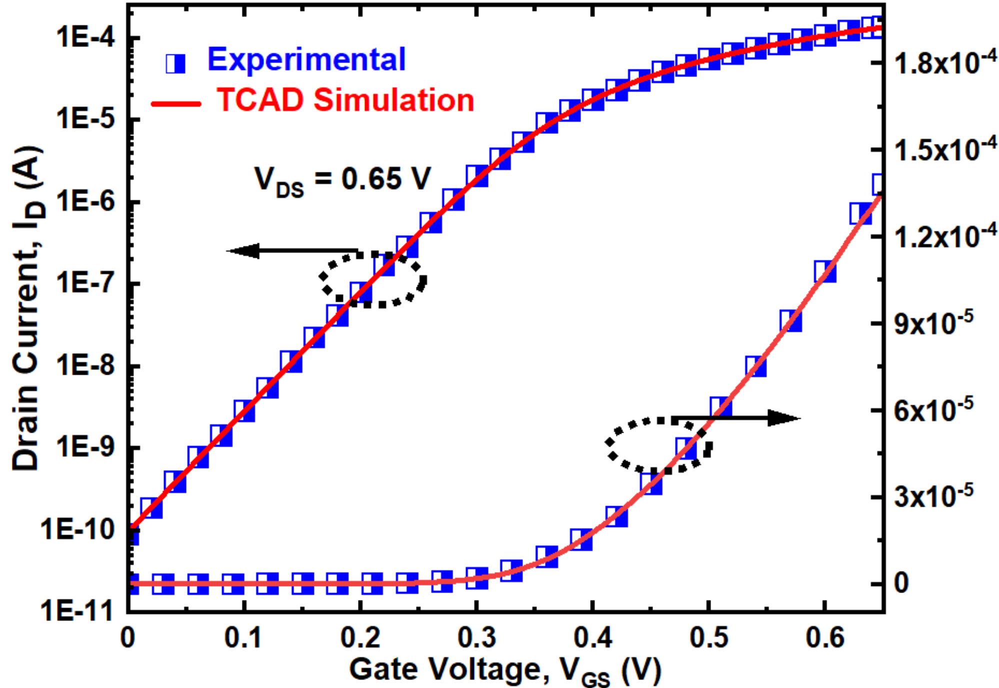
Shockley–Read–Hall (SRH), Auger, and direct recombination were all taken into account using the Carrier recombination model. As a result, final recombination U is equal to

$$U = U_{SRH} + U_{dir} + U_{Auger} \quad (3)$$

The electron and hole quantum correction equation can be written as:

$$\Lambda_n = -\frac{h^2 \gamma_n}{6qm_n} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \quad (4)$$

$$\Lambda_p = \frac{h^2 \gamma_p}{6qm_p} \frac{\nabla^2 \sqrt{p}}{\sqrt{p}} \quad (5)$$

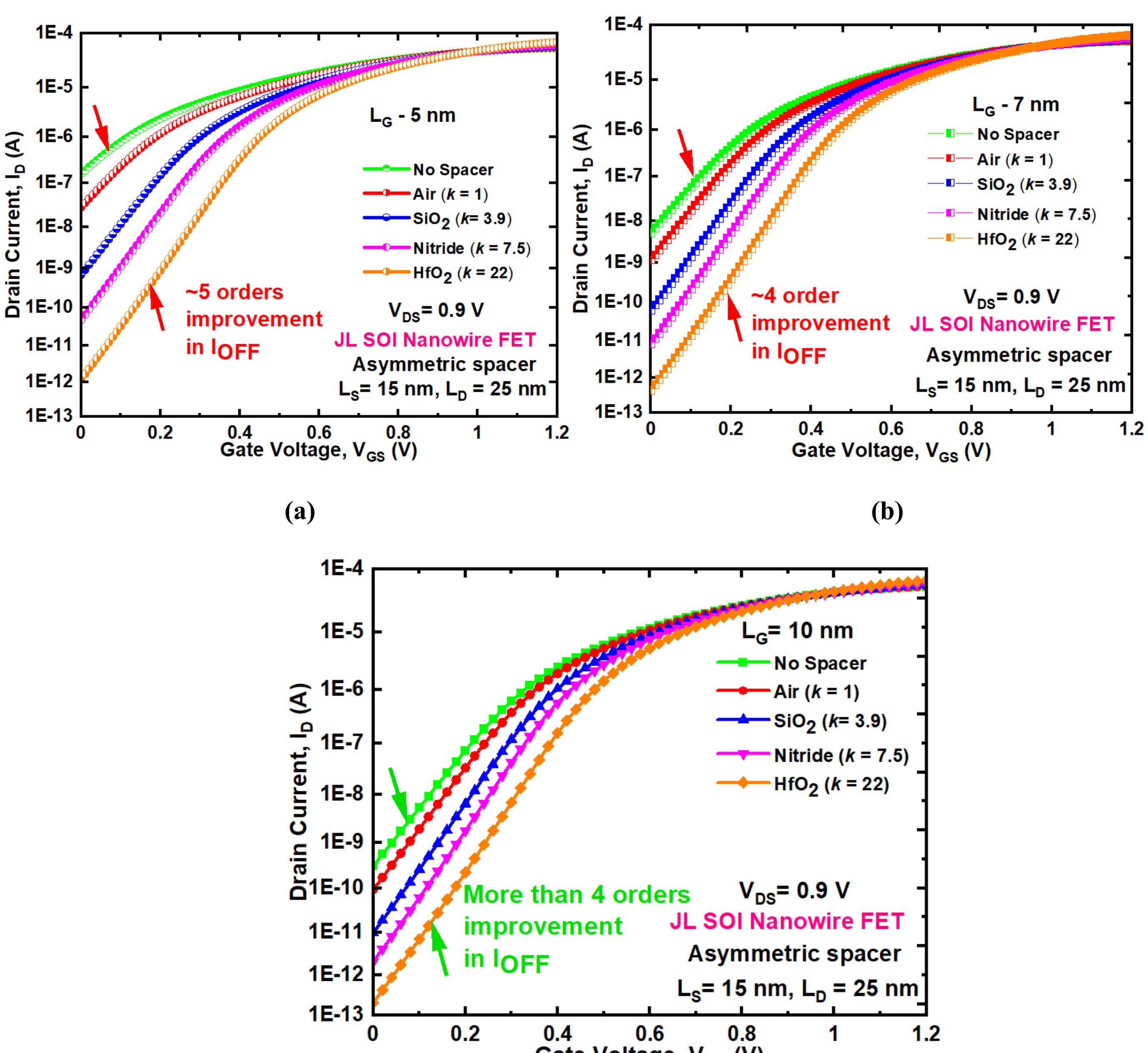


The SRH model is used to calculate carrier lifetime, and the Auger model is used to calculate current densities. Since the schenk's bandgap narrowing model for narrow bandgap effects and the caughey-Thomas model for velocity saturation calculation are used for higher doping, the schenk's bandgap narrowing model for narrow bandgap effects and the caughey-Thomas model for velocity saturation calculation are used. Quantum correction models are used in carrier confinement. The Lucent model is suggested for strong field mobility effects. The Selberherr impact ionisation model is used to calculate the electron-hole pair's producing rate. The device is well calibrated with experimental physics and simulated details are presented in Fig.2.

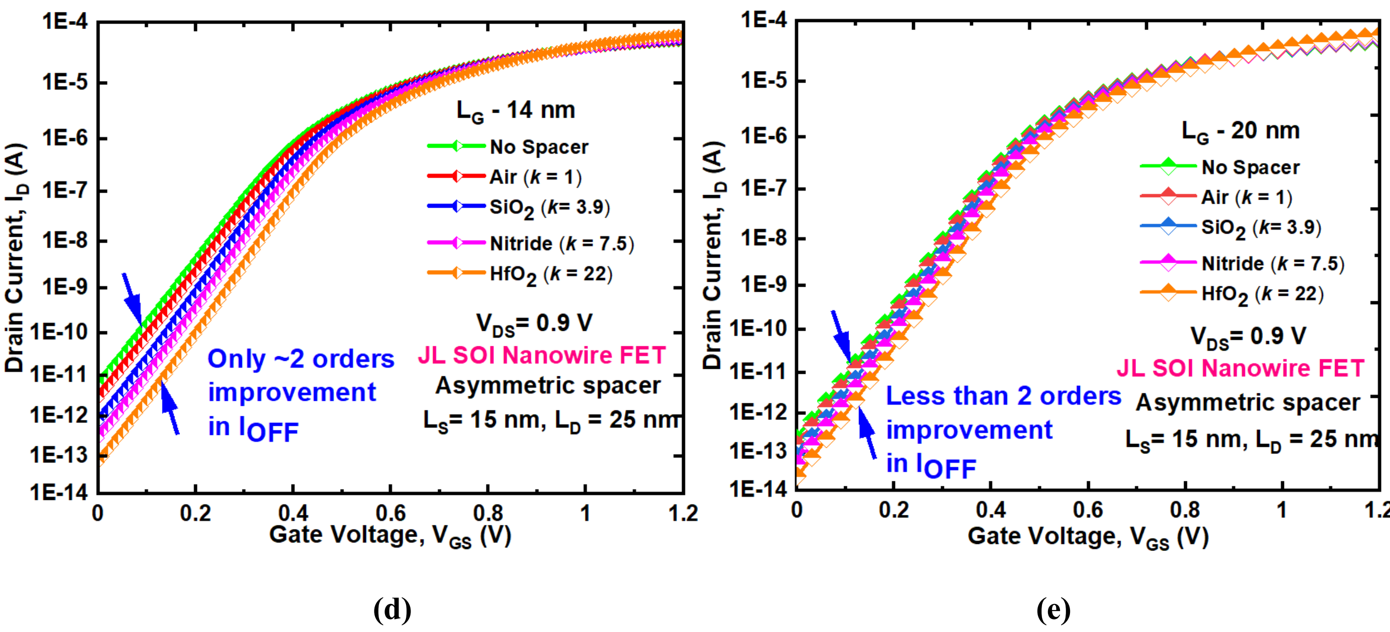
3. Result analysis

On scaling, the comparison of I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, and DIBL characteristics is examined. Scaling L_G from 20 nm to 5 nm illustrates, spacer materials influence I_D-V_{GS} features. The device obtains decreased I_{OFF} with HfO_2 spacer approaching less than pA range at L_G of 5 nm, as shown in Fig. 3(a), ensuring further scaling. The decrease in I_{OFF} as the '*k*' value increases is because of the increased electric field in the OFF state. The I_D, on the other hand, is unaffected by the flat band condition in the ON state, which results in zero electric field. The JL technology enters accumulation mode after a flat band state, and the spacer somewhat improves I_D. Because of increased series resistance and the lack of spacer fringing fields, the device suffers from a greater I_{OFF} when no spacer material is present. As a result, at ultra-scaled L_G, spacer dielectric plays a vital role in deciding performance in order to avoid leakages and mitigate SCEs. Except for Air and no spacer

dielectric, the device has an I_{OFF} of less than nA for all dielectric spacer combinations at L_G = 5 nm. Figure 3(b) shows the same pattern in I_D-V_{GS}, with a 4-order improvement in I_{OFF} as spacer dielectrics are changed. Figure 3(c) and 3(d) show a less than 2 order improvement in I_{OFF} with spacer dielectrics at 14 nm and 20 nm L_G compared to other L_G due to reduced fringing effects. Because the presence of more L_G increases gate electrostatic integrity, I_{OFF} is effectively reduced. Furthermore, because of the increased doping in the JL fin extension, the gate fringing fields are unaffected by changes in resistance at higher gate bias, producing in minor variations in I_{ON} and I_{OFF}.

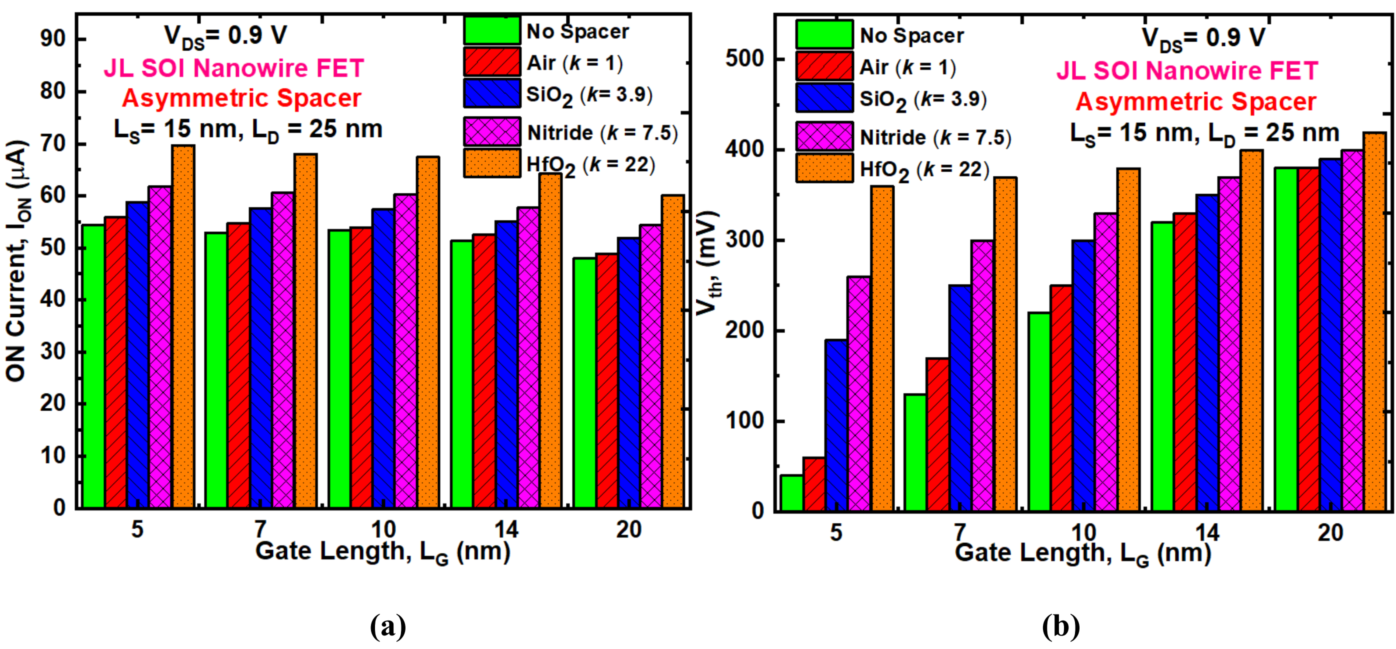


(a) **(b)**



(d) (e)

Figure. 3 Asymmetric spacer scaling at (a) L_G = 5 nm (b) L_G = 7 nm (c) L_G = 10 nm (d) L_G = 14 nm (e) L_G = 20 nm.



(a) (b)

Figure. 4 Asymmetric spacer variations on (a) ON current (I_{ON}) (b) threshold voltage (V_{th})

Figure 4(a) depicts the I_{ON} variation with various spacer dielectrics from 20 nm to 5 L_G. From results it is noticed that highest I_{ON} is obtained at 5 nm L_G with HfO_2 spacer and lowest with no spacer at 20 nm. For a device highest I_{ON} represents high performance. Figure 4(b) depicts the L_G variation for various spacer dielectrics. The device attains highest V_{th} with HfO_2 spacer at 20 nm L_G, and lowest with no spacer dielectric at 5 nm L_G. Higher V_{th} ensures better subthreshold performance.

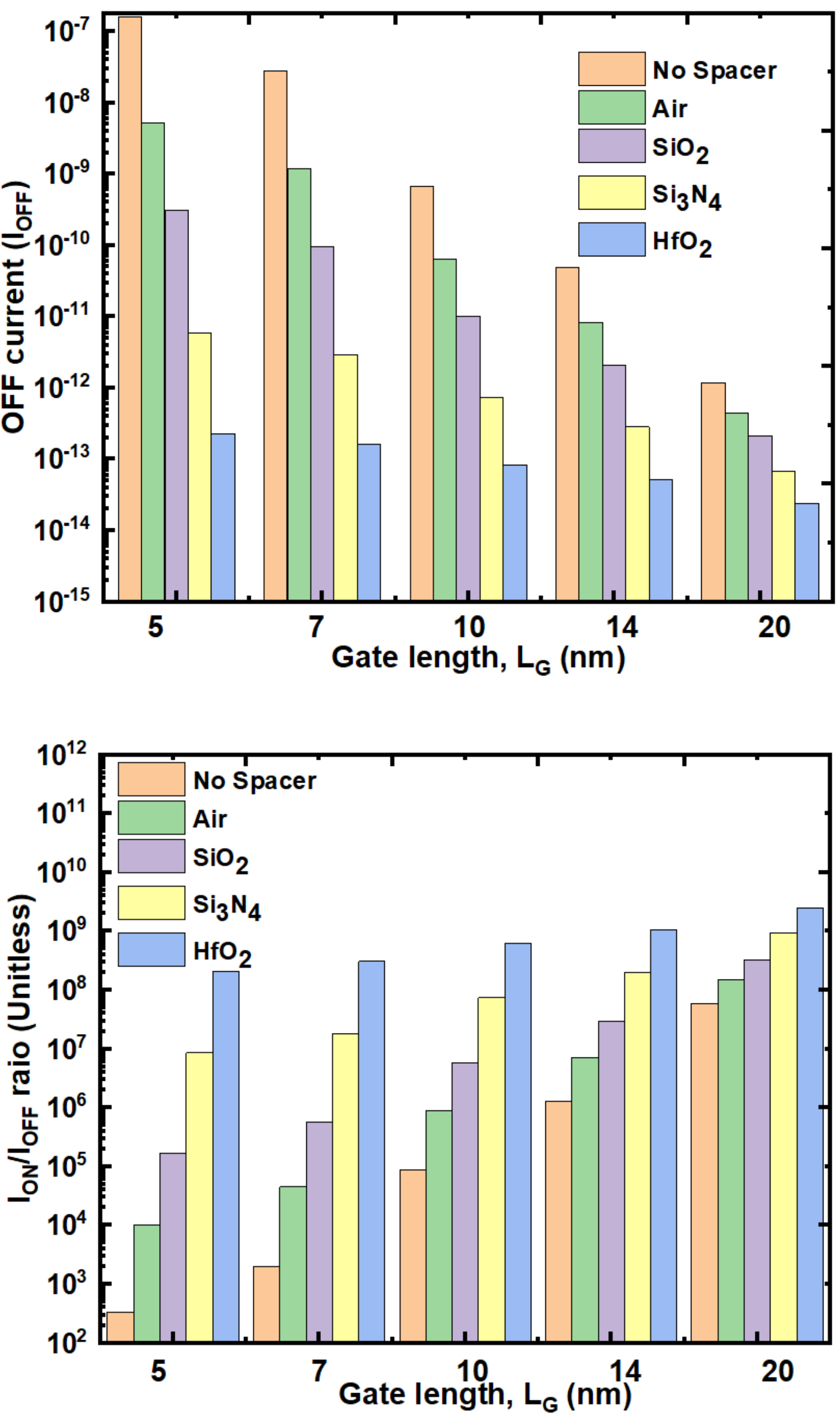


Figure. 5 Asymmetric spacer dielectric variation on (a) OFF current (I_{OFF}) (b) I_{ON}/I_{OFF} ratio.

Figure 5(a) depicts the I_{OFF} of asymmetric nanowire FET with various spacers. The device exhibits lowest I_{OFF} at L_G = 20 nm with HfO_2 spacer. Moreover, the device exhibits highest I_{OFF} with no spacer at L_G = 5 nm. However, with SiO_2, Si_3N_4, HfO_2 spacers the device exhibits I_{OFF} lesser than nA which is feasible for scaling towards low power applications. Figure 5(b) depicts the I_{ON}/I_{OFF} of asymmetric nanowire FET with various spacers. The device exhibits highest I_{ON}/I_{OFF} with HfO_2 spacer at 20 L_G. Moreover, the device shows lowest ratio at 5 nm with no spacer dielectric. The device exhibits I_{ON}/I_{OFF} ratio greater than 10^6 with Si_3N_4 and HfO_2 spacers.

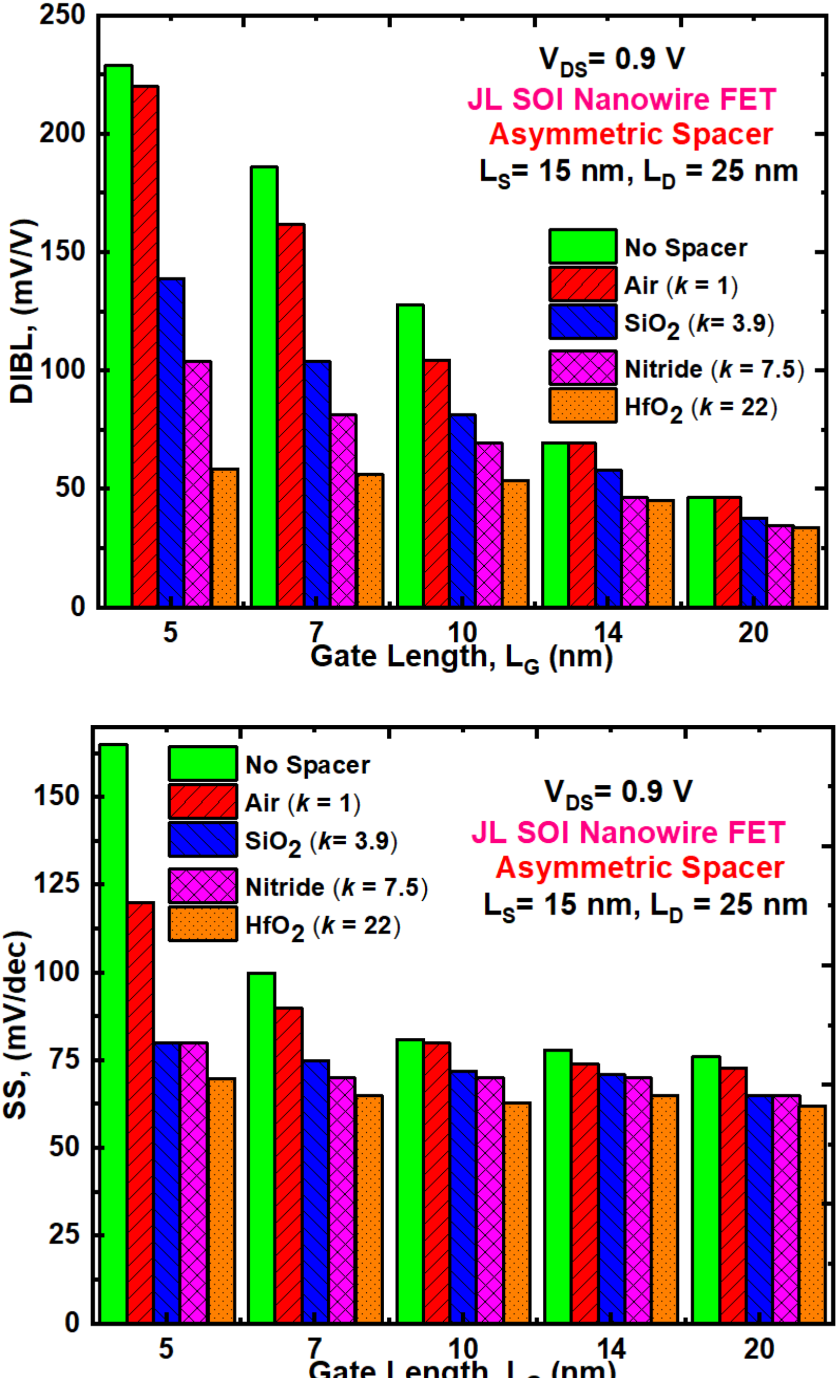


Figure. 6 Asymmetric spacer dielectric variation on (a) DIBL (b) SS.

The mathematical form of SS and DIBL is given as follows [13, 14]:

$$\text{DIBL (mV/V)} = \left|\frac{(V_{\text{th1}} - V_{\text{th2}})}{(V_{\text{DS1}} - V_{\text{DS2}})}\right| \quad (1)$$

$$\text{SS (mV/dec)} = \left[\frac{\partial \log_{10}(I_{\text{D}})}{\partial V_{\text{GS}}}\right]^{-1} \quad (2)$$

Figure 6(a) depicts the DIBL performance with scaling from 20 nm down to 5 nm with various spacers. The device exhibits highest DIBL at 5 nm with no spacer dielectric and lowest DIBL with HfO_2 spacer at 20 nm L_G. Larger value of spacer dielectric reduces DIBL impact due to series connected capacitance. The SS impact of dielectric spacer on nanowire FET from 20 nm to 5 nm L_G is depicted in Fig 6(b).

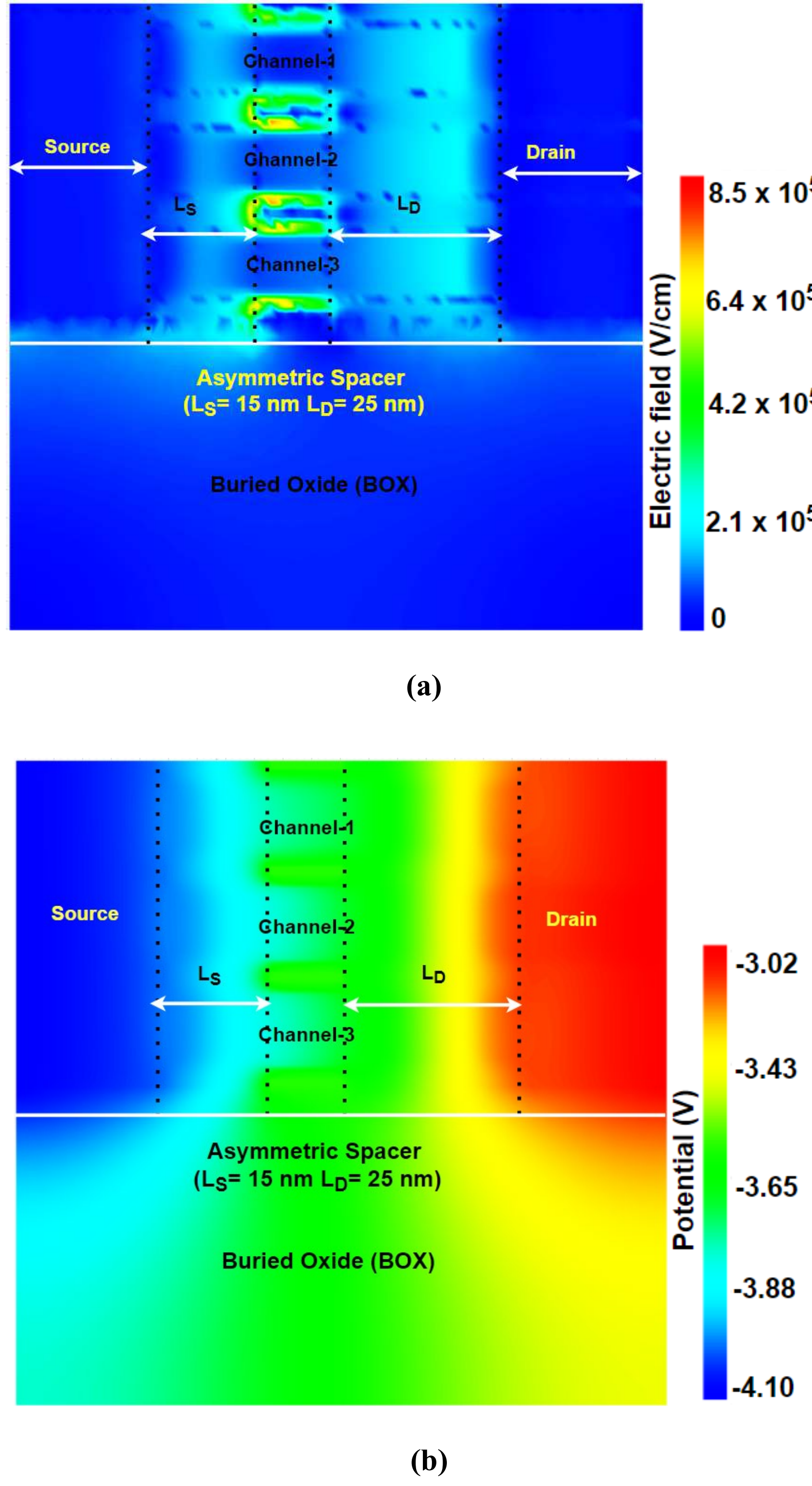


Figure. 7 Asymmetric spacer variations on (a) Electric field (b) Potential with HfO_2 spacer.

Figure 7 depicts the electric field and potential distribution of asymmetric spacer nanowire FET in ON state i.e., V_{DS} = 0.9 V and V_{GS} = 1.2 V. In Fig 7(a), Due to large spacer distance between channel and drain, there is less impact of electric field distribution on channel and thus reduces hot carriers and impact ionization. Moreover, in Fig 7(b), the large spacer distance even with high-*k* spacer reduces potential distribution over channel region.

4. Scaling effect of nanosheet FET

Figure 8(a) depicts the first derivative (g_m) of the transfer characteristics at V_{DS} of 0.9 V. The transconductance (g_m) is an important analog metric detrimental in obtaining better gain, amplification and cut-off frequencies [15, 16]. The device exhibits maximum peak of g_m with 0.119 mS at L_G = 20 nm at 1 V and g_m with 0.125 mS at L_G = 5 nm. The peaks of g_m have a window for V_{GS} values between 0.85 and 1 V ensuring potential for low power and high-speed operating capability.

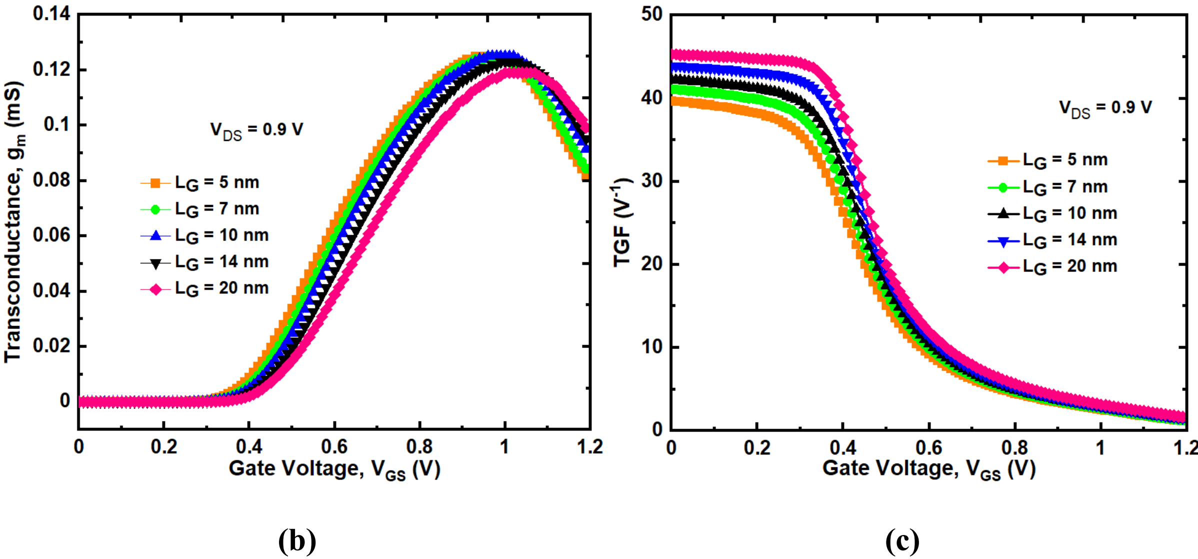


Fig. 8. Asymmetric spacer impact with gate length (L_G) variation on (a) Transconductance (g_m) (b) Transconductance generation factor (TGF).

Figure 8(b) depicts the transconductance generation factor (TGF) with L_G variation from 5 nm to 20 nm. The TGF is an important metric in determining the power required to obtain high speed with respect to gate bias. The TGF determined how current can be used to achieve a desired g_m value [17]. Due to the exponential dependence of I_D on V_{GS} in the subthreshold zone, the TGF is constant and high, but it diminishes at high V_{GS} because of mobility deterioration. From the Fig 8(b) it is observed that TGF is more at L_G = 20 nm and lower at L_G = 5 nm.

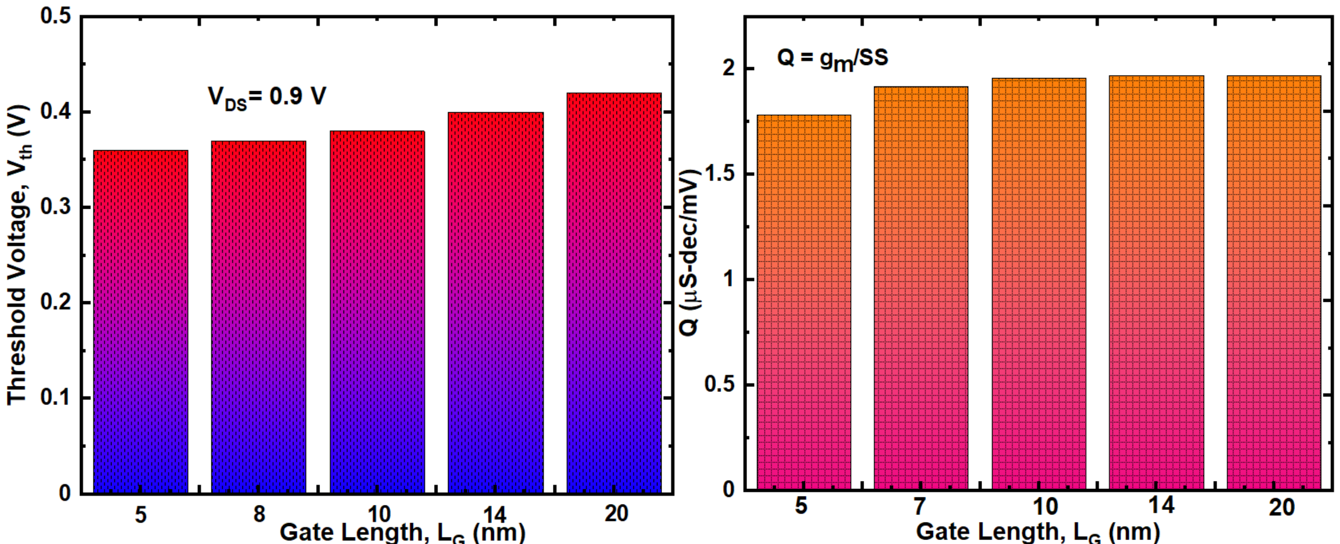
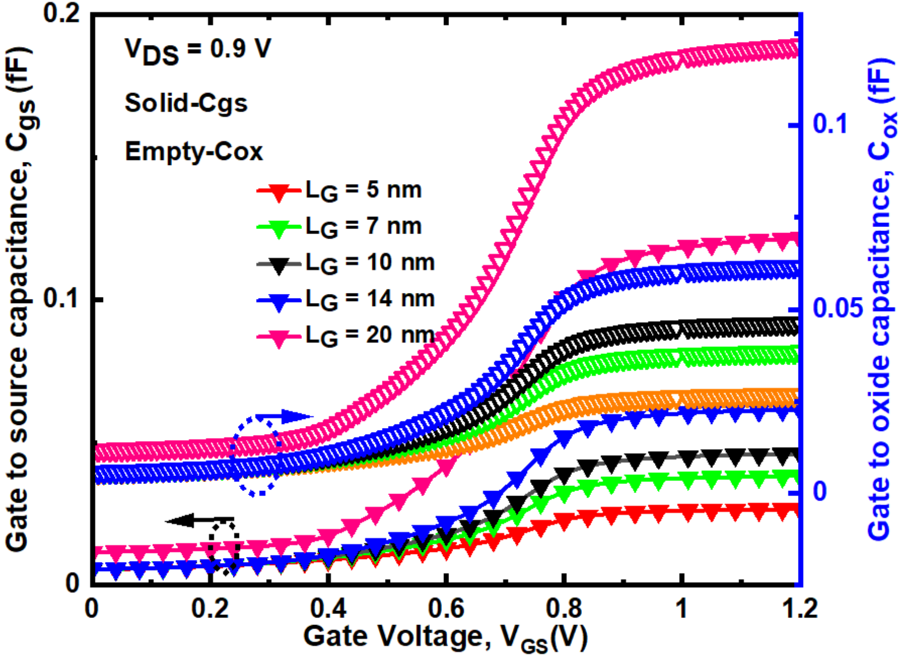


Fig. 9. Asymmetric spacer impact with gate length (L_G) variation on (a) Threshold voltage (V_{th}) (b) Q.

Figure 9(a) depicts the V_{th} variation with L_G scaling at V_{DS} = 0.9 V. Increase in L_G value enhances V_{th} due to improved gate control over channel. Narrow channel enhances V_{th} value and thus have better gate electrostatics. The device exhibits V_{th} of 0.4 V at L_G= 20 nm and 0.35 V at L_G = 5 nm. Even for lower scaled dimensions the device exhibits better V_{th} which is reasonable for driving logic device applications. Figure 9(b) depicts the variation of SS with various L_G at V_{DS} = 0.9 V. it is observed that increase in L_G SS decreases due to reduction of drain influence on channel. Moreover, at scaled L_G of 5 nm the device exhibits SS of 65 which stays below thermal limit of 80 mV/dec and thus ensure device drivability for low power applications.



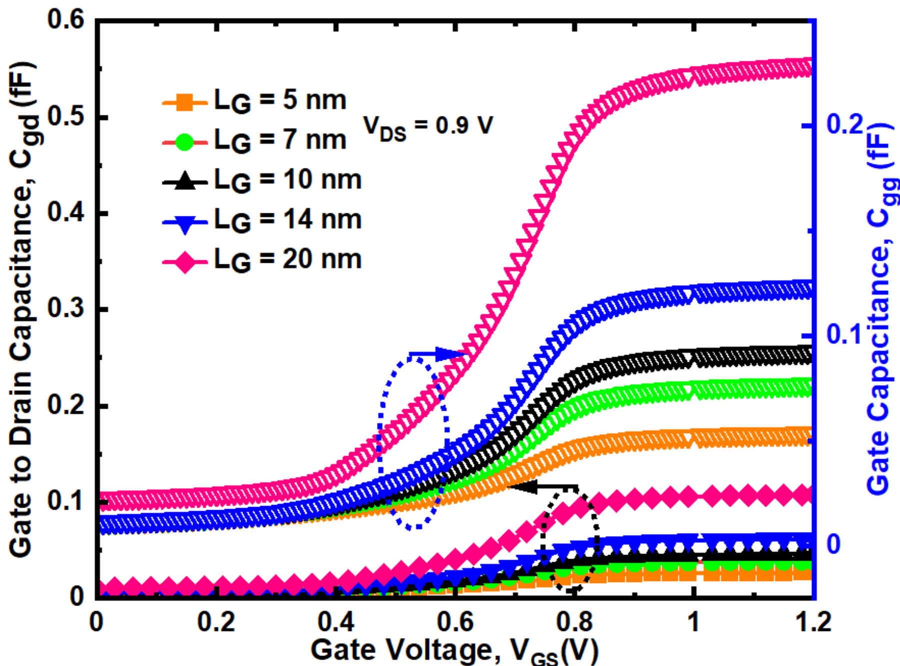


Fig. 10. Asymmetric spacer impact with gate length (L_G) variation on (a) C_{gg} and C_{gd} (b) C_{gs} and C_{ox}.

Figure 10(a) depicts the effect of C_{gd} and C_{gg} on L_G variation with respect to V_{GS} at V_{DS} = 0.7 V. Increases in L_G the total capacitance and miller capacitance increases [18]. The device exhibits C_{gd} of 0.9 fF at L_G = 20 nm and at L_G = 5 nm it shows 0.2 fF which is 4x times reduction. Reduced C_{gd} with scaling ensures reduced power consumption and better transient response.

Figure 10(b) depicts the effect of C_{gs} and C_{ox} on L_G variation with respect to V_{GS} at V_{DS} = 0.7 V. The parasitic capacitance C_{gs} and intrinsic capacitance C_{ox} decreases with L_G scaling [19]. The device exhibits C_{gs} of 0.2 fF at L_G = 5 nm and 0.1 fF which is 5x times increment. C_{ox} is the oxide capacitance which is detrimental in calculation of power consumption and dynamic power.

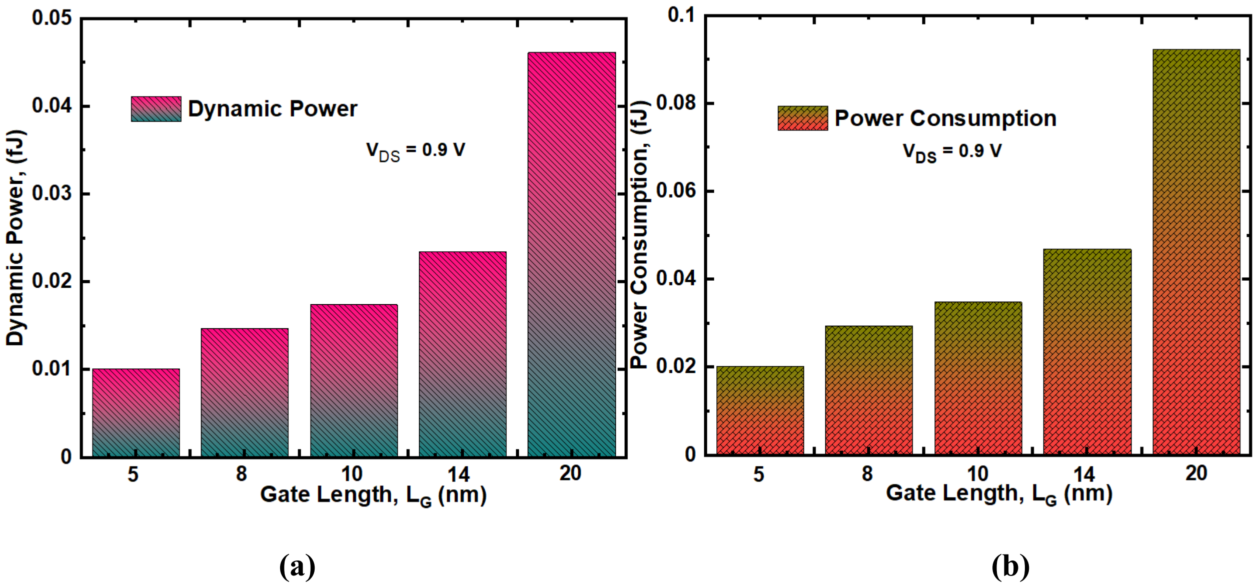


Fig. 11. Asymmetric spacer impact with gate length (L_G) variation on (a) Dynamic Power (b) Power Consumption.

The dynamic power is the power consumption due to charge and discharging cycles. The mathematical expression for dynamic power is $\left(C_{OX}{V_{DD}}^2\right)$ [20, 21] and is depicted in Fig. 11(a). The device shows DP of 0.01 at L_G = 5 nm and 0.05 at L_G = 20 nm which is 4x times more. Thus, scaling results decrease in dynamic power and ensures device feasibility for low power applications. The power consumption is the power required to drive the circuit [22]. The power consumption is mathematically expressed as $\left(\frac{1}{2}C_{OX}{V_{DD}}^2\right)$ [23-27] and is depicted in Fig. 11(b). The power consumption also reduces with L_G scaling. At L_G = 5 nm the device exhibits 0.02 fJ and at L_G = 20 nm 0.9 fJ which is 4x times higher.

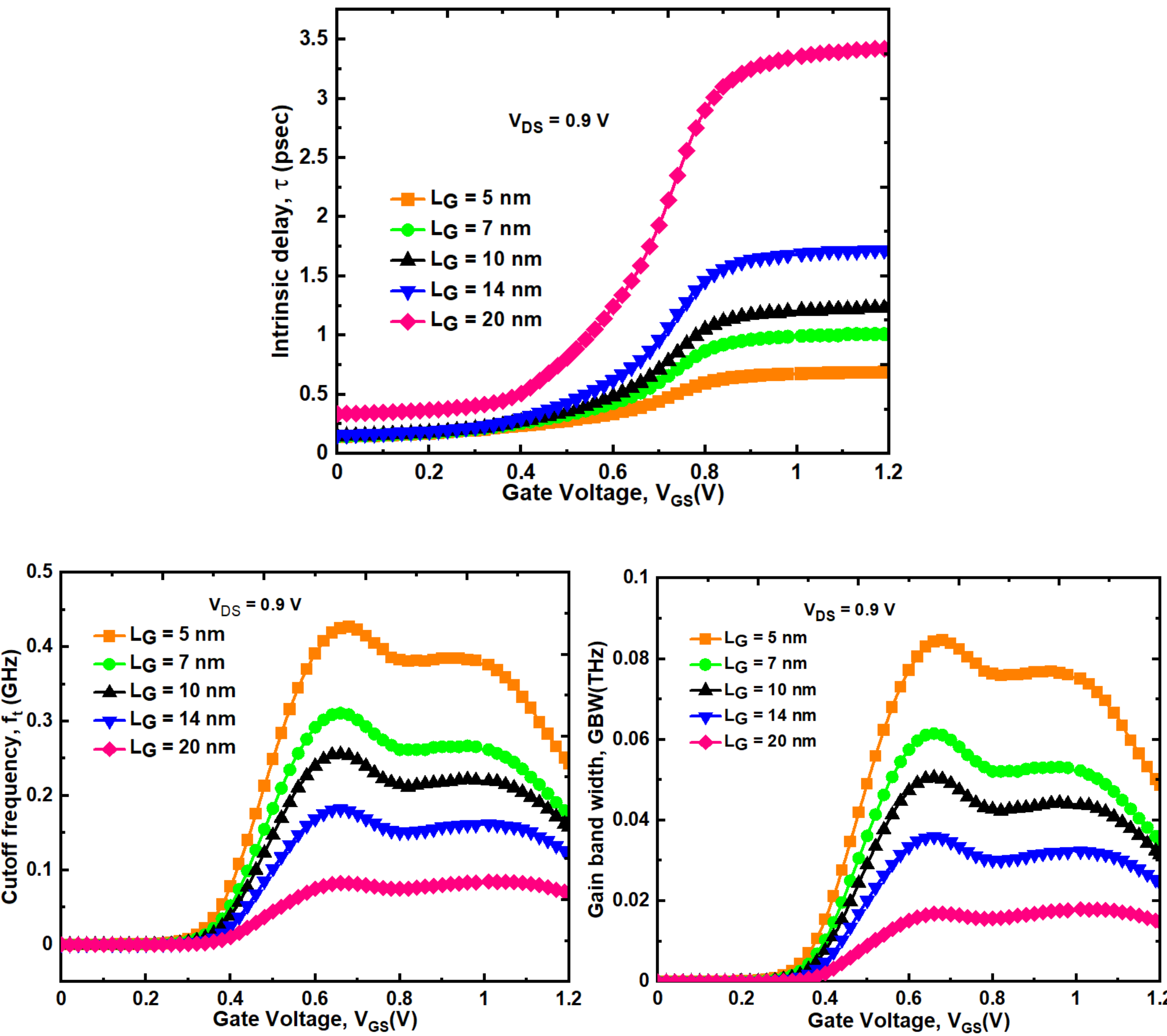


Fig. 12 Asymmetric spacer impact with gate length (L_G) variation on (a) intrinsic delay (b) Cutoff frequency

(f_T) (c) Gain bandwidth product.

The intrinsic delay (τ) value is determined at V_{DD} value of 0.9 V and is depicted in Fig 12. For L_G value of 20 nm the device exhibits τ of 3.5 ps and for 5 nm L_G the device shows 0.6 ps. decrease in L_G results reduced τ. The cut-off frequency determines the speed of the circuit [28]. The device exhibits (f_T) of 0.45 THz at L_G = 5 nm and 0.08 THz at L_G = 20 nm. The gain bandwidth product (GBW) is another important figure of merit for determining overall performance of a device [16]. The device exhibits GBW of 0.09 THz with 5 nm L_G and 0.04 THz with 20 nm L_G.

5. Conclusion

The dielectric impact on asymmetric spacer JL SOI nanowire FET has been studied towards scaling. The dielectric is predominant and fundamental at lower L_G compare to higher one. The device achieves better I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS and DIBL at L_G = 20 nm with HfO_2 spacer. However, Si_3N_4, HfO_2 spacers exhibits better overall performance and ensures possibility for scaling towards lower nodes. Moreover, the device exhibits better analog/RF metrics towards scaling. Result analysis shows the asymmetric spacer outperforms device performance for DC, analog/RF and ensures better option for scaling.

References:

1. T. Ernst et al., ‘‘Novel 3D integration process for highly scalable nanobeam stacked-channels GAA (NBG) FinFETs with HfO2/TiN gate stack,’’ IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2006, pp. 1–4. doi: 10.1109/IEDM.2006.346955.

2. S. Barraud et al., "Performance and design considerations for gate-all-around stacked-NanoWires FETs," 2017 IEEE International Electron Devices Meeting (IEDM), 2017, pp. 29.2.1-29.2.4, doi: 10.1109/IEDM.2017.8268473.

3. D. Yakimets, G. Eneman, P. Schuddinck, T. Huynh Bao, M. Garcia Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A. V.-Y. Thean, and K. De Meyer, “Vertical GAAFETs for the ultimate CMOS scaling,” IEEE Trans. Electron Devices, vol. 62, no. 5, pp. 1433-1439, May 2015, doi:

10.1109/TED.2015.2414924.

4. W. Lu and C. M. Lieber, “Semiconductor nanowires,” J. Phys. D: Appl. Phys., vol. 39, no. 21, p. R387, Oct. 2006. [Online]. Available: http://stacks.iop.org/0022-3727/39/i=21/a=R01
5. Kola, S.R., Li, Y. & Thoti, N. Random telegraph noise in gate-all-around silicon nanowire MOSFETs induced by a single charge trap or random interface traps. *J Comput Electron* **19,** 253–262 (2020). https://doi.org/10.1007/s10825-019-01438-9.
6. H. Mertens et al., ‘‘Vertically stacked gate-all-around Si nanowire transistors: Key process optimizations and ring oscillator demonstration,’’ IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2017, pp. 37.4.1–37.4.4. doi: 10.1109/IEDM.2017.8268511.
7. Bharath S. V. and Narendar. V, Design and Insights into Sub-10 nm Spacer Engineered Junctionless FinFET for Nanoscale Applications. ECS Journal of Solid State Science and Technology 10 (1) (2021) 013008.
8. V. B. Sreenivasulu, V. Narendar, Performance improvement of spacer engineered n-type soi finfet at 3-nm gate length, AEU-International Journal of Electronics and Communications 137 (2021) 153803.
9. V. Bharath Sreenivasulu, Vadthiya Narendar, Characterization and optimization of junctionless gate-all-around vertically stacked nanowire FETs for sub-5 nm technology nodes, Microelectronics Journal,2021,105214, https://doi.org/10.1016/j.mejo.2021.105214.
10. A. Goel, S. K. Gupta, K. Roy, Asymmetric drain spacer extension (adse) finfets for low-power and robust srams, IEEE Transactions on Electron Devices 58 (2) (2010) 296–308.
11. Cheng et.al., Method of forming asymmetric spacers and methods of fabricating semiconductor device using asymmetric spacers, U.S. patent 0 233 691, 2008.
12. Rumar R, Kumar A (2020) Hetro-Dielctric (HD) oxide-engineered junctionless double gate all around (DGAA) nanotube field effect transistor (FET). Silicon.
13. V. Narendar, R. Mishra, Analytical modeling and simulation of multigate finfet devices and the impact of high-k dielectrics on short channel effects (sces), Superlattices and Microstructures 85 (2015) 357–369.
14. Navaneetha A, Reddy AK, Deepthi SA, et al. Performance evaluation of noise coupling on germanium based TSV filled material for future IC integration technique. Mater Today Proc. 2021; 45:1494-1497.

15. C. K. Pandey, A. Singh, S. Chaudhury, A simulation-based analysis of effect of interface trap charges on dc and analog/HF performances of dielectric pocket SOI-Tunnel FET. Microelectronics Reliability 122 (2021) 114166, https://doi.org/10.1016/j.microrel.2021.114166.
16. C. K Pandey, D. Dash and S. Chaudhury, Improvement in analog/RF performance of SOI TFET using dielctric pocket, International Journal of Electronics. **107**, 1844-1860 (2020).
17. R. Saha, Simulation study on ferroelectric layer thickness dependence RF/Analog and linearity parameters in ferroelectric tunnel junction TFET, Microelectronics Journal, 113 (2021) 105081.
18. N. Gupta, A. Kumar, Assessment of High-k Gate Stack on Sub-10 nm SOI-FinFET for High Performance Analog and RF Applications Perspective ECS J. Solid state Sci. Technol.9 123009 2020.
19. Roy Barman, Kuheli Baishya, Srimanta 2019, An insight to the performance of vertical super-thin body (VSTB) FET in presence of interface traps and corresponding noise and RF characteristics, Applied Physics A, 125, 865, 2019.
20. Chahardah Cherik, Iman Mohammadi, Saeed2021 Germanium-source L-shaped TFET with dual in-line tunneling junction Applied Physics A 127, 525.
21. Yu E, Lee W, Jung J, Cho S. Ultrathin SiGe shell channel p-type FinFET on bulk Si for sub-10-nm technology nodes. IEEE Transac Electron Dev. 2018; 65: 1290-1297.
22. A.K. Panigrahy, Ghosh, T., Vanjari, S.R.K. and Singh, S.G., 2019. Surface density gradient engineering precedes enhanced diffusion; drives CMOS in-line process flow compatible Cu–Cu thermocompression bonding at 75° C. IEEE Transactions on Device and Materials Reliability, 19(4), pp.791-795.
23. V. B. Sreenivasulu, V. Narendar, Design and temperature assessment of junctionless nanosheet fet for nanoscale applications, Silicon (2021) 1–12. https://doi.org/10.1007/s12633-021-01145-w.
24. Kumar, B., Chaujar, R. Numerical Study of JAM-GS-GAA FinFET: A Fin Aspect Ratio Optimization for Upgraded Analog and Intermodulation Distortion Performance. *Silicon* (2021).
25. Madadi, D., Orouji, A.A. & Abbasi, A. Improvement of Nanoscale SOI MOSFET Heating Effects by Vertical Gaussian Drain-Source Doping Region. *Silicon* **13,** 645–651 (2021).
26. Sreenivasulu, V. B., Narendar, V. A Comprehensive Analysis of Junctionless Tri-gate (TG) FinFET Towards Low-power and High-frequency Applications at 5-nm Gate Length. Silicon (2021).

27. V. B. Sreenivasulu, V. Narendar, Design insights into RF/analog and linearity/distortion of spacer engineered multi-fin SOI FET for terahertz applications. Int J RF Microw Comput Aided Eng. 2021; 31(9): e22875. https://doi.org/10.1002/mmce.22875.
28. Rinku Rani Das, Santanu Maity, Atanu Chowdhury, Apurba Chakraborty,RF/Analog performance of GaAs Multi-Fin FinFET with stress effect, Microelectronics Journal, 117, 2021, 105267.

Author Contributions

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