

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2022.Doi Number

# Ladder-Type $G_m$ -C Filters with Improved Linearity

A.R. Ghasemi<sup>1</sup>, H. Aminzadeh<sup>2</sup>, Member, IEEE, and A. Ballo<sup>3</sup>, Member, IEEE

<sup>1</sup>Department of Electrical Engineering, Bushehr Branch, Islamic Azad University, Busheher, Iran; ar.ghasemi@iau.ac.ir

<sup>2</sup>Department of Electrical Engineering, Payame Noor University (PNU), 19395-4697, Tehran, Iran; aminzadeh@pnu.ac.ir

<sup>3</sup>Department of Electrical, Electronics and Computer Engineering, University of Catania, I-95125 Catania, Italy; andrea.ballo@unict.it

Corresponding authors: A. Ballo (e-mail: [andrea.ballo@unict.it](mailto:andrea.ballo@unict.it)) and H. Aminzadeh (e-mail: [aminzadeh@pnu.ac.ir](mailto:aminzadeh@pnu.ac.ir)).

**ABSTRACT** A simple yet effective approach to improve the linearity of the transconductor-capacitor ( $G_m$ -C) filters is proposed without any area or power overhead. Following a generalized nodal analysis, the transconductors of classical filter topology are rewired such that their input differential voltage lies within the linear regime. The effectiveness of the proposed method is validated through the design and simulation of a fifth-order Butterworth low-pass filter (LPF) in a standard 65-nm CMOS process. The proposed filter implementation occupies 0.0164 mm<sup>2</sup> (0.003 mm<sup>2</sup>/pole) die area and consumes 167- $\mu$ W for the cut-off frequency of 1-MHz. Operating at 1-V voltage supply, it shows an in-band total harmonic distortion (THD) of -49.14 dB for 200-mV peak-to-peak 1MHz differential voltage. An in-band 3rd-order intercept point (IIP3) of 9.36 dBm is also achieved with an in-band spurious-free-dynamic range (SFDR) greater than 53-dB, all of which reflect meaningful improvements relative to the classical architecture and despite the modest linearity performance of the internal  $G_m$  stages.

**INDEX TERMS** Analog filter, Butterworth approximation, complementary metal-oxide-semiconductor (CMOS), continuous-time,  $G_m$ -C, linearity, low-pass filter, low-power, operational transconductance amplifier (OTA), and signal flow graph (SFG).

## I. INTRODUCTION

Analog filters having a cut-off frequency from a few Hz to several GHz are one of the basic building blocks found in video signal processors, biomedical implants, read/write channels for hard-disk drives, ultra-wideband (UWB) communication transceivers and wireless Bluetooth and Zigbee networks [1]–[10]. Complementary-metal-oxide-semiconductor (CMOS) is the major technology to integrate the analog filters along with the digital sub-modules for such applications [11]–[14]. Power management is inevitably applied to different blocks of an integrated circuit (IC) for different purposes, the most important of which is to minimize battery size and to maximize the battery lifetime for mobile applications. In the case of filter design at minimum consuming power, stringent frequency response specifications are primarily required to meet the typical requirements of upcoming applications, complicating the implementation procedures in the nano-scale CMOS technologies which rely on a single supply voltage ( $V_{DD}$ ) of 1-V or below. Specifically, nano-scale transistors suffer from linearity issues and reduced intrinsic gain, and achieving sufficient dynamic range (DR) and linearity performance is quite challenging in recent technologies.

Continuous-time (CT) analog filters do not suffer from the switching noise sources such as clock leakage and clock feedthrough similar to the case of discrete-time (DT) filters

[15], [16]. No switching power is also wasting by the parasitic and load capacitors of the former [17]. Among the different choices for realizing a high-order CT filter, operational transconductance amplifier-capacitor (OTA-C or  $G_m$ -C) architecture is well-suited for the low-power and very low- to high-frequency applications [18]–[21]. It is comprised of capacitors and transconductors [22], both of which can be realized efficiently in CMOS technology.  $G_m$ -C integrators are composed of  $G_m$  stages in an open-loop formation, so their frequency response will not be compromised by the dominant poles of a frequency compensation network inserted for the stability of feedback amplifiers [23]–[27]. The bandwidth of a  $G_m$ -C filter can be tuned much more readily than their inductance-capacitor (LC) or active resistance-capacitor (RC) counterparts [28], [29], for the inductors and resistors cannot be realized efficiently in CMOS technology (with high quality factor and/or high accuracy). The bandwidth of the  $G_m$ -C filters is also higher than the active-RC filters [8], which is surely at the cost of inferior linearity performance in the absence of feedback amplifiers [30], [31]. The linearity problem of the  $G_m$ -C filters is aggravating in the recent technologies, where aggressive scaling of the geometric sizes as well as the reduction of the voltage supply is accomplished by sacrificing the most important linearity metrics. Many techniques have been proposed to improve the linearity of  $G_m$ -C filters, which mostly concentrate on the circuit-level

solutions for enhancing the transconductors' linearity. The idea of linearized transconductors with degenerated input pair and loop control is discussed in [32]. Several solutions based on transistor in the triode region [33], [34], or floating-gate [35], body-driven [36] and cross-coupled cells [37] have been also reported and combined with efficient techniques such as adaptive biasing [38]–[42], master-slave automatic tuning [43], and cancellation of the nonlinear terms [44], [45]. Most of the above methodologies, however, establish inevitable trade-offs between the power, area and noise parameters and the DR. Some solutions not only add to design complexity, but are found to be incompatible with the restrictions of nano-scale technologies. In [46], the linearity of the transconductors is relaxed by alternating the connections between the internal transconductors. Nonetheless, the idea is only applied to a kind of standard biquad filter. Alternatively, the voltage headroom at the inputs of the transconductors can be lowered to restrict the operation of input transistors in the linear region [47]. The voltage amplitude applied to the filter input should be, however, reduced accordingly, which eventually leads up to degraded signal-to-noise ratio (SNR) and DR.

Excellent linearity performance is a prerequisite to filter out with minimum distortion the out-of-band interferences of the front-end circuits in wireless transceivers and the similar applications. For this reason, we introduce in this paper a systematic design approach for improving the linearity of the ladder-type  $G_m$ – $C$  filters without setting any trade-off between area, power and DR. The proposed methodology can be as well adopted for low-voltage filter design. In what follows, we will review the operating principles of the ladder-type  $G_m$ – $C$  filters in Section II and manipulate the classical architecture for improving its linearity based on a proposed technique. In Section III, we find the equivalent single-ended topology by modifying the signal flow graph (SFG) of the classical implementation. As a proof of concept, a commonly-used fifth-order Butterworth LPF is subsequently designed and the post-layout simulation results are reported in Section IV. Some comparisons with the classical architectures from the prior research are also made in Section II. In the end, conclusions are drawn in Section V.

## II. POSSIBLE WAYS TO IMPLEMENT FULLY-DIFFERENTIAL LADDER-TYPE FILTERS

The first step towards successful filter design is to decide the frequency spectrum specifications, wherein the most important of which are the minimum stop-band attenuation and the maximum pass-band ripple at the pass-band and stop-band frequency ranges. Without losing generality, we choose

the Butterworth approximation for the poles constellation of the transfer function in this section, for a superior linear phase response with a maximally flat band can be acquired compared to Chebyshev or Elliptic approximations. High-order  $G_m$ – $C$  filters may be realized using the standard first-order, biquad or multiple-feedback  $G_m$ – $C$  modules in series, or possibly by implementing a ladder-type inductance–capacitance ( $LC$ ) topology via capacitors and  $G_m$  cells. The ladder-type arrangement is found to be less susceptible to the components' variations [48], making the final configuration less sensitive to the time-constant deviations of the integrators when the  $LC$  topology is realized by capacitors and OTAs.

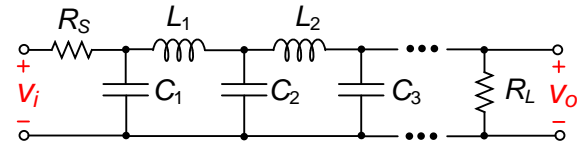


FIGURE 1. A single-ended ladder-type  $LC$  filter.

The order of the filter is decided subject to the trade-offs between power, die area, and the specifications of the frequency response. Let us start from the passive ladder-type ( $LC$ ) LPF topology depicted in Fig. 1 ( $v_i$  and  $v_o$  are the input and output voltages, respectively) and limit its order to 5 wherever required in the successive discussions to facilitate the analysis. Despite these considerations, the conclusions can be generalized to the type of all-pass (AP), band-pass (BP), high-pass (HP), and band-stop (BS) ladder-type filters of any order. The general voltage-gain transfer function of the fifth-order  $LC$  filter shown in Fig. 1 is given below

$$H(s) = \frac{v_o}{v_i} = \frac{1}{b_0 + b_1s + b_2s^2 + b_3s^3 + b_4s^4 + b_5s^5} \quad (1a)$$

where  $s$  is Laplace operator and

$$b_0 = 1 + \frac{R_S}{R_L} \quad (1b)$$

$$b_1 = \frac{L_1 + L_2}{R_L} + R_S(C_1 + C_2 + C_3) \quad (1c)$$

$$b_2 = \frac{R_S}{R_L}(L_1C_1 + L_2C_1 + L_2C_2) + (L_1C_2 + L_1C_3 + L_2C_3) \quad (1d)$$

$$b_3 = R_S(L_1C_1C_3 + L_2C_1C_3 + L_2C_2C_3) + \frac{L_1L_2C_2}{R_L} \quad (1e)$$

$$b_4 = \frac{R_S}{R_L}(L_1L_2C_1C_2) + (L_1L_2C_2C_3) \quad (1f)$$

$$b_5 = R_S L_1 L_2 C_1 C_2 C_3 \quad (1g)$$

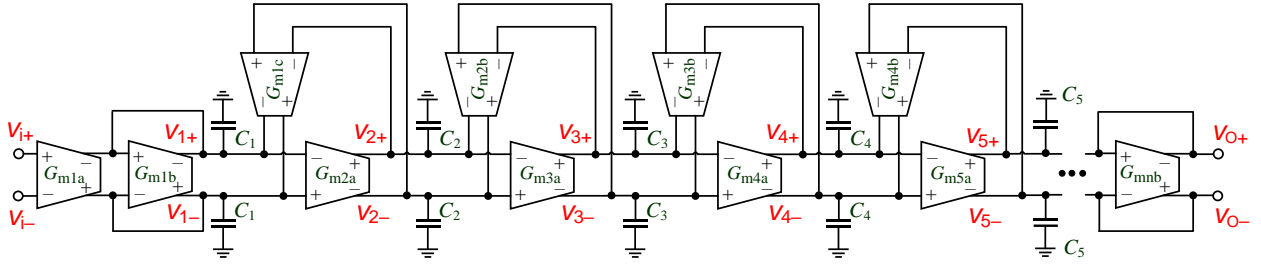


FIGURE 2. Classical ladder-type  $G_m$ -C LPF (fully-differential representation).

The normalized coefficients of a fifth-order Butterworth filter were extracted, just in the case where source internal resistance,  $R_S$ , equals the load resistance,  $R_L$ , from an numerical design manual as  $C_1 = 0.618$  F,  $L_1 = 1.618$  H,  $C_2 = 2$  F,  $L_2 = 1.618$  H,  $C_3 = 0.618$  F, and  $R_S = R_L = 1 \Omega$  (see, Table 2.9 in [49]), for the transfer function to be shaped as:

$$H(s) = \frac{0.5}{(s+1)(s^2+0.618s+1)(s^2+1.618s+1)} \quad (1h)$$

#### A. CLASSICAL IMPLEMENTATION

Fig. 2 depicts the  $G_m$ -C implementation of the ladder-type LPF in Fig. 1 [50]. The grounded load resistor  $R_L$  and the floating input resistor  $R_S$  are made by the  $G_{mnb}$  and the  $G_{m1a}$  and  $G_{m1b}$  stages, respectively, whereas each floating inductor is realized by four OTAs and a single capacitor ( $L_1$ , e.g., by  $G_{m2a}$ ,  $G_{m3a}$ ,  $G_{m1c}$ ,  $G_{m2b}$  and  $C_2$ , and  $L_2$  by  $G_{m4a}$ ,  $G_{m5a}$ ,  $G_{m3b}$ ,  $G_{m4b}$  and  $C_4$ ). The size of the normalized capacitors  $C_1$  to  $C_n$  should be scaled down subject to allowable noise level and die area. A big challenge for integrating the ladder-type  $G_m$ -C filters is to sufficiently lower the transconductance values, keeping unchanged the  $C/G_m$  time constants and the shape of the frequency spectrum. Careful considerations are accordingly required to implement a reliable small-size transconductor [51]. Three transconductors provide the current  $i_{C1}$  of  $C_1$  as is clear in Fig. 2, establishing the following relation between  $i_{C1}$  and the nodal voltages by applying the current law:

$$i_{C1} = G_{m1a}(v_{i-} - v_{i+}) + G_{m1b}(v_{1-} - v_{1+}) + G_{m1c}(v_{2+} - v_{2-}) \quad (2)$$

Similarly, the current  $i_{Cj}$  of  $C_j$  ( $j = 2$  to 5 in the case of  $n = 5$ ) can be formulated as:

$$i_{C2} = G_{m2a}(v_{1-} - v_{1+}) + G_{m2b}(v_{3+} - v_{3-}) \quad (3)$$

$$i_{C3} = G_{m3a}(v_{2-} - v_{2+}) + G_{m3b}(v_{4+} - v_{4-}) \quad (4)$$

$$i_{C4} = G_{m4a}(v_{3-} - v_{3+}) + G_{m4b}(v_{o+} - v_{o-}) \quad (5)$$

$$i_{C5} = G_{m5a}(v_{4-} - v_{4+}) + G_{m5b}(v_{o-} - v_{o+}) \quad (6)$$

As deduced from the above expressions, the linearity problem of the classical filter arises when the transconductors need to handle a large input amplitude. This corresponds to a

greater  $v_i = v_{i+} - v_{i-}$  which eventually enlarges all  $v_j = v_{j+} - v_{j-}$  ( $j = 2$  to 5 in case of  $n = 5$ ) at the input of the transconductors. Throughout the input range, they must therefore reflect a very linear behavior for the input voltage to be converted to an output current with minimum distortion.

#### B. PROPOSED IMPLEMENTATION

The linearity of the classical ladder-type filter not only depends on the voltage swing at the input of the transconductors, but also the linearity of the transconductors. Several solutions have been therefore proposed to realize a linear transconductor as described briefly in Section I. In this Section, we shall instead focus on the input voltage swing of the transconductors and improvise an alternative representation of a ladder-type  $G_m$ -C filter which defines less linearity constraints for the intermediate stages. At this purpose, we revisit and arrange the nodal equations in Section II.A to check whether it is possible to realize the filter by applying in-phase signals to the transconductors. With this idea in mind, (3), (4) and (5) can be rearranged when  $G_{m2a} = G_{m2b}$ ,  $G_{m3a} = G_{m3b}$ , and  $G_{m4a} = G_{m4b}$  as:

$$i_{C2} = G_{m2a}(v_{1-} - v_{3-}) + G_{m2b}(v_{3+} - v_{1+}) \quad (7)$$

$$i_{C3} = G_{m3a}(v_{2-} - v_{4-}) + G_{m3b}(v_{4+} - v_{2+}) \quad (8)$$

$$i_{C4} = G_{m4a}(v_{3-} - v_{o-}) + G_{m4b}(v_{o+} - v_{3+}) \quad (9)$$

Fig. 3 depicts an alternative representation of an  $n$ th-order LPF after the modifications made in (7) to (9) are applied. It maintains the total current pumped to  $C_2$ ,  $C_3$  and  $C_4$ , producing a transfer function similar to the case of the classical implementation. For in-band frequencies, however, the intermediate transconductors now analyze in-phase signals and can be realized much more simply than the standard configuration. The voltage swing at the input of the intermediate transconductors,  $G_{mja}$  and  $G_{mjb}$  ( $j = 2$  to 4 in case of  $n = 5$ ), is consequently lowered, enhancing the linearity of the filter without a compromised area or power. Fig. 4 compares the system-level simulation of the voltage amplitude at the input of  $G_{m2a}$ ,  $G_{m3a}$ ,  $G_{m4a}$  and  $G_{m2b}$ ,  $G_{m3b}$ ,  $G_{m4b}$ , by applying the values in Table I to implement a 1 MHz fifth-order Butterworth filter.

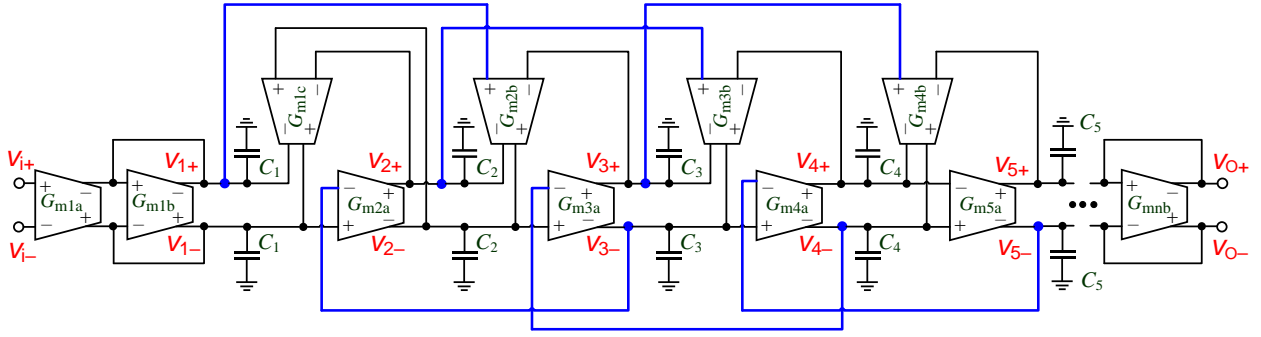


FIGURE 3. Proposed ladder-type  $G_m$ -C LPF (fully-differential representation).

The size of the transconductors is set to  $32 \mu\text{A/V}$ , enabling to scale down the capacitor sizes according to tolerable noise level in minimum silicon area. Fig. 4(a) compares the frequency response of the voltages at the input of the transconductors of the classical and modified topologies across the pass-band region. Unlike the classical case where the signal phases are unconditionally opposite and yield maximum amplitude, the phase differences are now a function of frequency. For low-frequency input signals, the nearly zero phase differences are accompanied by maximum efficiency. The input signal phases gradually deviate at higher frequencies (still less than  $180^\circ$ ), yielding less linearity improvement as compared with the classical structure. Fig. 4(b) compares the time responses at the input of the intermediate transconductors for a signal at the edge of the pass-band. Still, the systematic simulation results predict that the proposed configuration lead up to superior linearity performance regardless of the fabrication process, operating region and the scheme of the transconductors.

TABLE I  
VALUES OF THE ELEMENTS IN THE FIFTH-ORDER FILTERS

Denormalized fifth-order Butterworth coefficients		Classical and proposed filter parameters	
Name	Value	Name	Value
$C_1$	100 fF	$C_1$	100 fF
$L_1$	254 $\mu\text{H}$	$C_2$	260 fF
$C_2$	320 fF	$C_3$	320 fF
$L_2$	254 $\mu\text{H}$	$C_4$	260 fF
$C_3$	100 fF	$C_5$	100 fF
$R_L$	31 k $\Omega$	$G_m$	32 $\mu\text{A/V}$

From the above results, it is clear that maximum improvement in terms of linearity can be reached when the voltages applied to the input of the transconductors are in-phase signals with similar magnitudes. Equivalently, the efficiency of the proposed technique will diminish in cases when the transconductors should handle in-phase signals but with unequal amplitudes or with similar magnitude but alternative phases, like in certain BP or AP implementations. Depending on the amplitude and the phase of the signal

applied to the transconductances, the proposed fully-differential implementation has one drawback over the standard topology. Despite the resulted maximum swing, the differential nature of the signals at the input of the transconductances causes minimum susceptibility to the common-mode disturbances such as power supply ripples. As such, we expect that the higher linearity comes at the cost of less power supply rejection (*PSR*) at different frequencies.

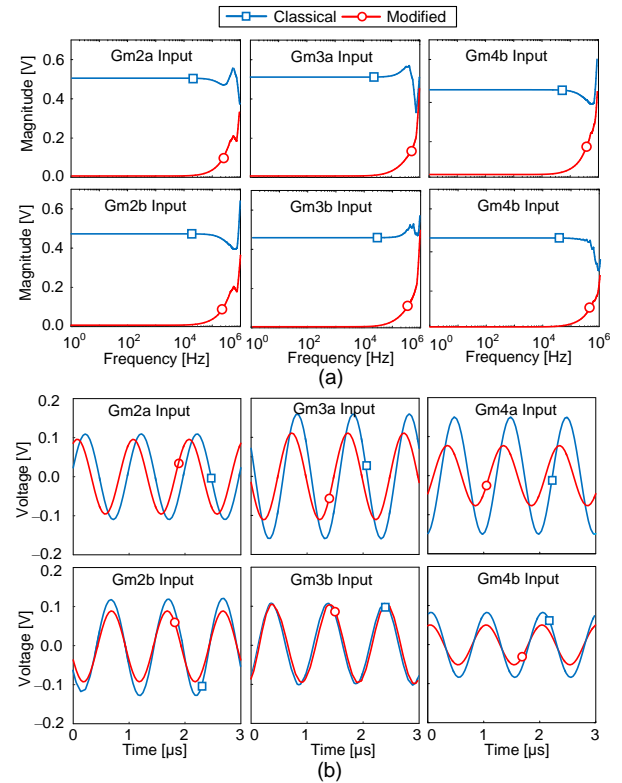
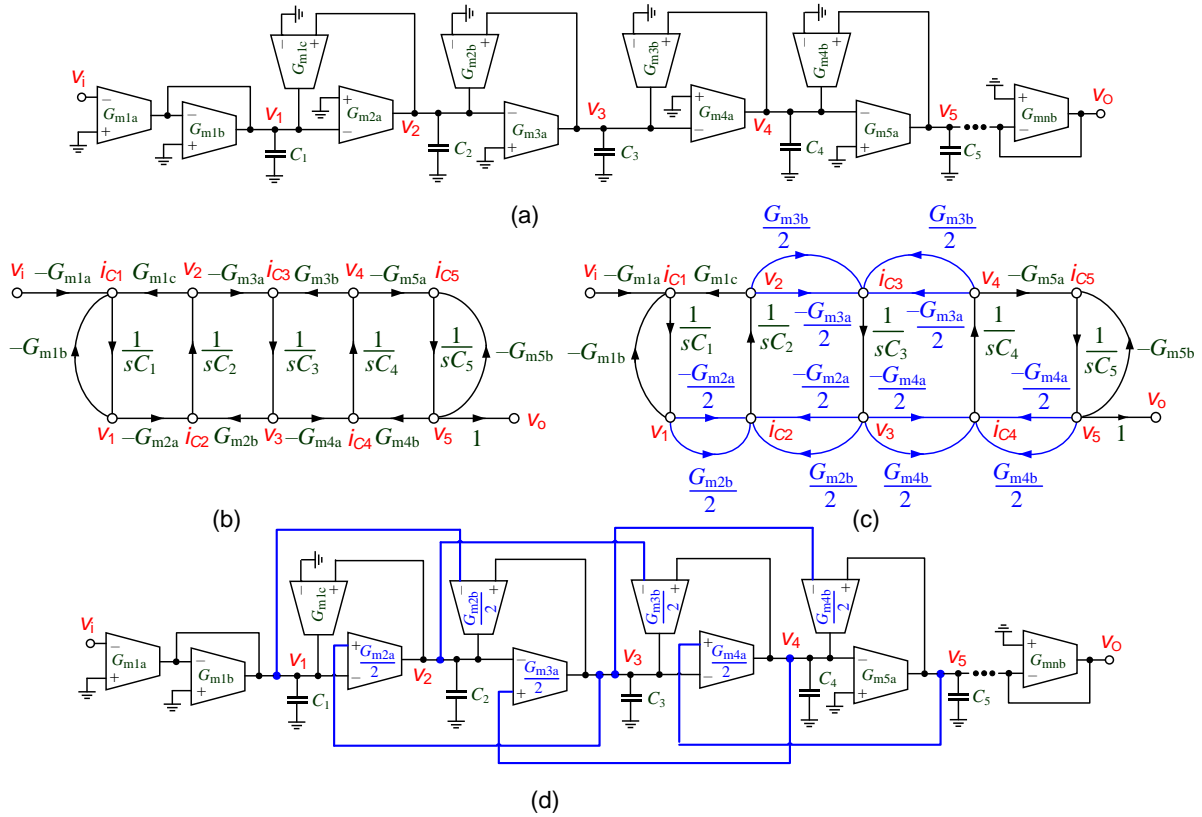


FIGURE 4. Comparison between the classical and proposed cases in terms of the input voltage applied to the input of the transconductors; (a) Systematic simulation of the frequency response; (b) Transient response at the edge of the pass-band.



**FIGURE 5.** Using SFG to transform the standard topology to the proposed topology; (a) Classical ladder-type  $G_m$ -C LPF (single-ended representation); (b) SFG diagram of classical filter; (c) Equivalent SFG diagram of the proposed filter; (d) Proposed ladder-type  $G_m$ -C LPF (single-ended).

### III. PROPOSED FILTER IN SINGLE-ENDED IMPLEMENTATION

It would be instructive to alternatively derive the single-ended implementation of the proposed filter based on the feasible manipulations on the SFG of the classical filter. Fig. 5(a) exhibits the single-ended representation of the classical topology shown in Fig. 2. The equivalent SFG graph of a fifth-order filter is sketched in Fig. 5(b), where  $v_i$  and  $v_o$  are the input and output nodes and the voltage  $v_j$  and the current nodes  $i_{c_j}$  ( $j = 1$  to  $5$  for  $n = 5$ ) denote the voltage and current of the capacitors, respectively. The SFG is formed by  $G_m$  and  $1/sC$  among the different current and voltage nodes. Let us take  $G_{m2a} = G_{m2b}$ ,  $G_{m3a} = G_{m3b}$ , and  $G_{m4a} = G_{m4b}$  the same as earlier, and divide the forward and backward ways which contain these weights into parallel twigs. One of the twigs having half weighting from each set can then be replaced by a corresponding twig from the adjacent branch such that the overall summations at each intermediate node is kept intact consistent with Fig. 5(c). The weighting of the left and right branches entering to the node  $i_{c2}$ , e.g., are now converted to  $G_{m2b}/2 - G_{m2a}/2$  rather than the original  $G_{m2b}$  and  $-G_{m2a}$ . The implementation of the modified SFG in Fig. 5(c) is then accomplished by the modified scheme depicted in Fig. 5(d), which represents the single-ended topology of the proposed filter in Fig. 3. In addition to the described advantages for linearity, the intermediate  $G_m$  values of the single-ended

configuration are halved as compared to the classical implementation, giving the possibility to implement the corresponding stages with less power consumption and silicon area. What's more, the classical single-ended implementation compares the signals at the input of the transconductances with ground. Therefore, from the perspective of  $PSR$ , it does not have the previously-described advantage over the proposed solution.

For both single-ended and fully-differential topologies, the design procedures of the proposed filter is similar to the commonly-used design procedures (choosing the filter specifications, implementing the standard  $LC$  ladder, denormalizing the coefficients similar to Table I). The transconductors would be, however, rewired in the final stage to reach superior linearity metrics as compared to standard implementation.

### IV. SIMULATION RESULTS

#### A. OTA

Irrespective of the filter implementation, it is possible to improve the linearity by resorting only to the circuit-level solutions that enhance the transconductors' linearity. These techniques can be used for the proposed filter, especially in the case of the first and the last OTAs whose input signals are opposite. In this work, a single-stage  $G_m$  stage with a relatively low DC gain was, however, chosen for the OTAs to better quantify the capabilities of the proposed solution. Fig. 6



presents the scheme of the single-stage folded-cascode amplifier [31] together with the transistor dimensions for  $G_m = 32 \mu A/V$  in 65-nm CMOS. It is made up of  $M_{1a}-M_{1b}$  to  $M_{5a}-M_{5b}$  biased by the tail transistor  $M_0$ . The input pair  $M_{1a}-M_{1b}$  transforms the input  $V_{i+} - V_{i-}$  into the differential  $I_{o+} - I_{o-}$ . This arrangement benefits from wider input common-mode than a telescopic-cascode configuration at the cost of elevated power consumption. Assuming a linear  $I-V$  characteristic, the output current expressed in terms of the input voltage is:

$$I_{o+} - I_{o-} = G_m (V_{i+} - V_{i-}) \quad (10)$$

The  $G_m$  value can be adjusted over a broad range by the tail current  $I_{SS}$ , while the input pair  $M_{1a}-M_{1b}$  may be arbitrarily biased in the weak, moderate, and strong inversion regions [52]. The biasing voltages from  $V_{B1}$  to  $V_{B4}$  are established by the biasing network (not shown here), whereas the common-mode feedback (CMFB) voltage is generated and applied to the gates of  $M_{5a}-M_{5b}$  (not included for simplicity). The cascoded devices  $M_{3a}-M_{3b}$  and  $M_{4a}-M_{4b}$  boost the gain of the amplifier. Important performance metrics such as noise, mismatch, and load drive capability were considered for sizing the core devices according to the gate ratios in Table II.

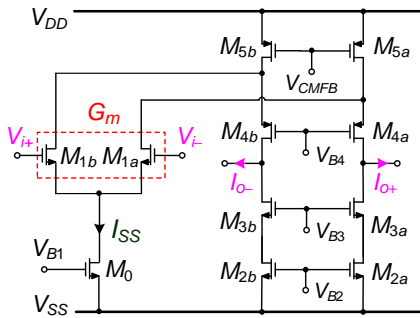


FIGURE 6. Schematic of the OTA.

TABLE II  
DEVICE DIMENSIONS IN 65-NM CMOS

Transistor	W/L	Transistor	W/L
$M_{1a}, M_{1b}$	$0.2\mu m / 0.18\mu m$	$M_{4a}, M_{4b}$	$8.0\mu m / 0.50\mu m$
$M_{2a}, M_{2b}$	$0.8\mu m / 0.18\mu m$	$M_{5a}, M_{5b}$	$8.0\mu m / 0.50\mu m$
$M_{3a}, M_{3b}$	$0.8\mu m / 0.18\mu m$	$M_0$	$0.2\mu m / 0.18\mu m$

Fig. 7 indicates the OTA frequency response under 1-V power supply. It achieves 35.4 dB DC gain and 1.4 MHz unity-gain frequency (UGF) with a phase margin (PM) greater than  $85^\circ$  for a 0.5-pF external load. Fig. 8 depicts the current-voltage ( $I-V$ ) characteristic of the OTA subject to a 0.5 V<sub>P-P</sub> input voltage swing. The input devices are biased in the strong inversion and  $I_{SS}$  is set to 5.4  $\mu A$ . The input voltage swing of the transconductors should be limited to around 500 mV peak-to-peak for maximum non-linearity of 10%.

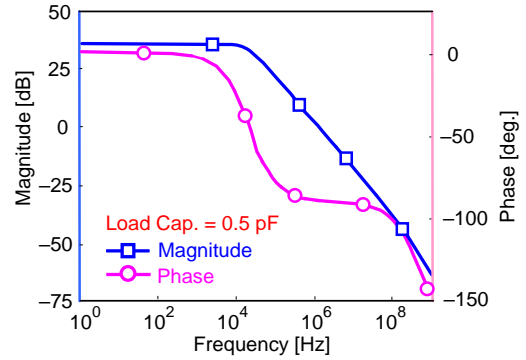


FIGURE 7. Frequency and phase responses of the OTA in 65-nm CMOS.

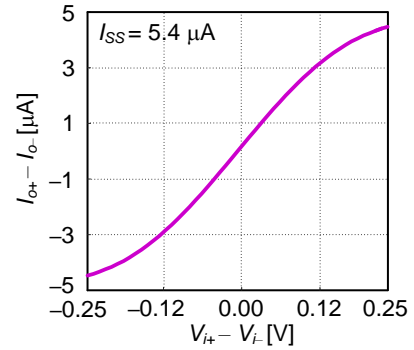


FIGURE 8.  $I-V$  characteristic of the OTA simulated in 65-nm CMOS.

## B. PROPOSED FULLY-DIFFERENTIAL FILTER

The efficiency of the proposed technique for enhancing the linearity of ladder-type filters is validated through simulation of the fifth-order fully-differential filter shown in Fig. 3. Fig. 9 exhibits the layout in 65-nm CMOS process, occupying an active area of  $164 \mu m \times 100 \mu m$  for the component values and the gate ratios specified in Table I and Table II. The filter core consumes a nominal power of 167.2  $\mu W$  under a 1-V voltage supply. The following results mostly pertain to the post-layout simulations.

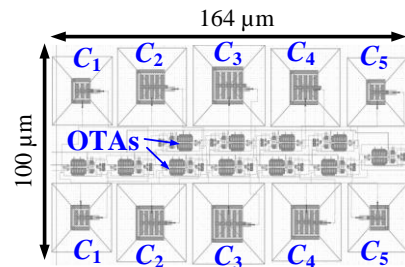
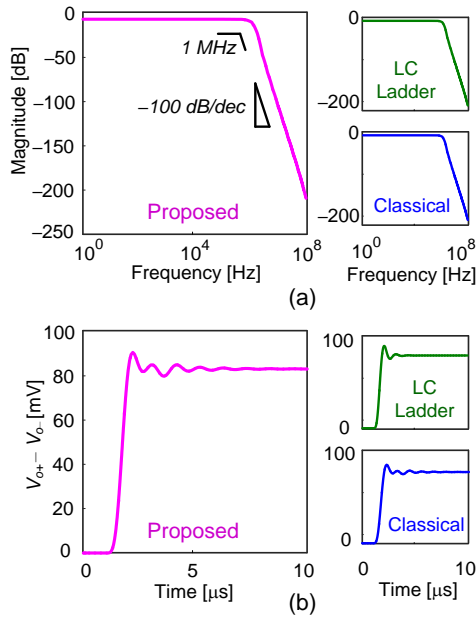
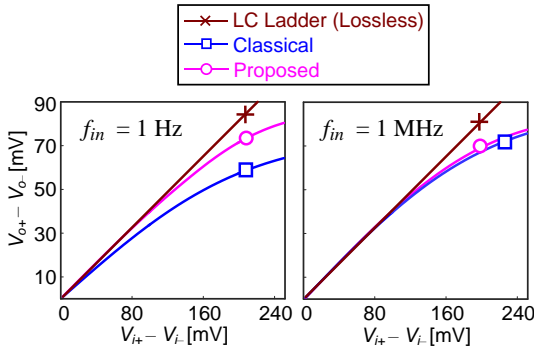


FIGURE 9. Core layout of the proposed filter.



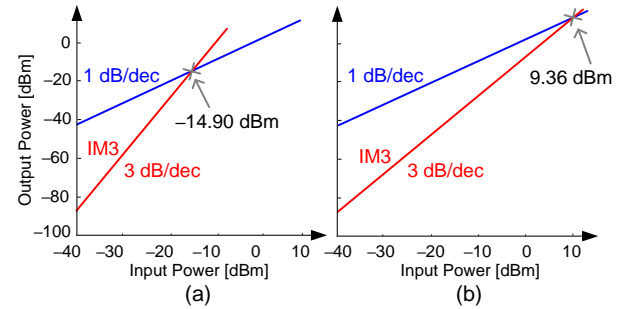
**FIGURE 10.** Comparison between different implementations. (a) Frequency response; (b) Step response.



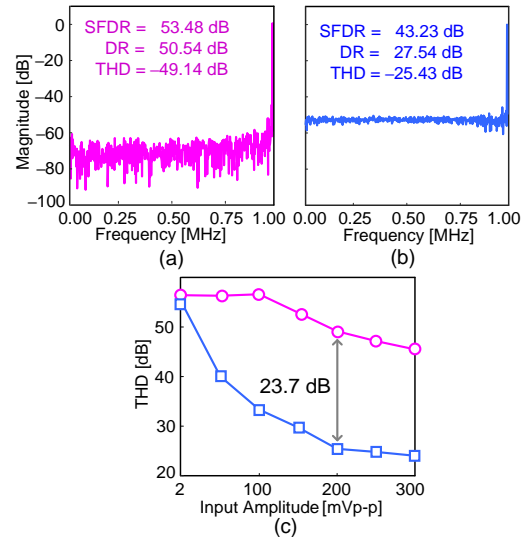
**FIGURE 11.** Comparison between the transfer curves at different frequencies.

Fig. 10(a) illustrates the frequency spectrum of the filter and compares it with the *LC* ladder and the classical implementations. It exhibits a  $-3$  dB cut-off frequency of approximately 1 MHz coherent with other implementations. An in-band 1.2 dB gain ripple was perceived owing to the finite OTA gains. Fig. 10(b) compares the small-signal step response of different implementations subject to 80 mV differential output step. The simulated similar frequency and time responses confirm that the proposed implementation is, indeed, an alternative implementation of the ladder-type *LC* filter. Fig. 11 presents the input-output characteristic of the proposed topology for different frequencies within the pass-band (1 Hz and 1 MHz). The transfer curves of the standard implementation and *LC* ladder are also sketched for comparison. For the low-frequency waveforms with higher amplitude, the graph of the proposed filter is found to be closer to the fixed-slope line belonging to the *LC* ladder. As described in Section II, this is due to the in-phase signals appear at the input of the transconductances at lower

frequencies. The phase differences smoothly increase at higher frequencies, reducing the linearity metrics at the edge of the 1 MHz pass-band in line with the qualitative results. As the other index of linearity, the output power spectrums of the classical and proposed designs have been plotted in Fig. 12, when a 1 MHz sinusoidal waveform is applied to the input with 200-mV peak-to-peak amplitude. The third intermodulation frequency (IM3) is included to measure IIP3. The 9.36 dBm IIP3 of the proposed arrangement outperforms  $-14.9$  dBm of the classical filter.



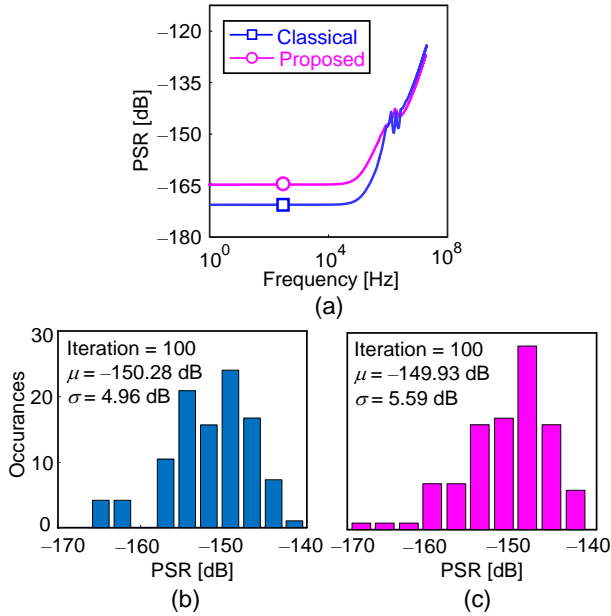
**FIGURE 12.** Simulation of the power spectrum; (a) Classical design; (b) Proposed design.



**FIGURE 13.** Simulation result of the frequency spectrum; (a) Proposed design; (b) Classical design; (c) THD vs. Input amplitude in both cases.

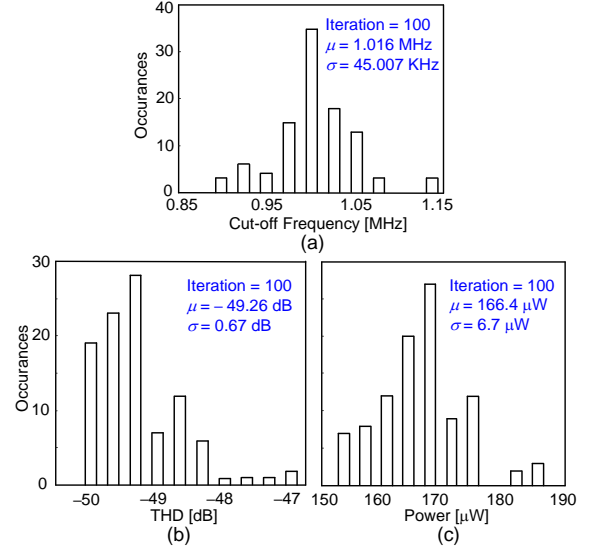
Fig. 13 compares the power spectral density of the classical and modified topologies for the same 200 mV<sub>P-P</sub> input amplitude. THD, SFDR and DR are measured as  $-49.14$  dB, 53.48 dB and 50.54 dB in Fig. 13(a), respectively, revealing significant improvement over the equivalent values  $-25.43$  dB, 43.23 dB and 27.54 dB for classical filter (Fig. 13(b)). Fig. 13(c) compares the THD vs. input amplitude of both configurations. The THD improvement is about 23.7 dB at the edge of the pass-band for 200 mV<sub>P-P</sub> input amplitude.

In return to the improvement of linearity metrics, what we miss is less immunity to the common-mode disturbances as evidenced by the post-layout simulations summarized in Fig. 14(a). The low-frequency *PSR* of the classical architecture is almost 10-dB better than the proposed implementation, reducing to lower values at higher frequencies until the two plots match each other. The similar *PSR* performance at the edge of the pass-band was also concluded by performing 100-times Monte-Carlo simulations on the layout extracted filter. The *PSR* histogram of the conventional topology at 1 MHz is depicted in Fig. 14(b), exhibiting a mean value ( $\mu$ ) of  $-150.28$  dB with a standard deviation ( $\sigma$ ) of 4.96 dB. These values are comparable to  $\mu = -149.93$  dB and  $\sigma = 5.59$  dB of the proposed filter as shown in Fig. 14(c).



**FIGURE 14.** Comparison between the *PSR* performances. (a) Classical vs. proposed topology; (b) *PSR* histogram of the classical topology at 1 MHz; (c) *PSR* histogram of the proposed topology at 1 MHz.

Monte-Carlo simulations of the cut-off frequency, THD, and consuming power are also performed to investigate the effect of the transistor mismatches on the operation of the proposed filter, and the distributions are summarized in Fig. 15 for 100 iterations. The mean value of the cut-off frequency is 1.016 MHz with a  $\sigma$  of 45 KHz, yielding a variation coefficient of  $\sigma/\mu = 4.42\%$ .



**FIGURE 15.** Monte-Carlo simulation results for (a) Cut-off frequency, (b) THD, and (c) Power consumption.

Table III reports the variations of these parameters referred to the process corners, where the symbols TT: typical; SS: Slow *n*MOS, Slow *p*MOS; FF: Fast *n*MOS, Fast *p*MOS; FS: Fast *n*MOS, Slow *p*MOS; SF: Slow *n*MOS, Fast *p*MOS are used to label different corners. A worst-case THD of  $-48.29$  dB was measured in the SS corner, which corresponds to the minimum power consumption of  $158$   $\mu$ W.

Performance	TT	FF	FS	SF	SS
Cut-off Frequency [MHz]	1.001	1.032	0.983	0.981	0.986
THD@0.2V <sub>pp</sub> ,1MHz [dB]	-49.14	-50.30	-50.21	-51.43	-48.29
Power consumption [ $\mu$ W]	167	176	171	161	158

The figure-of-Merit (FoM)

$$FoM_1 = \frac{B \times (\text{Bandwidth [MHz]})^2 \times \text{Technology Feature } [\mu\text{m}]}{\text{Power per Pole [mW]}} \quad (11)$$

was used to classify the operation of the new configuration among the prior art, when taking into account the bandwidth, power per pole and feature size of the technology [53].  $B$  is the amplification factor and is equal to 1.5 in case of amplification, and 1.0 if none. The following FoMs were additionally defined to include the effect of linearity on  $FoM_1$ .

$$FoM_2 = FoM_1 \times SFDR \quad (12)$$

$$FoM_3 = FoM_1 \times DR \quad (13)$$

TABLE IV  
TABLE IV OVERALL PERFORMANCE METRICS AND COMPARISON



	2022 <sup>a</sup> [10]	2020 [19]	2020 [54]	2019[2]	2018 [7]
Topology	LPF $G_m$ -C	LPF $G_m$ -C	LPF $G_m$ -C	LPF $G_m$ -C	LPF $G_m$ -C
Technology [nm]	180	180	180	180	65
$V_{DD}$ [V]	0.5	1.0	0.5	1.0	1.2
Power consumption [mW]	$0.05 \times 10^{-3}$	$0.208 \times 10^{-3}$	$0.00369 \times 10^{-3}$	$0.041 \times 10^{-3}$	5.10
Filter order	5	4	4	5	14
Bandwidth [MHz]	$0.25 \times 10^{-3}$	$0.1 \times 10^{-3}$	$0.2 \times 10^{-3}$	$0.25 \times 10^{-3}$	2.0
Index of Linearity	DR = 57.6dB @ 60mV <sub>pp</sub>	DR = 49.3dB @ 58mV <sub>pp</sub>	DR = 48.5dB @ 160mV <sub>pp</sub>	DR = 61.2dB @ 100mV <sub>pp</sub>	IIP3 = 9.0dBm
IRN [ $\mu$ V] @ Freq. Range	301 @ 1Hz-250Hz	70.77 @ 1-300 Hz	91.9 @ 1 Hz-400Hz	134 @ 0.1-250 Hz	N/A
Power [mW] / Pole	$0.01 \times 10^{-3}$	$5 \times 10^{-5}$	$0.92 \times 10^{-6}$	$0.0082 \times 10^{-3}$	0.36
Active Area [mm <sup>2</sup> ]	0.0073	0.46	0.074	0.24	0.35
FoM1	$1.125 \times 10^{-3}$	$3.4 \times 10^{-5}$	$7.8 \times 10^{-3}$	$1.37 \times 10^{-3}$	0.71
FoM2	N/A	N/A	N/A	N/A	N/A
FoM3	647.37	2.89	552.2	1806	N/A

	2017 [6]	2016 <sup>a</sup> [5]	This Work <sup>a</sup>	
			Conventional	Proposed
Topology	BPF $G_m$ -C	LPF Active-RC	LPF $G_m$ -C	LPF $G_m$ -C
Technology [nm]	180	180	65	65
$V_{DD}$ [V]	1.8	1.8	1.0	1.0
Power consumption [mW]	0.50	10.27	0.167	0.167
Filter order	4	4	5	5
Bandwidth [MHz]	0.6	2.55	1.0	1.0
Index of Linearity	SFDR = 65.6dB @ 120mV <sub>pp</sub>	IIP3 = -2.6dBm	THD = -25.4dB @ 200mV <sub>pp</sub> IIP3 = -14.9dBm	THD = -49.1dB @ 200mV <sub>pp</sub> IIP3 = 9.4dBm
IRN [ $\mu$ V] @ Freq. Range	0.126	0.058	193.4 @ 1 Hz - 1 MHz	193.4 @ 1 Hz -1 MHz
Power [mW] / Pole	0.125	2.56	0.0334	0.0334
Active Area [mm <sup>2</sup> ]	0.14	0.23	0.0164	0.0164
FoM1	0.5184	0.43	1.94	1.94
FoM2	$1.88 \times 10^6$	86192.3	40813.3	432316.42
FoM3	N/A	N/A	1101	219685.6

<sup>a</sup>Post-layout simulation results

A summary of the performance metrics of the proposed design is presented in Table III and compared with some publications. The proposed fifth-order filter occupies 0.0164 mm<sup>2</sup> (0.003-mm<sup>2</sup>/pole) active area and consumes 167  $\mu$ W (0.0334-mW/pole), both of which are among the minimum cases in the topologies compared. It thus obtained the highest  $FoMs$  when taking into account the bandwidth, power per pole, feature size of the technology and the metrics of linearity. The smallest active area is also attributed to two factors: 1. A simple architecture was chosen for the OTAs since the proposed arrangement allows achieving comparable linearity metrics using a simpler OTA topology; 2. Size of the integrated capacitors is minimized at the cost of 193  $\mu$ V input-referred noise (IRN) in the pass-band, which was still acceptable for the application of concern in this paper. The IRN vs. frequency is sketched in Fig. 13, indicating that flicker noise is dominant in the low-frequency range up to 73.8 kHz corner frequency.

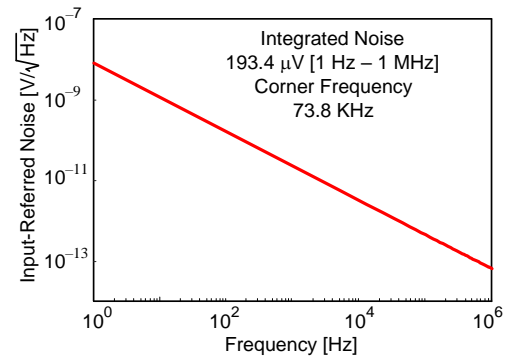


FIGURE 16. Input referred noise of the proposed design.

## V. CONCLUSION

A modified design approach was introduced to improve the linearity of the intermediate transconductors in ladder-type  $G_m$ -C filters. It resulted in smaller input voltage swing at the input of the transconductors, which eventually lead up to superior linearity performance without any compromise on area and power. The design of a fifth-order  $G_m$ -C low-pass filter was accomplished using the proposed solution. Post-layout simulation results were carried out in a standard 65-

nm CMOS process, demonstrating superior performance metrics as compared to the previous art. Endorsed by analytical and simulated results, the proposed technique relies on a systematic design approach which reconfigures the connections between the transconductors such that superior linearity metrics are resulted. It does not depend on the topology of the OTAs.

## REFERENCES

- [1] S.-Y. Lee, C.-P. Wang, C.-Y. Sun, P.-H. Cheng, and Y.-S. Chu, 'Low-Power Fifth-Order Butterworth OTA-C Low-Pass Filter with an Impedance Scaler for Portable ECG Applications', *IEICE Trans. Electron.*, vol. E101-C, no. 12, pp. 942–952, Dec. 2018.
- [2] S.-Y. Lee, C.-P. Wang, and Y.-S. Chu, 'Low-Voltage OTA-C Filter With an Area- and Power-Efficient OTA for Biosignal Sensor Applications', *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 1, pp. 56–67, Feb. 2019, doi: 10.1109/TBCAS.2018.2882521.
- [3] H. Wu, X. Liu, J. Yang, and M. Sawan, 'A Power-Efficient Source-Follower Based Tunable Pseudo-RC Low-Pass Filter for Wearable Biomedical Applications', in *2022 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct. 2022, pp. 178–182. doi: 10.1109/BioCAS54905.2022.9948655.
- [4] R. Arya, G. Souliotis, S. Vlassis, and C. Psychalinos, 'A 0.5 V 3 rd-order Tunable gm-C Filter', *Radio Eng.*, vol. 22, no. 1, pp. 174–178, 2013.
- [5] M. S. Oliveira, P. C. de Aguirre, L. C. Severo, A. G. Girardi, and A. A. Susin, 'A digitally tunable 4th-order Gm-C low-pass filter for multi-standards receivers', in *2016 29th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Aug. 2016, pp. 1–6. doi: 10.1109/SBCCI.2016.7724064.
- [6] A. Rasekh and M. Sharif Bakhtiar, 'Design of Low-Power Low-Area Tunable Active RC Filters', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 1, pp. 6–10, Jan. 2018, doi: 10.1109/TCSII.2017.2658635.
- [7] M. Zhou and K. Wang, '0.18 mW/pole inverter-based Gm-C bandpass filter with automatic frequency tuning', *Electron. Lett.*, vol. 54, no. 15, pp. 943–945, 2018, doi: 10.1049/el.2018.1128.
- [8] A. Ballo, A. D. Grasso, S. Pennisi, and C. Venezia, 'High-Frequency Low-Current Second-Order Bandpass Active Filter Topology and Its Design in 28-nm FD-SOI CMOS', *J. Low Power Electron. Appl.*, vol. 10, no. 3, Art. no. 3, Sep. 2020, doi: 10.3390/jlpea10030027.
- [9] P. Prommee, N. Wongprommoon, M. Kumngern, and W. Jaikla, 'Low-Voltage Low-Pass and Band-Pass Elliptic Filters Based on Log-Domain Approach Suitable for Biosensors', *Sensors*, vol. 19, no. 24, Art. no. 24, Jan. 2019, doi: 10.3390/s19245581.
- [10] F. Khateb, P. Prommee, and T. Kulej, 'MIOTA-Based Filters for Noise and Motion Artifact Reductions in Biosignal Acquisition', *IEEE Access*, vol. 10, pp. 14325–14338, 2022, doi: 10.1109/ACCESS.2022.3147665.
- [11] T. Kunto, P. Prommee, and M. T. Abuelma'atti, 'Electronically Tunable Current-mode High-order Ladder Low-pass Filters Based on CMOS Technology', *Radioengineering*, vol. 24, no. 4, pp. 974–987, Sep. 2015, doi: 10.13164/re.2015.0974.
- [12] P. PROMMEE, A. TIAMSUPHAT, and M. ABUELMAATTI, 'Electronically tunable MOS-only current-mode high-order band-pass filters', *Turk. J. Electr. Eng. Comput. Sci.*, vol. 25, no. 2, pp. 1116–1136, Jan. 2017, doi: 10.3906/elk-1508-250.
- [13] M. NiaboliGuilani and G. Ardeshtir, 'A mathematical method to realize complex poles in a high-order passive switched-capacitor filter', *Int. J. Circuit Theory Appl.*, vol. 47, no. 11, pp. 1762–1774, 2019, doi: 10.1002/cta.2689.
- [14] P. Prommee and E. Saising, 'CMOS-based high-order LP and BP filters using biquad functions', *IET Circuits Devices Syst.*, vol. 12, no. 4, pp. 326–334, 2018, doi: 10.1049/iet-cds.2017.0493.
- [15] P. Prommee, P. Thongdit, and K. Angkeaw, 'Log-domain high-order low-pass and band-pass filters', *AEU - Int. J. Electron. Commun.*, vol. 79, pp. 234–242, Sep. 2017, doi: 10.1016/j.aeue.2017.06.014.
- [16] C.-Y. Sun and S.-Y. Lee, 'A Fifth-Order Butterworth OTA-C LPF With Multiple-Output Differential-Input OTA for ECG Applications', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 4, pp. 421–425, Apr. 2018, doi: 10.1109/TCSII.2017.2695366.
- [17] J. R. Machha Krishna Reddy and T. Laxminidhi, '1.8 V, 25.9 nW, 91.86 dB dynamic range second-order lowpass filter tunable in the range 4–100 Hz', *IET Circuits Devices Syst.*, vol. 13, no. 7, pp. 1086–1092, 2019, doi: 10.1049/iet-cds.2019.0031.
- [18] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, 'Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors', *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2009–2018, Sep. 2006, doi: 10.1109/JSSC.2006.880606.
- [19] V. S. Rajan, K. H. Kishore, R. Sanjay, S. Kumaravel, and B. Venkataramani, 'A novel programmable attenuator based low Gm-OTA for biomedical applications', *Microelectron. J.*, vol. 97, p. 104721, Mar. 2020, doi: 10.1016/j.mejo.2020.104721.
- [20] X. Wang, C. C. Boon, K. Yang, and L. Kong, 'A 20–80 MHz Continuously Tunable Gm-C Low-Pass Filter for Ultra-Low Power WBAN Receiver Front-End', *IEEE Access*, vol. 9, pp. 154136–154142, 2021, doi: 10.1109/ACCESS.2021.3128154.
- [21] P. Prommee, K. Karawanich, F. Khateb, and T. Kulej, 'Voltage-Mode Elliptic Band-Pass Filter Based on Multiple-Input Transconductor', *IEEE Access*, vol. 9, pp. 32582–32590, 2021, doi: 10.1109/ACCESS.2021.3060939.
- [22] H. Aminzadeh, 'Nano-scale area-efficient Gm-C filters using MOS capacitors', *Int. J. Electron. Lett.*, vol. 7, no. 3, pp. 311–320, Jul. 2019, doi: 10.1080/21681724.2018.1494319.
- [23] H. Aminzadeh, A. Ballo, and A. D. Grasso, 'Frequency Compensation of Three-Stage OTAs to Achieve Very Wide Capacitive Load Range', *IEEE Access*, vol. 10, pp. 70675–70687, 2022, doi: 10.1109/ACCESS.2022.3187169.
- [24] H. Aminzadeh, A. D. Grasso, and G. Palumbo, 'A Methodology to Derive a Symbolic Transfer Function for Multistage Amplifiers', *IEEE Access*, vol. 10, pp. 14062–14075, 2022, doi: 10.1109/ACCESS.2022.3147879.
- [25] H. Aminzadeh and A. Dashti, 'Hybrid cascode compensation with current amplifiers for nano-scale three-stage amplifiers driving heavy capacitive loads', *Analog Integr. Circuits Signal Process.*, vol. 83, no. 3, pp. 331–341, Jun. 2015, doi: 10.1007/s10470-015-0522-2.
- [26] H. Aminzadeh, M. Danaie, and R. Lotfi, 'Design of Two-Stage Miller-Compensated Amplifiers Based on an Optimized Settling Model', in *20th International Conference on VLSI Design held jointly with 6th International Conference on Embedded Systems (VLSID'07)*, Jan. 2007, pp. 171–176. doi: 10.1109/VLSID.2007.65.
- [27] H. Aminzadeh and M. M. Valinezhad, '0.7-V supply, 21-nW All-MOS voltage reference using a MOS-Only current-driven reference core in digital CMOS', *Microelectron. J.*, vol. 102, p. 104841, Aug. 2020, doi: 10.1016/j.mejo.2020.104841.
- [28] M. Mojarad and M. Kamarei, 'Bandwidth extension, linearity enhancement, and cost reduction techniques for continuous-time channel-select filters', *Int. J. Circuit Theory Appl.*, vol. 45, no. 11, pp. 1600–1620, 2017, doi: 10.1002/cta.2301.
- [29] R. Póvoa et al., 'Sub-μW Tow-Thomas based biquad filter with improved gain for biomedical applications', *Microelectron. J.*, vol. 95, p. 104675, Jan. 2020, doi: 10.1016/j.mejo.2019.104675.
- [30] S. Kousai, M. Hamada, R. Ito, and T. Itakura, 'A 19.7 MHz, Fifth-Order Active-RC Chebyshev LPF for Draft IEEE802.11n With Automatic Quality-Factor Tuning Scheme', *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2326–2337, Nov. 2007, doi: 10.1109/JSSC.2007.906189.
- [31] H. Aminzadeh, R. Lotfi, and K. Mafinezhad, 'Design of low-power single-stage operational amplifiers based on an optimized settling model', *Analog Integr. Circuits Signal Process.*, vol. 58, no. 2, pp. 153–160, Feb. 2009, doi: 10.1007/s10470-008-9226-1.
- [32] G. Bollati, S. Marchese, R. Castello, and M. Demicheli, 'An eighth-order CMOS lowpass filter with 30–120 Mhz tuning range and programmable boost', in *Proceedings of the 26th European Solid-State Circuits Conference*, Sep. 2000, pp. 133–136.
- [33] S. Hori, T. Maeda, N. Matsuno, and H. Hida, 'Low-power widely tunable Gm-C filter with an adaptive DC-blocking, triode-biased MOSFET transconductor', in *Proceedings of the 30th European*

*Solid-State Circuits Conference*, Sep. 2004, pp. 99–102. doi: 10.1109/ESSCIR.2004.1356627.

[34] T. Sánchez-Rodríguez, J. A. Gomez-Galan, R. G. Carvajal, M. Sánchez-Raya, F. Muñoz, and J. Ramírez-Angulo, 'A 1.2-V 450- $\mu$ W -  $\$C\$$  Bluetooth Channel Filter Using a Novel Gain-Boosted Tunable Transconductor', *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 23, no. 8, pp. 1572–1576, Aug. 2015, doi: 10.1109/TVLSI.2014.2341929.

[35] C. Garcia-Alberdi, A. J. Lopez-Martin, L. Acosta, R. G. Carvajal, and J. Ramirez-Angulo, 'Tunable Class AB CMOS Gm-C Filter Based on Quasi-Floating Gate Techniques', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 5, pp. 1300–1309, May 2013, doi: 10.1109/TCSI.2012.2220504.

[36] R. F. L. Moreno, F. A. P. Barúqui, and A. Petraglia, 'Bulk-tuned Gm-C filter using current cancellation', *Microelectron. J.*, vol. 46, no. 8, pp. 777–782, Aug. 2015, doi: 10.1016/j.mejo.2015.05.010.

[37] Y. C. Lim, W. H. Lai, X. W. Zhang, and M. F. Li, 'Improved cross-coupled quad transconductor cell', *Microelectron. J.*, vol. 31, no. 2, pp. 77–81, Feb. 2000, doi: 10.1016/S0026-2692(99)00082-8.

[38] A. M. Ismail and A. M. Soliman, 'Novel CMOS wide-linear-range transconductance amplifier', *IEEE Trans. Circuits Syst. Fundam. Theory Appl.*, vol. 47, no. 8, pp. 1248–1253, Aug. 2000, doi: 10.1109/81.873880.

[39] K.-C. Kuo and A. Leuciuc, 'A linear MOS transconductor using source degeneration and adaptive biasing', *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 48, no. 10, pp. 937–943, Oct. 2001, doi: 10.1109/82.974782.

[40] S. Sengupta, 'Adaptively biased linear transconductor', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 52, no. 11, pp. 2369–2375, Nov. 2005, doi: 10.1109/TCSI.2005.853516.

[41] F. Rezaei and S. J. Azhari, 'A new controllable adaptive biasing linearization technique for a CMOS OTA and its application to tunable Gm-C filter design', *Microelectron. J.*, vol. 46, no. 9, pp. 810–818, Sep. 2015, doi: 10.1016/j.mejo.2015.06.012.

[42] C. Bocciarelli, F. Centurelli, P. Monsurrò, V. Spinogatti, and A. Trifiletti, 'A class-AB linear transconductor with enhanced linearity', *AEU - Int. J. Electron. Commun.*, vol. 140, p. 153955, Oct. 2021, doi: 10.1016/j.aeue.2021.153955.

[43] J. Wu, Z. Xie, T. Yu, and C. Chen, 'A wide tuning range Gm-C complex filter with master-slave automatic frequency tuning based switched-capacitor', *Microelectron. J.*, vol. 81, pp. 200–207, Nov. 2018, doi: 10.1016/j.mejo.2018.04.009.

[44] A. Lewinski and J. Silva-Martinez, 'A High-Frequency Transconductor Using a Robust Nonlinearity Cancellation', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 53, no. 9, pp. 896–900, Sep. 2006, doi: 10.1109/TCSII.2006.880025.

[45] F. Rezaei, 'Adaptive cancellation linearisation and its application to wide-tunable Gm-C filter design', *IET Circuits Devices Syst.*, vol. 11, no. 5, pp. 478–486, 2017, doi: 10.1049/iet-cds.2016.0474.

[46] A. Tajalli and Y. Leblebici, 'Low-Power and Widely Tunable Linearized Biquadratic Low-Pass Transconductor-C Filter', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 3, pp. 159–163, Mar. 2011, doi: 10.1109/TCSII.2011.2111530.

[47] C. D. Salthouse and R. Sarpeshkar, 'A micropower band-pass filter for use in bionic ears', in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, May 2002, p. V–V. doi: 10.1109/ISCAS.2002.1010672.

[48] Y. Chen, P.-I. Mak, S. D'Amico, L. Zhang, H. Qian, and Y. Wang, 'A Single-Branch Third-Order Pole-Zero Low-Pass Filter With 0.014-mm<sup>2</sup> Die Size and 0.8-kHz (1.25-nW) to 0.94-GHz (3.99-mW) Bandwidth-Power Scalability', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 60, no. 11, pp. 761–765, Nov. 2013, doi: 10.1109/TCSII.2013.2281717.

[49] Winder 'Analog and Digital Filter Design - 2nd Edition'.

[50] R. Arya, G. Souliotis, S. Vlassis, and C. Psychalinos, 'A 0.5 V tunable complex filter for Bluetooth and Zigbee using OTAs', *Analog Integr. Circuits Signal Process.*, vol. 79, no. 1, pp. 73–81, Apr. 2014, doi: 10.1007/s10470-013-0241-5.

[51] V. S. Rajan and B. Venkataramani, 'Design of low power, programmable low-Gm OTAs and Gm-C filters for biomedical applications', *Analog Integr. Circuits Signal Process.*, vol. 107, no. 2, pp. 389–409, May 2021, doi: 10.1007/s10470-020-01748-0.

[52] H. Aminzadeh, 'Systematic circuit design and analysis using generalised g m/I D functions of MOS devices', *IET Circuits Devices Amp Syst.*, vol. 14, no. 4, pp. 432–443, Jan. 2020, doi: 10.1049/iet-cds.2019.0209.

[53] P. Pandey, J. Silva-Martinez, and X. Liu, 'A CMOS 140-mW fourth-order continuous-time low-pass filter stabilized with a class AB common-mode feedback operating at 550 MHz', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 53, no. 4, pp. 811–820, Apr. 2006, doi: 10.1109/TCSI.2005.859621.

[54] Z. Liu, Y. Tan, H. Li, H. Jiang, J. Liu, and H. Liao, 'A 0.5-V 3.69-nW Complementary Source-Follower-C Based Low-Pass Filter for Wearable Biomedical Applications', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 67, no. 12, pp. 4370–4381, Dec. 2020, doi: 10.1109/TCSI.2020.2995351.



**AbdolRasool Ghasemi** was born in Bushehr, Iran, in 1980. He received the M.S. and PhD. (honors) in electronics engineering from Ferdowsi University of Mashhad, Mashhad, Iran in 2006 and 2017, respectively. In 2008, he joined the Islamic Azad University of Bushehr, Bushehr, Iran, where he is currently an assistant professor. His research interests include low-voltage, ultra-low-power analog integrated circuits such as switched-capacitor filters and analog-to-digital converters for biomedical and telecommunication applications.

**Hamed Aminzadeh** (S'05–M'10) received the M.S. and PhD. degrees in electronics engineering in 2008 and 2010, respectively. From 2010 to 2014, he was with the Delft University of Technology, the Netherlands, where he worked on low-voltage power regulation techniques for biomedical implanted devices. Since 2012, he has been also with Payame Noor University, Tehran, Iran, where he is currently an associate professor. His current research interests include modeling and optimization of analog circuits for low-voltage IoT and biomedical devices, and low-power digital-to-analog and analog-to-digital converters design for telecommunication applications. He has coauthored more than 50 papers on international journals and conference proceedings.



**Andrea Ballo** (S'17–M'20) was born in Catania, Italy, in 1990. He received the Laurea degree (summa cum laude) and the Ph.D. degree in electronic engineering from the University of Catania, Italy, in 2016 and 2020, respectively. From 2021 he is a research fellow and Adjunct Professor of electronic devices at the University of Catania, Italy. Actually, he is a member of the editorial board of UWP Journal of Electronics and Electrical Engineering (JEEE) and member of the topical advisory panel of different journals of MDPI, like Applied Sciences and Electronics. His current research interests include low-voltage low-power analog circuit design and analog and mixed electronics for energy harvesting applications.