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Large Area 1.2 kV GaN Vertical Power FinFETs with a Record Switching Figure-of-Merit

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Abstract—This work presents the first experimental study on capacitances, charges and power-switching figure-of-merits (FOMs) for a large-area vertical GaN power transistor. A 1.2 kV, 5 A GaN vertical power FinFET was demonstrated in a chip area of 0.45 mm², with a specific on-resistance of 2.1 mΩ·cm² and a threshold voltage of 1.3 V. Device junction capacitances were characterized and their main components were identified. This was used to calculate the switching charges and practical switching frequencies. Device FOMs were then derived that take into account the trade-offs between conduction and switching power losses. Our GaN vertical FinFETs exhibit high frequency (~MHz) switching capabilities and superior switching FOMs when compared to commercial 0.9-1.2 kV Si and SiC power transistors. This work shows the great potential of GaN vertical FinFETs for next-generation medium-voltage power electronics.

Index Terms— gallium nitride, vertical power transistors, FinFETs, power switching, junction capacitances, switching charges, switching frequency, power switching figure of merits.

I. INTRODUCTION

GaN devices are excellent candidates for next-generation power electronics. Vertical GaN transistors have several potential advantages over lateral GaN transistors: 1) higher breakdown voltage (BV) and current for a given chip area; 2) superior reliability and 3) easier thermal management [1]. Until now, several structures have been demonstrated for vertical GaN power transistors, such as current-aperture vertical electron transistors (CAVETs) [2]–[4] and trench MOSFETs [5]–[7]. However, the fabrication of these devices requires either the epitaxial regrowth or p-type GaN layers, which either greatly increases the fabrication complexity and cost, or limits

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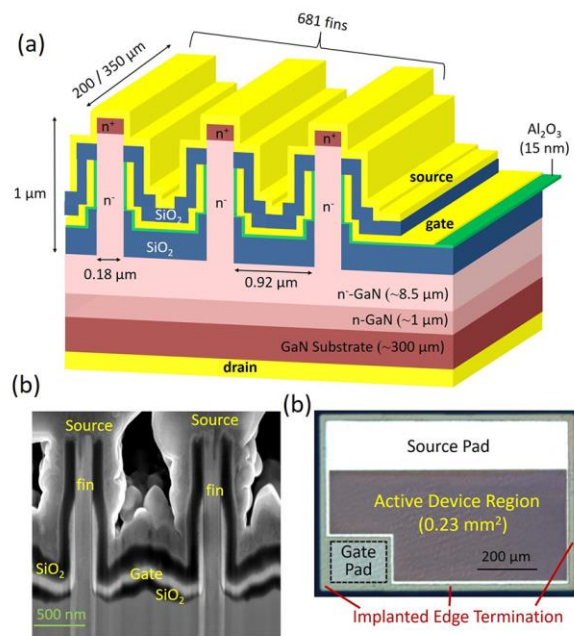


Fig. 1. (a) 3-D schematics of the GaN vertical power FinFETs with multiple fin channels. (b) Cross-sectional SEM image of the fin area in the fabricated device, taken in a focused ion beam system. (c) Optical microscopy image of the fabricated large-area device.

the channel carrier mobility.

Recently, the GaN vertical power FinFET [8]–[10] (Fig. 1 (a)) was demonstrated. This transistor overcomes most of the challenges of CAVETs and trench MOSFETs as it only needs n-GaN layers and does not require epitaxial regrowth. The current in this device is controlled through the fin-shaped n-GaN channels with all-around gate stacks. In narrow fin channels, all electrons can be depleted at zero gate bias due to the work function difference between the gate metal and GaN, enabling normally-off operation. A BV of 1.2 kV and a specific on-resistance ($R_{on,sp}$) of 1 mΩ·cm² have been demonstrated [8] on small devices with tens of fins. 10 A transistors have also been fabricated but their BV was limited to 800 V [8]. To advance the device applications in power converters, large-current 1.2 kV devices are typically required. Critical device parameters for switching considerations, such as capacitance and charges, also need to be characterized.

In this work, we demonstrate a 1.2 kV, 5 A GaN vertical power FinFET by incorporating edge termination structures. Besides BV and $R_{on,sp}$, device capacitance and charges were

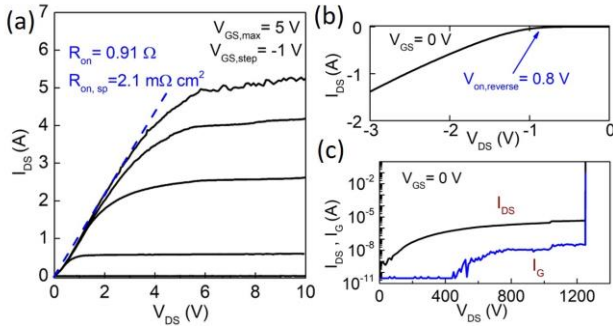


Fig. 2. (a) Device output curves and the extracted R_{on} and $R_{sp,on}$. (b) Reverse conduction curves and the extracted reverse turn-on voltage. (c) Off-state leakage characteristics at $V_{GS}=0$ V with a BV of 1250 V.

characterized for power switching considerations. Switching FOMs were derived and then used to benchmark these devices with other existing 0.9-1.2 kV power transistors.

II. DEVICE FABRICATION & STATIC PERFORMANCE

The epitaxial structure in this work consists of a 0.3 μm -thick n^+ -GaN cap layer (Si : $\sim 2 \times 10^{19} \text{ cm}^{-3}$) and 9.5 μm -thick n -GaN drift layer ($N_D \sim 4 \times 10^{15} \text{ cm}^{-3}$), grown by MOCVD on 2-inch n^+ -GaN substrates. As shown in Fig. 1(c), the large-area device consists of 498 fins with 350- μm fin length and 183 fins with 200- μm fin length. The fin width, fin spacing and height are 0.18 μm , $\sim 0.92 \mu\text{m}$ and $\sim 1 \mu\text{m}$, respectively. The area of active device regions is 0.23 mm^2 . The total device area, including the source/gate pad areas, is $\sim 0.45 \text{ mm}^2$. Device fabrication started with the fin etch and corner rounding [9][11]. Edge termination was then formed, for the first time in vertical GaN FinFETs, below the gate pad edges by argon implantation [12][13]. The details of edge termination will be elaborated in a future paper. After edge termination, the remaining fabrication steps for spacer oxides and gate, source and drain contacts were similar to our previous report [8]. Fig. 1 (b) shows a cross-section scanning electron microscopy (SEM) image of the fin region.

Fig. 2 (a) shows the device output characteristics. The extracted threshold voltage (V_{th}) is 1.3 V (at $I_{DS}=2$ mA) with almost no hysteresis. A high drain current over 5 A and a R_{on} of 0.9 Ω (a $R_{on,sp}$ of 2.1 $\text{m}\Omega \cdot \text{cm}^2$ normalized with the active device area) were obtained. Fig. 2 (b) shows the reverse conduction characteristics, revealing a reverse turn-on voltage ($V_{on,reverse}$) of 0.8 V, which is much smaller than the one in SiC/GaN MOSFETs (typically 2-3 V) as no pn junctions are present in our FinFETs. This low $V_{on,reverse}$ can reduce the power loss and eliminate the need for paralleling a freewheeling diode in many switching applications. Fig. 2 (c) shows the off-state characteristics, revealing a destructive BV over 1.2 kV (occurring at edge termination regions) with a μA -level leakage current at BV . The leakage current at high bias exhibits a $\ln(I) \propto V$ relation, indicating the variable-range-hopping through dislocations as the dominant leakage mechanism [14].

Device junction capacitances C_{ds} , C_{gs} and C_{gd} were measured as a function of V_{DS} (Fig. 3 (a)). C_{gs} and C_{gd} dominate the device capacitance, while C_{ds} is very small as the fin region is fully depleted at zero gate bias. Fig. 3 (b) illustrates the main components of C_{gs} and C_{gd} in both device active regions and pad/edge regions. The C_{gs} in device active regions

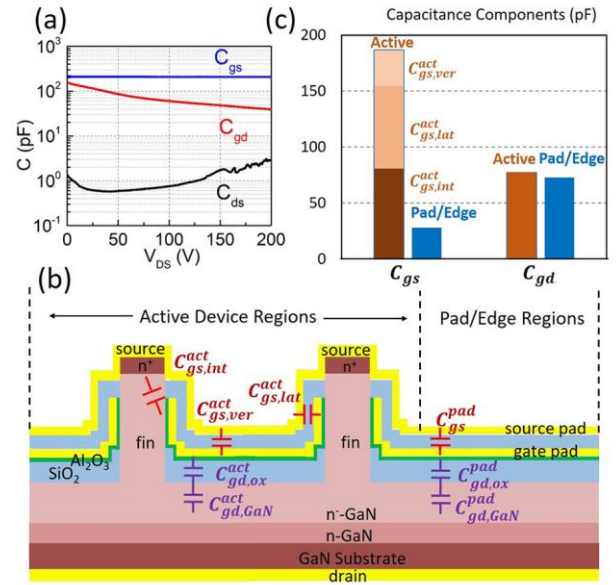


Fig. 3. (a) Device junction capacitances C_{ds} , C_{gs} and C_{gd} measured by using the Agilent B1505A power device analyzer and a custom-built RC circuit. (b) Schematics of different C_{gs} and C_{gd} components in the active and pad/edge regions of a GaN vertical FinFET. (c) Calculated components break-out for the measured C_{gs} and C_{gd} .

consists of three parts: intrinsic gate-source capacitance, $C_{gs,int}^{act}$, vertical parasitic capacitance, $C_{gs,ver}^{act}$, and lateral parasitic capacitance, $C_{gs,lat}^{act}$. The C_{gs} in the pad/edge regions only has the $C_{gs,ver}^{act}$ component. The C_{gd} consists of two parts: MOS capacitance, $C_{gs,ox}$, and drift-layer-depletion capacitance, $C_{gs,GaN}$. With the geometry parameters extracted from Fig. 1 (b), all oxide-based capacitances can be calculated based on the parallel-plate approximation (calculation details will be elaborated in a future paper). Fig. 3 (c) shows the calculated components break-out for C_{gs} and C_{gd} . The parasitic capacitance in the pad/edge regions can be further reduced by optimizing the device layout to minimize the source-gate overlap and gate pad areas in these regions.

Input capacitance $C_{iss}(=C_{gs}+C_{gd})$, output capacitance $C_{oss}(=C_{gd}+C_{ds})$, and reverse capacitance $C_{rss}(=C_{gd})$, were then calculated for our GaN FinFETs, showing lower values than comparable 1.2 kV SiC and Si power transistors (see Table I).

III. SWITCHING CHARGES & FOMS

In general, device power loss under switching operations consists of the conduction losses, switching losses and the losses related to device/diode reverse conduction [15]–[17]:

$$\begin{aligned} P &= P_{cond} + (P_{gate} + P_{Q_{oss}}) + P_{rr} \\ &= I^2 R_{on} D + Q_G V_G f_{sw} + Q_{gd} V_{DS} f_{sw} I_{DS} / I_G + P_{rr} \text{ (Hard SW)} \\ &= I^2 R_{on} D + Q_G V_G f_{sw} + Q_{oss} V_{DS} f_{sw} + P_{rr} \text{ (Soft SW)} \end{aligned} \quad (1)$$

where D is the duty cycle and f_{sw} is the switching frequency.

Based on the dominant switching loss in specific switching applications, different FOMs have been proposed to benchmark the performance of power devices, such as the $R_{on} \cdot Q_{gd}$ for high-voltage hard-switching [16] and the $R_{on} \cdot (Q_{oss} + Q_G)$ for resonant and soft-switching [17]. In these FOMs, the R_{on} accounts for conduction losses and the charges account for

TABLE I. Summary and benchmark of device technologies and their key device metrics for 900-1200 V power switching applications.

Device Technology	Manufacturer / Maker	$R_{on,sp}$ ($m\Omega cm^2$) (R_{on})	BV (kV)	I_{rate} (A)	Chip Area (mm^2)	V_{TH} (V)	C_{ISS} (pF)	C_{OSS} (pF)	Q_G (nC)	Q_{GD} (nC)	Q_{rr} (nC)	Switching FOM ($n\Omega \cdot C$) $R_{on} \cdot (Q_G + Q_{GD})$ $R_{on} \cdot (Q_G + Q_{GD} + Q_{rr})$
GaN Vertical FinFET (this work)	MIT	2.1 (0.91 Ω)	1.2	5	0.45	1.3	248.3*	42.2*	1.24	2.42	-0	3.3 ~2.0 (pad optimized)
SiC MOSFET (CPM2-1200-0160B)	Cree	2.7 [19] (0.16 Ω)	1.2	20	6.28	2.5	525	47	34	14	105	7.68 24.48 (include Q_{rr})
SiC JFET Cascode (UJN1208Z)	United SiC	1.7** (0.15 Ω)	1.2	18.4	>1.13***	4.4	738	58	30	6	63	5.4 14.85 (include Q_{rr})
Si IGBT (NGTB15N120FLWG)	ON Semi	~20 (~0.25 Ω)	1.2	15	320	2	3600	110	150	68	1500	54.5 429.5 (include Q_{rr})
Si CoolMOS (IPD90R1K2C3)	Infineon	~8**** (1.2 Ω)	0.9	5	~23.6	3	710	35	28	12	3700	48 4488 (include Q_{rr})
GaN HEMT Cascode [20]	Transphorm	(0.19 Ω)	1.2	>20	N.A.	2.3	N.A.	43.1	10	N.A.	N.A.	N.A.
Vertical GaN MOSFET [5]	TOYODA GOSEI	2.7	1.2	23.2	2.25	3.5						N. A.
Vertical GaN CAVET [2]	Avogy	2.2	1.5	2.3	0.17	0.5						

Note: *@ $V_{DS}=200$ V; **Source: <http://unitedsic.com/cascodes>; ***Calculated by using the R_{on} in the data sheet and the reported $R_{on,sp}$, reflecting the active device area (not including pad/edge areas); ****Source: Infineon's application note titled "CoolMOS™ C7: Mastering the Art of Quickness".

switching losses. To evaluate the performance of our new GaN vertical FinFETs in a broad range of power switching applications, the following power switching FOM is used considering all possible conduction and switching losses:

$$FOM_{sw} = R_{on}(Q_G + Q_{gd} + Q_{rr}) \quad (2)$$

This FOM is independent of device area or current ratings, and is suitable for evaluating our devices for both hard and soft switching (as $Q_{oss} \approx Q_{gd}$ for our devices). As only majority carriers are involved in our devices, $Q_{rr} \approx 0$. Q_G is the amount of charge provided by the gate driver circuit to charge/discharge the C_{iss} during the device switching. As C_{iss} changes very little with junction biases, $Q_G \approx C_{iss}V_G$, where V_G is the gate bias for device on-state operation. Q_{gd} is the amount of charge depleted in the drift region in the off-state. As the drift layer is designed to be fully depleted at 1.2 kV for our device (punch-through model), $Q_{gd} = qN_D t_D A$. Then the FOM of our GaN vertical FinFETs is given by:

$$FOM_{sw}^{FinFETs} = R_{on}(C_{iss}V_G + qN_D t_D A) = 3.3 n\Omega \cdot C \quad (3)$$

where V_G of 5 V is used; N_D ($\sim 4 \times 10^{15} \text{ cm}^{-3}$) and t_D (8.5 μm) is the net donor concentration and thickness of the drift region between the gate and drain, respectively; and A is the total device area ($\sim 0.45 \text{ mm}^2$).

Switching frequency of power devices is a compromise between the conduction and switching losses. Sound design typically requires these two losses to be about the same [18]. Given this design approach, from Eqn. (1), a practical f_{sw} of ~ 3.5 MHz is calculated for our 1.2 kV GaN vertical FinFETs, which is much higher than 1.2 kV Si IGBTs (10-20 kHz).

Table I summarizes the key device metrics of our 1.2 kV GaN vertical FinFETs, including the chip area, R_{on} , BV , V_{th} , capacitances, switching charges and FOMs, benchmarked against state-of-the-art commercial 0.9-1.2 kV Si and SiC [19] power transistors. Other large-area 0.9-1.2 kV GaN devices at the R&D level [2][5][20] are also included, although, to the best of our knowledge, there is no complete experimental data reported so far for the capacitance and charges of these devices.

As shown, our device exhibited the best power switching FOMs among all 0.9-1.2 kV power transistors. This is attributable to the combination of the superior physical properties of GaN (high critical electric field and high mobility) and the merits of our vertical FinFET (small capacitances, low V_G and no Q_{rr}).

Despite the excellent performance, there is still much room for improvement in our GaN vertical FinFETs. For example, if the pad capacitances can be minimized, the FOM could be reduced to $\sim 2 \text{ n}\Omega \cdot C$. On the other hand, the fin spacing currently used in our devices (0.92 μm) is relatively large compared to the fin width (0.18 μm). This indicates large room for improvement in $R_{on,sp}$, junction capacitances and charges by shrinking the fin spacing. From the fabrication point of view, the fin spacing could be well reduced to below 0.3 μm , while the derivation of the optimum fin spacing requires a more comprehensive consideration of spreading resistance, capacitances and heat dissipation. We will do this derivation in the future work.

IV. SUMMARY

This work demonstrates a large-area 1.2 kV, 5 A GaN vertical power FinFET. Systematic device characterization of R_{on} , BV , V_{th} and capacitances is presented, followed by the charge analysis and FOM derivation for power switching applications. Our device shows superior power switching FOMs when compared to commercial 0.9-1.2 kV Si and SiC power transistors. This performance demonstrates the great potential of GaN vertical FinFETs for next-generation medium-voltage and high-frequency power applications.

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