Large-Area Compliant Tactile Sensors Using Printed Carbon Nanotube Active-Matrix Backplanes

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Fabrication of devices and sensors on flexible substrates allows for conformal coverage of electronic systems on nonplanar surfaces,[1,2] thus enabling new functionalities. Potential applications include flexible displays,[3–7] wearable electronics,[1,8–14] interactive surfaces,[2,11,15] and electronic wallpapers.[16] In many applications, large-area coverage of electronics beyond the size limits of conventional batch processing is desirable. In this regard, the use of printing processes is of tremendous advantage. Over the past several years, significant progress has been made in the development of printing techniques based on organic molecules[17–19] and polymers,[20–23] nanoparticles,[24,25] nanowires,[26,27] and single-walled carbon nanotubes (SWCNTs).[28–32] Printed devices have been readily configured as the building blocks for various electronic systems.[3,18,32,33] Each material system and printing technique presents unique advantages and disadvantages, depending on the specific needs of the targeted application. For instance, partly and fully printed SWCNT transistors have been reported in the past,[28,30,31,33] exhibiting excellent electrical properties,[33] high air-stability,[33] with low sensitivity to strain due to their miniaturized diameters.[31] Particularly, we recently demonstrated multistep gravure printing of thin film transistors (TFTs) utilizing semiconductor-enriched SWCNTs as the active channel material with printed Ag source/drain/gate electrodes and inorganic/organic high-κ gate dielectrics.[31] Building on these recent advancements, here, we demonstrate the fabrication of an active-matrix backplane consisting of a 20 × 20 SWCNT TFT array through a printed process scheme. Backplanes are the critical component for any multipixel system, such as displays or sensor arrays, since they reduce the number of addressing lines in an arbitrarily large $m \times n$ matrix from $m \times n$ to just $m + n$. In addition, active matrices offer significant advantages over passive matrices in terms of power consumption and contrast, which are critical for increased scaling[34] and resolution.[35] As an example demonstration, we integrate the printed SWCNT active-matrix backplane with tactile sensor arrays for large-area pressure mapping. The demonstrated system presents a scalable route toward realization of user-interactive surfaces, capable of spatial and temporal mapping of stimuli over large-areas.

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The fabrication of the active-matrix backplane is performed by using a custom-built roll-to-plate gravure printing tool (Figure S1a, Supporting Information). The backplane consists of a 20 × 20 pixel matrix with an area of 45 cm^2, limited by the size of the tool used in this work, although the gravure printing process is known to be scalable to much larger sample areas.[32,36] Each pixel consists of a printed SWCNT TFT integrated with a pressure sensor on top, with the TFT used to address the pixel for the signal readout. The printer uses a dual camera setup to align the substrate with the engraved plate so that each subsequent printed layer can be properly aligned to the layers underneath with an alignment accuracy of down to 10 μm. The engraved plates consist of small cells etched into chrome plated copper plates which are filled with the desired ink. The design of the cells is critical to minimize ink bleeding outside of the desired printing areas (see Figure S1b,c, and Discussion S1, Supporting Information). If not designed properly, it can lead to variation in TFT performance due to variation in the channel length, and in the worst case scenario, shorting of the source and drain (S/D) electrodes, affecting pixel yield and reliability.

Figure 1a depicts the fabrication process for the flexible TFT backplane. First, solution processing is used to assemble a random network of semiconductor-enriched SWCNTs onto a poly(ethylene terephthalate) (PET) substrate. The PET is initially cleaned with oxygen plasma and then surface functionalized with poly(L-lysine) (0.1% w/v in H_2O, Sigma–Aldrich) by immersion for 5 min followed by a rinse with deionized (DI) water. This surface functionalization serves as an adhesion layer for subsequent SWCNT assembly. A 99% semiconductor-enriched SWCNT solution (NanoIntegris, Inc.) is dropcast onto the PET surface for 2 h and then rinsed off with DI water. After SWCNT deposition, the S/D electrodes of the TFT are printed onto the substrate by using silver nanoparticle ink (PG-007AA; Paru Corporation, Korea) with a channel length and width of 100 μm and 1.25 mm, respectively. After the S/D deposition, a dielectric layer (≈1 μm in thickness) is printed over the channel regions of the TFTs by using a commercial ink composed of high-κ barium titanate ($BaTiO_3$) (BTO) nanoparticles embedded within a poly(methyl methacrylate) (PMMA) binder (PD-100; Paru Corporation, Korea). This dielectric layer is then used as a hard mask to pattern and etch the SWCNTs. Specifically, the sample is exposed to oxygen plasma (120 W for 2 min) to etch away the SWCNTs not covered by the S/D and BTO/PMMA layers so that the CNTs are only present in the active regions of the TFTs. A second, BTO/PMMA layer (≈2 μm in thickness) is then

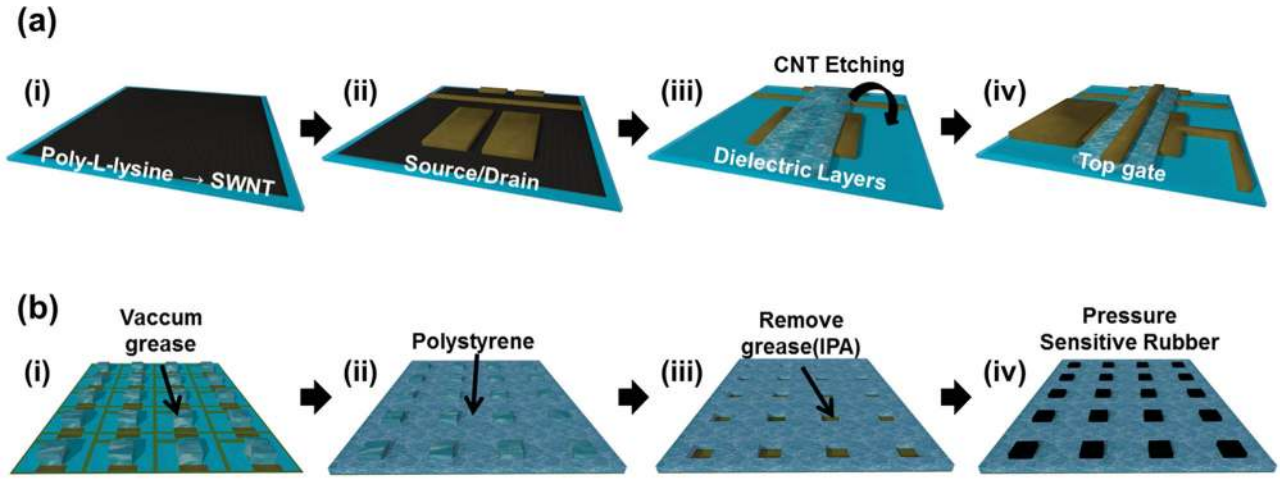

Figure 1. Fabrication of the pressure sensor array: a) First, a 99% carbon nanotube suspension was dropcast onto the PET surface after surface functionalization with poly(L-lysine). The S/D metal layer was then printed onto the SWCNT coated surface followed by a BTO dielectric layer over only the S/D channel region. After O_2 plasma etching of the SWCNTs, two more BTO layers were printed followed by printing of the gate metal layer. b) Vacuum grease was dropped onto the source pads of the printed backplane which was then coated with a layer of polystyrene solution. After annealing for 20 min at 150 °C, the vacuum grease was removed with isopropyl alcohol and individual squares of PSR were placed inside the vias.

printed over the channel to minimize the gate leakage current as the first BTO layer is partially damaged during the oxygen plasma etch. To ensure no pinholes exist between the drain lines and the gate lines of the backplane, a third BTO/PMMA layer (≈1 µm) is printed over the metal interconnect overlap regions of the matrix (Figure S2, Supporting Information). Finally, the top gate layer, composed of the same Ag nanoparticle ink as the S/D lines is printed over the BTO/PMMA gate dielectric to complete the fabrication of the active matrix. The gate electrodes overlap S/D by ≈50 µm on each side. More details of the fabrication process can be found in the Experimental Section and Table S1, Supporting Information.

In order to demonstrate the use of printed TFTs as an active-matrix backplane for a sensor network, pressure sensors are integrated on top of the backplane using a pressure sensitive rubber (PSR) (PCR Technical). The PSR acts as a variable resistor in this setup between the source of the transistor and ground. As the applied pressure increases, the resistance of the PSR drops, allowing the normally insulating rubber to be conductive. The change of conductance in the PSR is due to the reduction of the spacing between conductive carbon particles embedded in the film, thus enhancing the tunneling current upon induced pressure.

Figure 1b shows the process flow for integrating the pressure sensors. First, vacuum grease (Dow Corning) is dropcast onto the source pad of each TFT in the matrix, and then fully coated with a solution composed of polystyrene ($M_w \approx 350\,000$ g mol^{-1}, Sigma–Aldrich) and diethylene glycol monoethyl ether acetate (99%, Sigma–Aldrich) via drop-casting and spreading using an air gun as an insulating layer. The polystyrene solution is cured onto the backplane by baking the sample at 150 °C for 20 min. The vacuum grease is then removed using isopropyl alcohol, thus opening up the source pads of each pixel for integration with the PSR. The depth of these vias in the polystyrene insulating layer, measured using a profilometer (NanoSystem Co.,Ltd, NV-2200), is approximately 27.6 µm (Figure S3, Supporting Information). PSR films cut to a slightly smaller size than the vias are picked and placed individually into the vias as the through via contact. Finally, a silicone rubber coated with a layer of conductive carbon is laminated on top of the completed device as a universal ground output.

Figure 2a shows an optical image of the printed TFT backplane before PSR integration, along with a zoomed-in image of a single TFT pixel. Figure 2b shows a scanning electron microscope (SEM) image of the PET film after SWCNT deposition, showing a clear high-density percolation network of nanotubes. From the cross-sectional SEM image in Figure 2c, it can be seen that the S/D lines are ≈1 µm thick, the total dielectric thickness is ≈3 µm, and the thickness of the top gate is ≈0.5 µm.

After the fabrication was concluded, the transfer characteristics of individual TFTs in the backplane were analyzed. All the devices were measured at room temperature in ambient conditions. **Figure 3**a depicts a drain current versus gate voltage (I_{DS}–V_{GS}) graph of a representative TFT at drain voltages of −1 and −5 V. Figure 3b shows the I_{DS} −V_{GS} plots of the 388 working TFTs out of a total of 400 in the backplane at a drain voltage of −5 V. It is important to note that the yield of the working TFTs in the backplane, printed in ambient conditions, was 97%. The main failure modes for the devices were short circuits between the source and drain contacts or pinholes in the BTO gate dielectric, which can be attributed to printing in an uncontrolled environment, where fluctuations in temperature and humidity can change the spreading and printing properties of the inks and particles in the air can obstruct the ink. Figure 3c–g shows the statistical histograms for the 388 working TFTs. At a drain voltage of −5 V, the average on-current density normalized per unit width of the TFTs was measured to be 4 ± 2 µA mm^{-1} (Figure 2c). The TFTs also have an average on/off current ratio of ≈10^4 (Figure 3d), which facilitates a low enough off-current level for distinguishing between pressure loading and unloading. The average threshold voltage of the TFTs is −3 ± 0.6 V (Figure 3e). The negative threshold voltage, indicating enhancement mode behavior of the TFTs, is important for the operation of the backplane. Otherwise, a positive gate voltage must be applied to the pixels that are not being accessed

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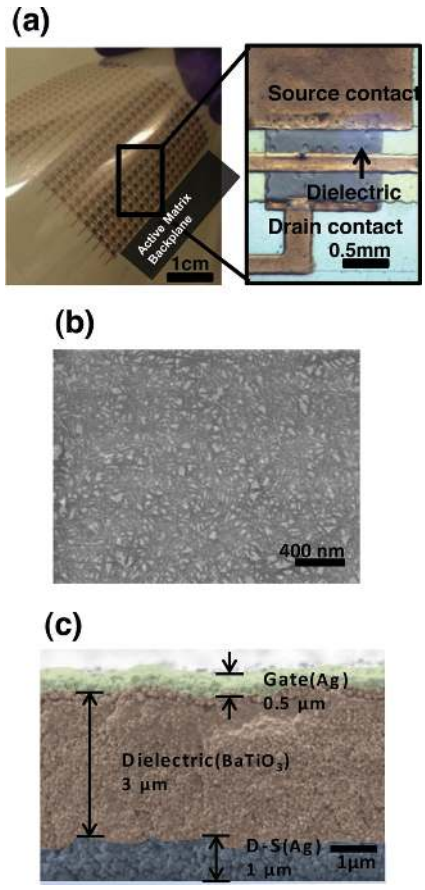

Figure 2. Images of printed SWCNT TFT array: a) An optical image of a printed active-matrix backplane along with a zoomed-in image of a single TFT pixel. b) An SEM image of the PET surface after SWCNT deposition. c) False-color cross-sectional SEM image of the printed TFT.

to avoid signal cross-talk between the pixels while the backplane is being mapped. While the relatively large subthreshold swings of the TFTs do result in a noticeable drain current at zero gate voltage in our devices, this leakage current level is still sufficiently low to allow for mapping of applied pressure as demonstrated later. The average transconductance and field-effect mobility of the TFTs are calculated to be 0.4 ± 0.2 µS mm^{-1} (Figure 3f) and 0.8 ± 0.3 cm^2 V^{-1} s^{-1} (Figure 3g), respectively. The mobility calculations were done using a parallel plate model following the equation: $\mu = Lg_m/(|V_{DS}|C_{OX}W)$ where g_m is the transconductance, L and W are the channel lengths and widths of the TFTs, respectively, V_{DS} is the applied drain bias of –5 V, and C_{OX} is the capacitance per unit area, measured to be 9.5 nF cm^{-2} using an LCR meter and parallel-plate capacitor test structures. We speculate that the mobility is lower than our previous work on printed TFTs possibly due to different printing conditions which result in different layer thicknesses/overlap areas increasing parasitics as well as partial damage to the nanotube channel due to the use of oxygen plasma to etch away carbon nanotubes not within the TFT channels. In the future, printing conditions can be better optimized and a thicker dielectric can be printed to serve as a more robust hard mask.

Figure 4a shows the equivalent circuit diagram of a single pixel in the array, consisting of a TFT with its source connected to ground through the PSR, which acts as a variable resistor. Figure 4b shows the pressure response of a representative pixel with an applied drain voltage of –5 V in the array. Here, the pixel consists of a TFT with its source connected to ground through the PSR, which acts as a pressure sensitive variable resistor. The response time of the pixel is limited to operations below ≈15 Hz due to the response time of the PSR,[37] which is still sufficient for many applications such as human tactile pressure sensing. As more pressure is applied, the PSR becomes more conductive and thus the on-current of the pixels increase. The pixels are sensitive to pressures ranging from ≈1 kPa up to 20 kPa, with a linear sensitivity of ≈800% kPa^{-1} (Figure 4c), corresponding to pressures similar to that of a light human touch.

To conduct pressure mapping using the whole array, a block of polydimethylsiloxane (PDMS) (Sylgard 184, Dow Corning) is cut out in the shape of a "*C*" and placed on top of the sensor array (**Figure 5**a,b). The mapping is done by applying –5 V on the drain (column select) and –10 V on the gate (row select) lines as shown in Figure 5c and then measuring the current out of the PSR common ground for each pixel. Figure 5d–f shows the output current maps of the sensor matrix without applying pressure, with only the PDMS *C* slab (≈0.7 kPa), and with 6.5 kPa of pressure applied onto the PDMS slab (total 7.2 kPa). As expected, when no pressure is applied, all of the pixels are in the off-state, with on-currents <100 nA. When a pressure of 0.7 kPa was applied, some pixels begin to turn on, but no clear response is observed as the applied pressure is below the sensing threshold of 1 kPa for the pixels. When 7.2 kPa was applied, the output current of the pixels underneath the PDMS block increases up to ≈1 µA while the output current of the pixels not underneath the PDMS mostly remain <100 nA, reflecting the applied pressure.

Since the backplane is fabricated on a flexible substrate, one advantage is that it can be bent to cover nonplanar surfaces. To test the operation of our devices under such circumstances, the I_{DS}–V_{GS} behavior of a representative TFT on the backplane was measured while it was flat and subsequently wrapped around a cylinder with a radius of ≈1.85 cm. As can be seen in **Figure 6**, there is virtually no change in the transfer characteristics of the transistor. The ability for the TFTs to operate while under strain comes from the excellent mechanical properties of the carbon nanotubes which we have used as the active channel material, as well as the organic binder components of the printed Ag and BTO inks. This shows that our printed backplane may be operated while laminated conformally around nonplanar surfaces, preventing potential crosstalk between lateral strain and the applied tactile pressure in the vertical direction being measured.

In conclusion, we have demonstrated a pressure sensor array capable of mapping out the applied pressure over an area using a printed active-matrix TFT backplane. We are able to achieve a yield of 97% out of 400 individual TFTs with very reasonable performance variation between the transistors. While only a pressure sensor array is described in this work, the active-matrix backplane could be integrated with a variety of other sensors such as photodetectors[1] or implemented as the backplane for a flexible display.[4,15] Also, the TFTs in the backplane see virtually no change in performance while under strain,

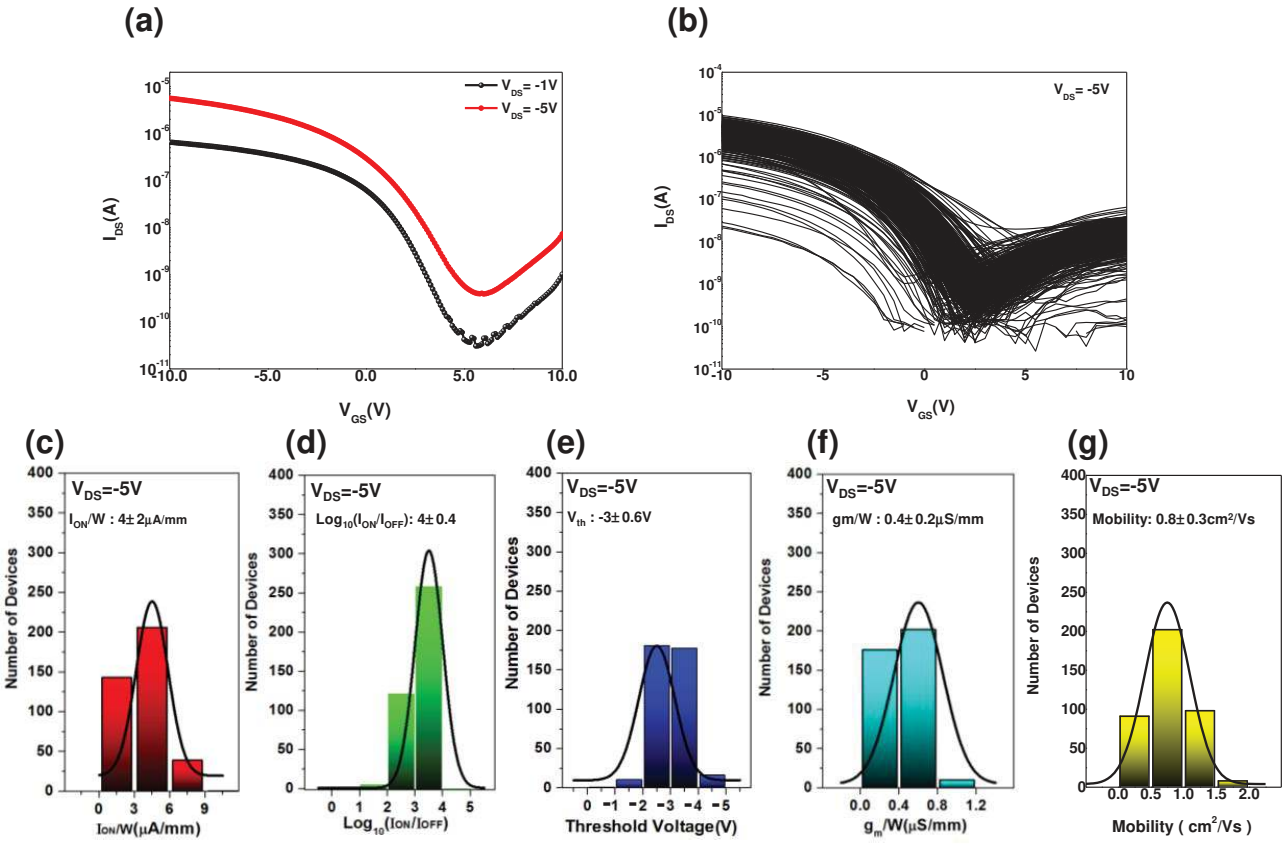

Figure 3. Electrical characterization of TFTs: a) Transfer curve of a representative TFT in the array at a drain voltage of –1 and –5 V. b) Transfer curves of the 388 working TFTs in the printed backplane at a drain voltage of –5 V. c–g) Histograms of the TFTs showing the statistical distribution of c) normalized on-current, d) log of the on/off ratio, e) threshold voltage, f) transconductance, and g) field-effect mobility. Channel length and width of the devices are 100 μm and 1.25 mm, respectively.

allowing it to be used in applications where it may be placed onto a nonplanar surface. It is also important to note that while the roll-to-plate gravure process used in this work limits the size of the backplane, all methods reported here can be transferred into a fully printed roll-to-roll gravure printing process[36] that could scale up the production of the backplane and sensor network to arbitrarily large sizes for truly ubiquitous sensor networks.

Experimental Section

Printing of the Active-Matrix Backplane: A blank PET substrate was first exposed to oxygen plasma at 120 W for 2 min. Poly(L-lysine) solution was dropcast onto the substrate for 5 min and then rinsed with deionized (DI) water and dried with N_2 gas. The 99% semiconducting CNT solution was then dropcast onto the surface for 2 h and then rinsed with DI water and dried with N_2 gas. The PET substrate with CNTs everywhere was then attached to the roller of the printer. To print the S/D layer,

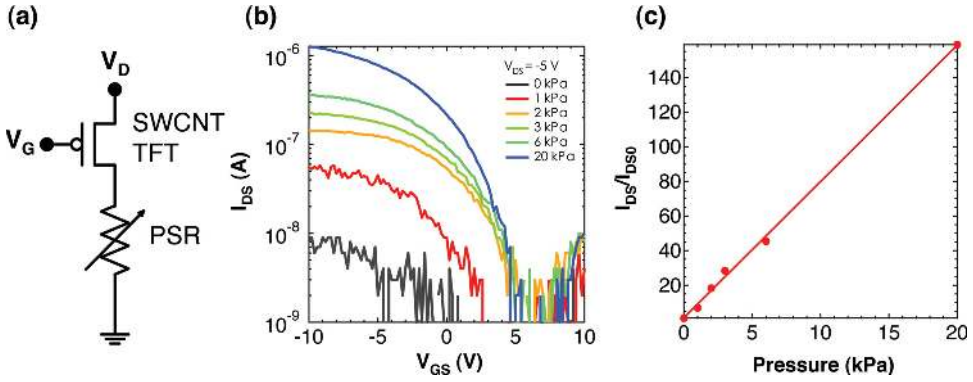

Figure 4. Single-pixel pressure sensing: a) Equivalent circuit diagram of a single pixel in the TFT array with the PSR acting as a variable resistor in series with the SWCNT TFT. b) Transfer curves of a representative pixel with varying amounts of applied pressure (from 0 to 20 kPa) at a drain voltage of –5 V. c) Plot of the ratio of on-current (at a gate voltage of –10 V) versus applied pressure. I_{DS0} is the drain current at zero applied pressure (at 0 kPa).

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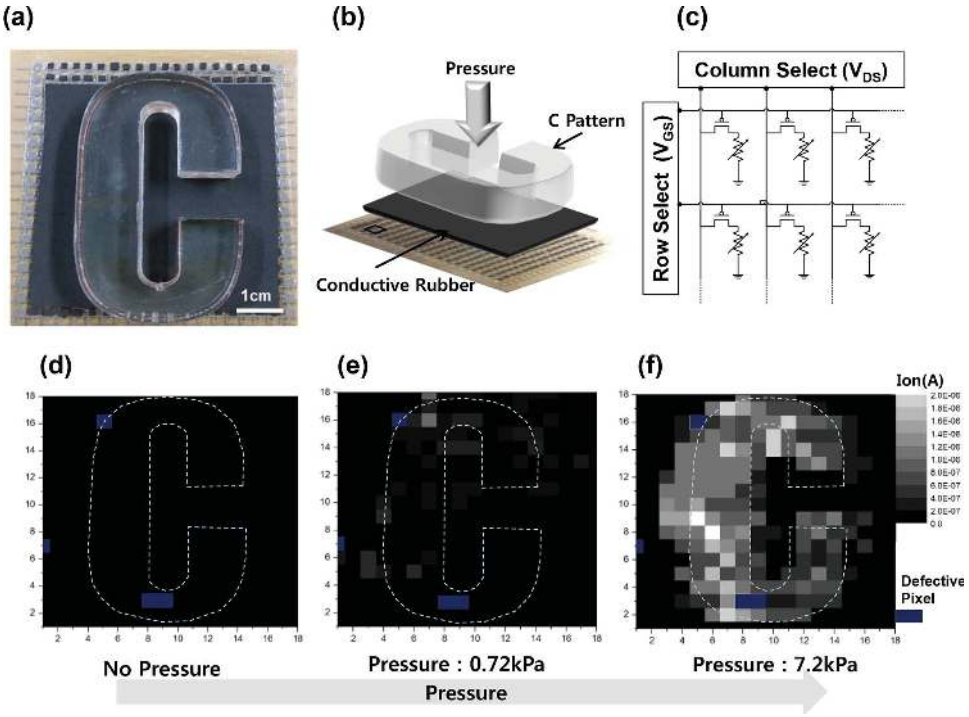

Figure 5. Pressure mapping: a) Optical image of the printed TFT backplane with the PDMS slab in the shape of a *C*, placed on top of the universal ground sheet. b) Schematic drawing of the measurement method for mapping pressure. c) Equivalent circuit diagram of the pressure sensitive array. Drain voltages act as the column select while gate voltages act as the row select to control each individual pixel. d–f) Output currents of the array at applied pressures of d) 0 kPa, e) 0.7 kPa, and f) 7.2 kPa.

the silver ink composite was dropped onto one edge of the engraved plate. Using a doctor blade, the ink was spread out into the wells of the plate with all excess ink removed. The engraved plate was then brought into contact with the PET substrate on the roller with an applied force of 5 kg and then passed under the roller with a speed of 100 mm s^{-1}. After printing, the PET substrate was detached from the print roller and baked in an oven at 150 °C for 30 s. To print the first BTO layer, which is only placed over the channels between the source/drain pads, the PET substrate was once again attached to the roller. Using an alignment camera on the printer, the engraved plate was aligned to the substrate using two alignment marks at the ends of the printed areas. The BTO ink solution was then spread into the engraved plate and then printed onto the PET in the same manner as the S/D layer except the contact force was increased to 8 kg and printing speed lowered to 50 mm s^{-1}. The PET substrate was then baked at 150 °C for 1 min. Then the substrate was placed into an oxygen plasma system

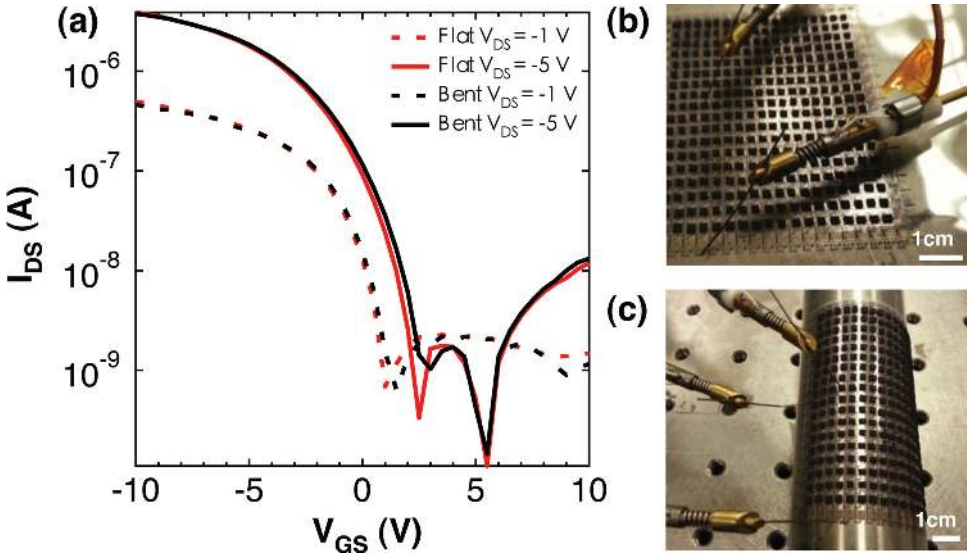

Figure 6. TFT performance under strain: a) Transfer curves of a representative TFT while flat and when bent around a rod with a radius of curvature of ≈1.85 cm. b) Optical image of the device measurement while flat and c) when bent around the rod.

and exposed to oxygen plasma for 2 min at 120 W to etch away all of the CNTs that are not covered by the S/D or BTO layer. Afterward, a second BTO layer was printed onto the substrate in a continuous line covering both the overlap between the gate metal lines and S/D metal lines in the transistor regions as well as the interconnect regions. A third BTO layer was printed using the same engraved plate and conditions as the first BTO layer, except the alignment was offset to cover the metal interconnect regions to ensure the removal of any pinholes. Finally, the gate layer was printed on and a final 150 °C bake in an oven for 1 h was done. All the printing pressures and print speeds for each layer can be found in Table S1, Supporting Information.

Integration of the Pressure Sensors: First, vacuum grease was dropped onto the source contacts of each pixel. Then, a solution of polystyrene and diethylene glycol monoethyl ether acetate was spread out over the entire backplane and cured for 20 min in an oven at 150 °C. Using isopropyl alcohol, the vacuum grease was removed to expose the source contacts. Small PSR pieces were individually placed into the source vias. Finally, a sheet of silicone rubber coated with a layer of conductive carbon tape is laminated over the device as the universal ground output of the sensor array to complete the fabrication process.

Device Measurement: All of the current versus voltage measurements were taken using an Agilent B1500A semiconductor device parameter analyzer. To collect the I_{DS}–V_{GS} data shown in Figure 2, the gate and drain probes were placed at the ends of their respective lines in the array, while the source probe was placed directly onto the source contact of each pixel. To obtain the pressure mapping plots, the source probe is connected to the conductive carbon tape, away from the active sensing area to avoid applying pressure to the PSR and I_{DS}–V_{GS} measurements were taken of each pixel with the pressure applied. The on-currents at $V_{GS} = -10$ V and $V_{DS} = -5$ V were then plotted.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] T. Takahashi, K. Takei, A. G. Gillies, R. S. Fearing, A. Javey, *Nano Lett.* **2011**, *11*, 5408.
[2] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 12321.
[3] T. Sekitani, H. Nakajima, H. Maeda, T. Fukushima, T. Aida, K. Hata, T. Someya, *Nat. Mater.* **2009**, *8*, 494.
[4] J. Zhang, C. Wang, C. Zhou, *ACS Nano* **2012**, *6*, 7412.
[5] C. Wang, J. Zhang, K. Ryu, A. Badmaev, L. G. De Arco, C. Zhou, *Nano Lett.* **2009**, *9*, 4285.
[6] J. Zhang, Y. Fu, C. Wang, P.-C. Chen, Z. Liu, W. Wei, C. Wu, M. E. Thompson, C. Zhou, *Nano Lett.* **2011**, *11*, 4852.
[7] Z. Yu, X. Niu, Z. Liu, Q. Pei, *Adv. Mater.* **2011**, *23*, 3989.
[8] Y.-L. Park, B.-R. Chen, R. J. Wood, *IEEE Sens. J.* **2012**, *12*, 2711.
[9] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, T. Sakurai, *Proc. Natl. Acad. Sci. USA* **2004**, *101*, 9966.
[10] K. Takei, T. Takahashi, J. C. Ho, H. Ko, A. G. Gillies, P. W. Leu, R. S. Fearing, A. Javey, *Nat. Mater.* **2010**, *9*, 821.
[11] S. C. B. Mannsfeld, B. C. -K. Tee, R. M. Stoltenberg, C. V. H.-H. Chen, S. Barman, B. V. O. Muir, A. N. Sokolov, C. Reese, Z. Bao, *Nat. Mater.* **2010**, *9*, 859.
[12] G. Schwartz, B. C.-K. Tee, J. Mei, A. L. Appleton, D. H. Kim, H. Wang, Z. Bao, *Nat. Commun.* **2013**, *4*, 1859.
[13] W.-H. Yeo, Y.-S. Kim, J. Lee, A. Ameen, L. Shi, M. Li, S. Wang, R. Ma, S. H. Jin, Z. Kang, Y. Huang, J. A. Rogers, *Adv. Mater.* **2013**, *25*, 2773.
[14] D.-H. Kim, N. Lu, R. Ghaffari, Y.-S. Kim, S. P. Lee, L. Xu, J. Wu, R.-H. Kim, J. Song, Z. Liu, J. Viventi, B. de Graff, B. Elolampi, M. Mansour, M. J. Slepian, S. Hwang, J. D. Moss, S.-M. Won, Y. Huang, B. Litt, J. A. Rogers, *Nat. Mater.* **2011**, *10*, 316.
[15] C. Wang, D. Hwang, Z. Yu, K. Takei, J. Park, T. Chen, B. Ma, A. Javey, *Nat. Mater.* **2013**, *12*, 899.
[16] R. Wisnieff, *Nature* **1998**, *394*, 225.
[17] J. A. Rogers, Z. Bao, A. Makhija, P. Braun, *Adv. Mater.* **1999**, *11*, 741.
[18] V. Subramanian, P. C. Chang, J. B. Lee, S. E. Molesa, S. K. Volkman, *IEEE Trans. Compon. Packag. Technol.* **2005**, *28*, 742.
[19] T. Sekitani, M. Takamiya, Y. Noguchi, S. Nakano, Y. Kato, T. Sakurai, T. Someya, *Nat. Mater.* **2007**, *6*, 413.
[20] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E. P. Woo, *Science* **2000**, *290*, 2123.
[21] Y.-Y. Noh, N. Zhao, M. Caironi, H. Sirringhaus, *Nat. Nanotechnol.* **2007**, *2*, 784.
[22] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler, A. Facchetti, *Nature* **2009**, *457*, 679.
[23] J.-U. Park, M. Hardy, S. J. Kang, K. Barton, K. Adair, D. kishore Mukhopadhyay, C. Y. Lee, M. S. Strano, A. G. Alleyne, J. G. Georgiadis, P. M. Ferreira, J. A. Rogers, *Nat. Mater.* **2007**, *6*, 782.
[24] S. B. Fuller, E. J. Wilhelm, J. M. Jacobson, *J. Microelectromechanical Syst.* **2002**, *11*, 54.
[25] V. Subramanian, J. M. J. Frechet, P. C. Chang, D. C. Huang, J. B. Lee, S. E. Molesa, A. Murphy, D. R. Redinger, S. K. Volkman, *Proc. IEEE* **2005**, *93*, 1330.
[26] Z. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, A. Javey, *Nano Lett.* **2008**, *8*, 20.
[27] M. C. McAlpine, H. Ahmad, D. Wang, J. R. Heath, *Nat. Mater.* **2007**, *6*, 379.
[28] M. Ha, Y. Xia, A. A. Green, W. Zhang, M. J. Renn, C. H. Kim, M. C. Hersam, C. D. Frisbie, *ACS Nano* **2010**, *4*, 4388.
[29] M. Ha, J.-W. T. Seo, P. L. Prabhumirashi, W. Zhang, M. L. Geier, M. J. Renn, C. H. Kim, M. C. Hersam, C. D. Frisbie, *Nano Lett.* **2013**, *13*, 954.
[30] J. Zhao, Y. Gao, W. Gu, C. Wang, J. Lin, Z. Chen, Z. Cui, *J. Mater. Chem.* **2012**, *22*, 20747.
[31] P. H. Lau, K. Takei, C. Wang, Y. Ju, J. Kim, Z. Yu, T. Takahashi, G. Cho, A. Javey, *Nano Lett.* **2013**, *13*, 3864.
[32] J. Noh, M. Jung, K. Jung, G. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, V. Subramanian, G. Cho, *IEEE Electron Device Lett.* **2011**, *32*, 638.
[33] P. Chen, Y. Fu, R. Aminirad, C. Wang, J. Zhang, K. Wang, K. Galatsis, C. Zhou, *Nano Lett.* **2011**, *11*, 5301.
[34] T. N. Jackson, Y.-Y. Lin, D. J. Gundlach, H. Klauk, *IEEE J. Sel. Top. Quantum Electron.* **1998**, *4*, 100.
[35] M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, *IEEE Trans. Electron Devices* **2001**, *48*, 845.
[36] J. Noh, D. Yeom, C. Lim, H. Cha, J. Han, J. Kim, Y. Park, V. Subramanian, G. Cho, *IEEE Trans. Electron. Packag. Manuf.* **2010**, *33*, 275.
[37] PCR Technical, The Pressure Sensitive Electric Conductive Elastomer CS57–7RSC (CSA).

ADVANCED MATERIALS

Supporting Information

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Large-Area Compliant Tactile Sensors Using Printed Carbon Nanotube Active-Matrix Backplanes

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Supporting Information

Large-area, Compliant Tactile Sensors Using Printed Carbon Nanotube Active-matrix Backplanes

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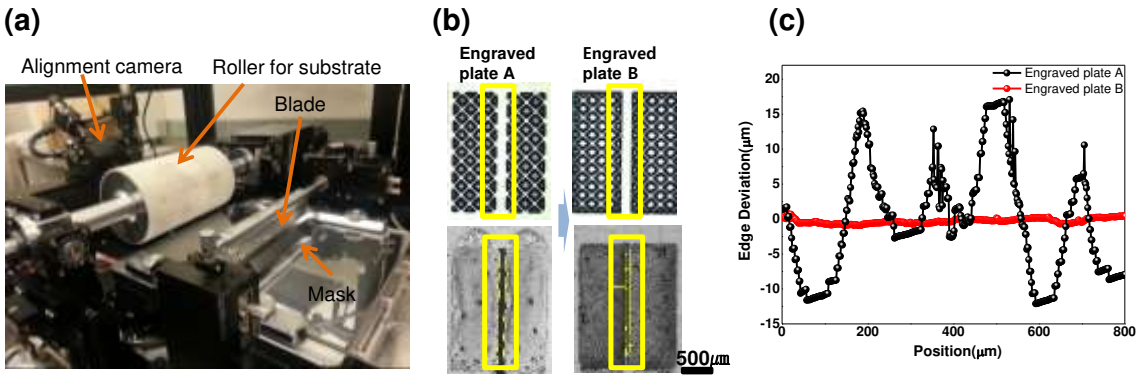

Figure S1: Design of the gravure engraved plates. a) Optical images of an engraved plate design with non-contiguous line edge (top left) and the engraved plate used in this paper with a continuous line edge (top right) along with images of the respective patterns printed onto the PET substrate. b) Line edge roughness of the printed patterns from the two engraved plates extracted from the optical images.

Discussion D1:

Proper design of the gravure engraved plates is critical for minimizing line edge roughness and increasing device yield. The engraved plates consist of halftone wells etched into a chromium plated copper plate. The rheological behavior of the inks during the transfer from the engraved plate onto the substrate is affected strongly by the design of the halftone patterning. When using a pattern with a noncontiguous line edge, the printed ink can spread out from the sides of the engraved plate into the unpatterned areas, causing severe line edge roughness of over ten microns. However, by implementing a continuous line edge into the engraved plate pattern, the inks are unable to spread easily, allowing the line edge roughness to be contained to within one or two microns.

Table T1: Ink formulations, print speeds, pressure, and annealing conditions used for the various printed layers of the active matrix backplane.

Layer	Ink Formulation	Print Speed (mm/s)	Printing Force (kg)	Annealing Conditions
S/D	PG-007AA	100	5	150 °C for 30 sec
First BTO Layer	PD-100:Butyl Carbitol (10:8)	50	8	150 °C for 60 sec
Second BTO	PD-100:Butyl Carbitol (5:1)	50	8	150 °C for 60 sec
Third BTO	PD-100:Butyl Carbitol (10:8)	50	8	150 °C for 60 sec
Gate	PG-007AA:Ethylene Glycol (10:1)	50	10	150 °C for 1 hour

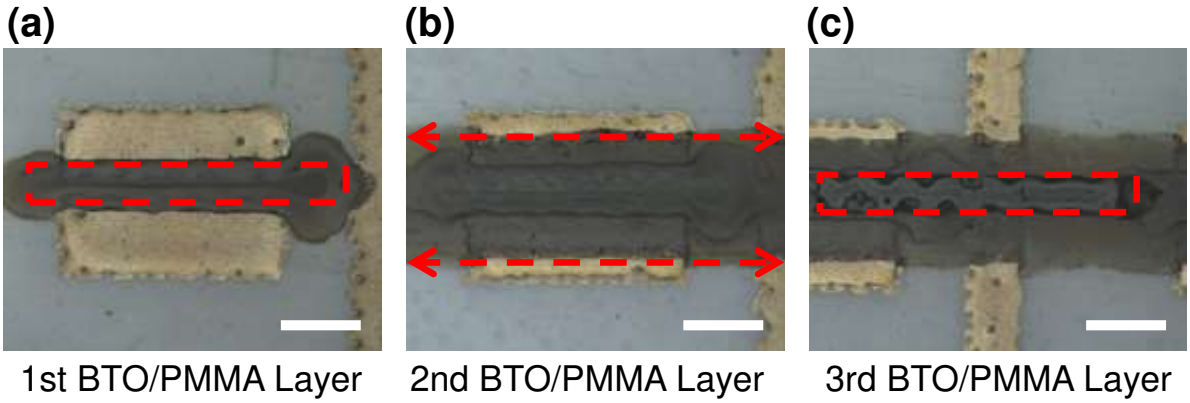

Figure S2: Optical microscope images of a pixel after printing of the a) first, b) second, and c) third BTO layers. Scale bars are all 500 µm. First, a thin BTO layer is put between the S/D area (red box in Fig. S2a). After etching the SWCNTs, the second BTO layer cover whole row along the S/D electrodes (indicated with arrows in Fig. S2b) and the third BTO layer is printed over the gate line (red box in Fig. S2c).

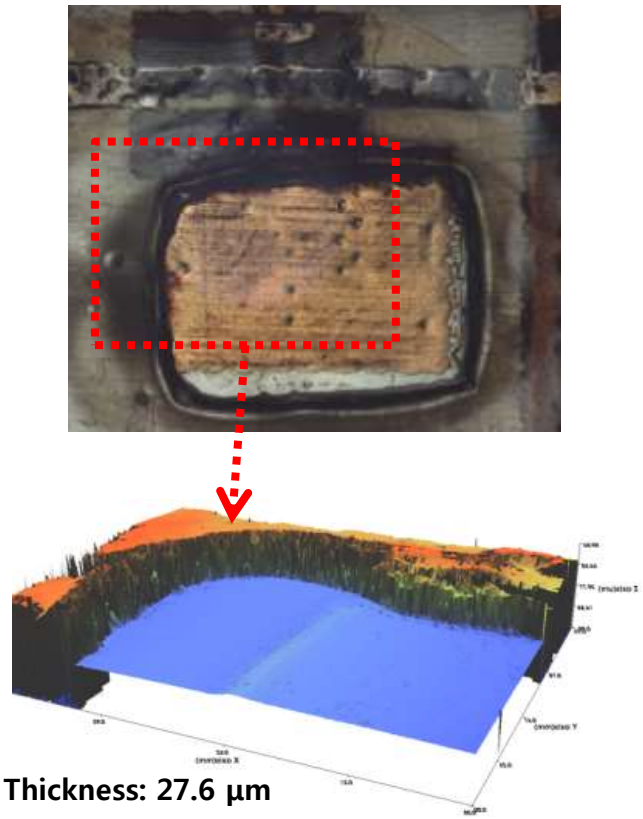

Figure S3: Optical image of a via through the polystyrene layer (top) and a profilometer measurement of the via (bottom) shown to be 27.6 µm.