Review

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Large-area metasurface on CMOS-compatible fabrication platform: driving flat optics from lab to fab

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Abstract: A metasurface is a layer of subwavelength-scale nanostructures that can be used to design functional devices in ultrathin form. Various metasurface-based optical devices – coined as flat optics devices – have been realized with distinction performances in research laboratories using electron beam lithography. To make such devices mass producible at low cost, metasurfaces over a large area have also been defined with lithography steppers and scanners, which are commonly used in semiconductor foundries. This work reviews the metasurface process platforms and functional devices fabricated using complementary metal-oxide-semiconductor-compatible mass manufacturing technologies. Taking both fine critical dimension and mass production into account, the platforms developed at the Institute of Microelectronics (IME), A*STAR using advanced 12-inch immersion lithography have been presented with details, including process flow and demonstrated optical functionalities. These developed platforms aim to drive the flat optics from lab to fab.

Keywords: large area; metasurface; flat optics; lithography.

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1 Introduction

In recent years, metasurface has become one of the fastest expanding areas in nanophotonics [1–3]. It is made from subwavelength-scale unit cell (metaelement) that can precisely control the phase shift of the optical wave from 0 to 2π. By designing the spatial distribution of metaelements, the wavefront can be shaped by the metasurface to achieve various optical functionalities, including focusing [4–9], polarization control [10–13], surface plasmon polariton manipulation [14, 15], spectral filtering [16–18], optical vortex handling [19–23], beam deflection [24–27], and hologram generation [28–36]. Most metasurface-based devices are patterned using either electron beam lithography (EBL) or focused ion beam (FIB). For the patterning of nanostructures in large scale, EBL and FIB need long processing time and hence are not suitable for mass production. In comparison, photolithography and nanoimprint technologies are able to pattern large-scale nanostructures in short time. They are the most promising candidates to move the flat optics from lab to fab in the future [37]. Nanoimprint lithography technology patterns the nanostructure by creating mechanical deformation on either metasurface layer [38] or imprint resist [39] or transferring the pattern onto the substrate as an etching mask [40]. Although the feasibility of nanoimprint lithography for mass production is demonstrated, due to the contact mode of nanoimprinting, there still are concerns about defects, throughput, and template wear.

Meanwhile, photolithography uses light to transfer a geometric pattern from a photomask to a photoresist on the substrate, which has advantages in terms of consistency and throughput. Photolithography is currently used as a part of the standard complementary metal-oxide-semiconductor (CMOS) fabrication process in the microelectronics industry. In addition, it has also been used for the fabrication of microelectromechanical system (MEMS)-based devices [41, 42] and photonics devices [43, 44]. To achieve higher fabrication resolution and smaller critical dimension

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(CD) for photonics devices, especially for near-infrared (IR) and visible wavelength range, 193 nm deep ultraviolet (UV) immersion photolithography can be used to pattern nanostructures. Benefitting from this technology, a number of photonics devices have been demonstrated for various applications, including communications [45–47], nonlinear optics [48–50], signal generation [51–55] and synthesis [56–58], and light detection and ranging [59–61]. Recently, it has also been used to fabricate metasurface devices in large scale, demonstrating metasurface-based devices with various functionalities [62–67]. Photolithography, as a mature technology in semiconductor manufacturing, is one of the most suitable technologies for the high yield mass production of large-area metasurfaces [68].

In this review, we summarized the most recent metasurface work using the CMOS-compatible photolithography technique to pattern large-area nanostructures. These metasurface-based functional devices are fabricated on either silicon (Si) or glass substrate, as presented in Section 2. The overall metasurface-based devices patterned by CMOS-compatible photolithography technology is presented in Table 1, which summarizes the works based on the fabrication approach and includes material, functionality, lithography tool, working wavelength, etc. Next, in Section 2.1, the pioneer works on metasurface-based devices patterned by stepper are reviewed, with the fabrication steps and device performances presented. These works are using either 365 or 248 nm light source for lithography and patterned on 4-inch Si or glass wafer substrate. In comparison, in Section 2.2, the metasurface works patterned using more advanced 193 nm immersion scanner on 12-inch wafers are reviewed, with the fabrication processes and device performances also presented. Such technology enables smaller fabrication CD and larger fabrication scale. These works are based on the Institute of Microelectronics (IME) in-house-developed fabrication processes for metasurface devices. Last but not least, in Section 3, a summary of the work is presented, and the future outlook to drive flat optics from lab to fab is provided.

2 Metasurface-based functional devices patterned by photolithography

Overall functional devices patterned using photolithography have been summarized in this section. The functional devices include lens, spectral filter, polarization bandpass filter (PBF), wave plate, and beam deflector. By choosing the proper materials for metasurface layer and substrate, different working wavelengths have been achieved, covering from visible up to mid-IR.

The most straightforward way of patterning metasurface layer is through direct etching on crystalline Si (c-Si) wafer. PBF and half-wave plate (HWP) have been demonstrated on this platform, working in transmission mode at near-IR wavelength [63, 69], with nanostructures patterned using immersion lithography. The pillar height after etching has achieved 1700 nm in [69], which is enough to achieve 2π phase shift to design lens and many other metasurface-based optical components in the visible and near-IR wavelength regime. Also, metalens and microlens array working in mid-IR (10.6 μm) have been demonstrated through standard single-step UV photolithography followed by direct etching on c-Si wafer [70, 71].

Meanwhile, by depositing and patterning an amorphous Si (a-Si) layer on a dielectric layer or glass wafer, the refractive index contrast can be increased; hence, the etching depth can be reduced. Based on such platform, spectral filter and lens have been demonstrated on either Si or glass wafer substrate [62, 64, 67, 73]. A pillar height of 600 nm is enough to achieve 2π phase shift for a-Si on SiO_2 at 1550 nm wavelength [73]. It is worth to mention that a tunable metalens working at 1550 nm has been demonstrated on transparent stretchable electrodes [72]. Furthermore, the tuning of metalenses at both visible and near-IR wavelength regime have also been achieved by adjusting the relative position of two metalenses, whose metasurface layer is patterned on either Si or quartz substrate using a 365 nm stepper [76].

To make metasurface-based devices work in the visible wavelength regime with high transmission, the transparent glass substrate is expected. Color filter and metalens have also been demonstrated on glass wafer through either layer transfer process from Si wafer [66] or direct patterning on glass [74, 75]. The nanostructures in [75] are patterned using a 248 nm stepper on a 4-inch glass wafer. Further, the patterning in [66, 74] is done by a 193 nm immersion scanner on a 12-inch wafer, which enables smaller CD and closer to the industrial large-scale standard. More fabrication details about the above-mentioned works will be discussed in the following sections.

Metallic nanostructures patterned by photolithography have also been used as a metasurface layer to demonstrate a metalens working at mid-IR wavelength regime [77, 81]. The metalens in [77] works at 4.6 μm in reflection mode, which has been mounted on motorized rotation and translation stage to achieve angular and translational scan of the focal spot. In addition, the mid-IR metalens can also be attached to an MEMS stage to achieve scanning functionality [78]. Furthermore, the metallic layer

Table 1: Summary of metasurface-based devices patterned using photolithography.

Fabrication approach	Materials		Functional devices	Photolithography tool	Metaelement structure; minimum feature size[a]; thickness	Wavelength	Reference (year)
	Metasurface	Substrate					
Direct etching on Si wafer	c-Si	Si wafer	PBF	193 nm immersion scanner	Pillar; 156 nm; 750 nm	Near-IR (1310 and 1610 nm)	[63] (2019)
			HWP		Pillar; 180 nm; 1700 nm	Near-IR (1700 nm)	[69] (2019)
			Lens Microlens array	N.A. (UV lithography)	Pillar; 1500 nm; 6800 nm	Mid-IR (10,600 nm)	[70] (2018) [71] (2019)
Patterning on top of the dielectric layer	a-Si	SiN on Si wafer	Spectral filter for color display	193 nm immersion scanner	Pillar; 70 nm; 130 nm	Visible (400–800 nm)	[62] (2018)
		SiO_2 on Si wafer	Lens		Pillar; 100 nm; 850 nm	Near-IR (1550 nm)	[64] (2019)
Layer transfer onto glass wafer		Glass wafer	Beam deflector array		Pillar; 221 nm; 100 nm	Near-IR (940 nm)	[65] (2019)
			Lens		Pillar; 100 nm; 600 nm	Near-IR (940 nm)	[67] (2019)
			Spectral filter		Pillar; 130 nm; 400 nm	Visible (400–800 nm)	[66] (2019)
Layer transfer onto stretchable electrodes		Carbon nanotube (stretchable electrodes)	Lens	365 nm stepper	Pillar; 810 nm; 950 nm	Near-IR (1550 nm)	[72] (2018)
Patterning on glass wafer	a-Si	Glass wafer	Lens	365 nm stepper	Pillar; 830 nm; 600 nm	Near-IR (1550 nm)	[73] (2018)
				193 nm immersion scanner	Pillar; 100 nm; 400 nm	Near-IR (940 nm)	[74] (2020)
	SiO_2			248 nm stepper	Tapered pillar; 250 nm; 1500 nm	Visible (400–700 nm)	[75] (2019)
Patterning on Si or glass wafer	SiN	Si and quartz substrates	Lens	365 nm stepper	Pillar; 500 nm; 1500 nm	Visible (633 nm); near-IR (1550 nm)	[76] (2018)
Patterning on glass wafer or SiO_2 layer	Au	SiO_2 on Au film and glass wafer	Lens	365 nm stepper	Disc; 800 nm; 50 nm	Mid-IR (4600 nm)	[77] (2016)
		SiO_2 on Au film and Si membrane					[78] (2018)
Patterning of W on SiO_2	W	SiO_2 on W and glass substrate	Thermal emitter		Disc; 350 nm; 50 nm	Visible to mid-IR (600–2000 nm)	[79] (2019)
Lift-off process	Au and insulator (Si/SiO_2)	Si substrate	Thermal emitter and absorber		Disc; 550 nm; 50 nm	Mid-IR	[80] (2019)

[a]Minimum feature size refers to the smallest pillar/disc diameter or dimension in the designed device.

has been patterned to form metasurface for thermal emitter or absorber with wavelength selectivity in near-IR and mid-IR [79, 80, 82].

The recent works of metasurface-based functional devices using photolithography technology for large area patterning are listed in Table 1. They are categorized based on the fabrication approach, materials, functionality, photolithography tools, metaelement structure, and working wavelength. These works are demonstrated in the past 5 years, which indicates the maturity of the metasurface technology and the trend to move from laboratory to mass manufacturing.

2.1 Metasurface patterned by photolithographic stepper

In this section, the metasurface work patterned using stepper is summarized and presented from the fabrication process and the device functionality perspectives. The stepper with 365 nm light source has been used to pattern and demonstrate the metasurface working at near-IR [72, 73] and mid-IR [77, 78] wavelength. Also, the stepper with 248 nm light source has been used to fabricate metalens working in the visible wavelength regime [75].

The fabrication process flow of the large-area metalens (2 cm diameter) working at 1550 nm is shown in Figure 1A [73]. A stepper (GCA AS200 i-line 365 nm stepper) is used to pattern the a-Si layer grown through plasma-enhanced chemical vapor deposition (PECVD) on a 4-inch glass substrate. The 600-nm-high nanopillars are formed through the reactive ion etching process. The fabricated metalens and the zoomed-in scanning electron microscopy (SEM) image of the etched nanopillars (with scale bar of 2 μm) are also presented in Figure 1A. The fabricated metalens demonstrates diffraction-limited focusing at 1550 nm communication wavelength, with the intensity distribution at the focal plane illustrated in Figure 1B (left). In addition, the measured modulation transfer function (MTF) together with the theoretical diffraction-limited MTF are plotted in Figure 1B (right) for comparison. The focusing efficiency of the metalens is reported to be 91.8 ± 4.1% at 1550 nm working wavelength, which is based on the measured power ratio with and without the metalens. In [73], high-quality images (Figure 1C) are also obtained using the fabricated metalens, showing the clear image of the Harvard logo and U.S. Air Force (USAF) 1951 resolution chart.

In addition, an electrically tunable a-Si-based metalens with 6 mm diameter working at the same wavelength has been patterned on the Si wafer using the same stepper model [72]. The fabrication process flow is illustrated in Figure 1D. The a-Si metasurface layer is grown on top of a sacrificial layer GeO_2 (step I). After the patterning of the a-Si layer, the device is attached to an elastomer layer and then immersed into a water bath (step II). The false-colored SEM image of the patterned a-Si pillars at the center of the metalens before attaching to the elastomer layer is shown in Figure 1E (top). The straight pillar shape and smooth side wall indicate the good quality of the patterning and etching process. The GeO_2 layer is later dissolved in water (step III); then, the patterned a-Si layer can be transferred onto the elastomer layer to achieve adaptive functionality in terms of focal length, astigmatism, and shift (step IV). The schematic of the functional adaptive metalens with stretchable electrodes on the elastomer layer is also included in Figure 1E (bottom). The tuning of the focal length is demonstrated in Figure 1F (left). It presents the focusing intensity along the z-direction under different electrical voltages applied for tuning. The intensity distributions at the focal plane under two voltages are also presented in Figure 1F (middle). The diffraction-limited focusing has been proven by comparing the MTF from measurement and theoretical diffraction limit as shown in Figure 1F (right). The focal length and the stretch with respect to the applied voltage are shown in Figure 1G. Besides the focal length, the astigmatism control and image shift correction have also been demonstrated through adding electrical voltage [72].

The mid-IR metallic metalens demonstrated on either glass or Si-on-insulator (SOI) substrate are patterned using the same i-line 365 nm stepper [77, 78]. Figure 2A shows the fabrication process based on SOI wafer, which enables the formation of the membrane for later MEMS scanner integration. A layer of Si_3N_4 and SiO_2 is deposited via PECVD process on top and bottom of the SOI wafer, respectively (step I), followed by the patterning of the bottom SiO_2 layer to produce back-side etching window (step II). Then, the top Si_3N_4 layer is removed, and a gold (Au) layer is deposited via electron beam evaporation (EBE) followed by SiO_2 layer deposition via PECVD (steps III and IV). The bilayer photoresist (LOR3A + SPR700) is exposed using a stepper (step V). At last, the Au layer is deposited via EBE followed by a lift-off process to remove the photoresist layer to form the metasurface layer with a nanodisk structure. The diameter of the nanodisk varies from 0.8 to 2 μm, and they have either a fixed pitch size of 2.5 μm [77] or a fixed edge-to-edge gap of 0.5 μm [78].

The metaelement unit cell is presented in Figure 2B (left), with bottom Au as a reflecting layer. The SEM image of the patterned Au antenna is illustrated in Figure 2B (right). An additional back-side etching process is applied on the Si substrate to form a 2.8-μm-thick membrane, with the cross-section shown in Figure 2C (left). The schematic of the fabricated metalens is illustrated in Figure 2C (right), demonstrating the functionality of the metalens device. This metalens is later cut using the needle from FIB tool and attached onto a MEMS scanner to achieve tuning purpose. The process is recorded and illustrated in Figure 2D (left). An optical microscopy image of the metalens on

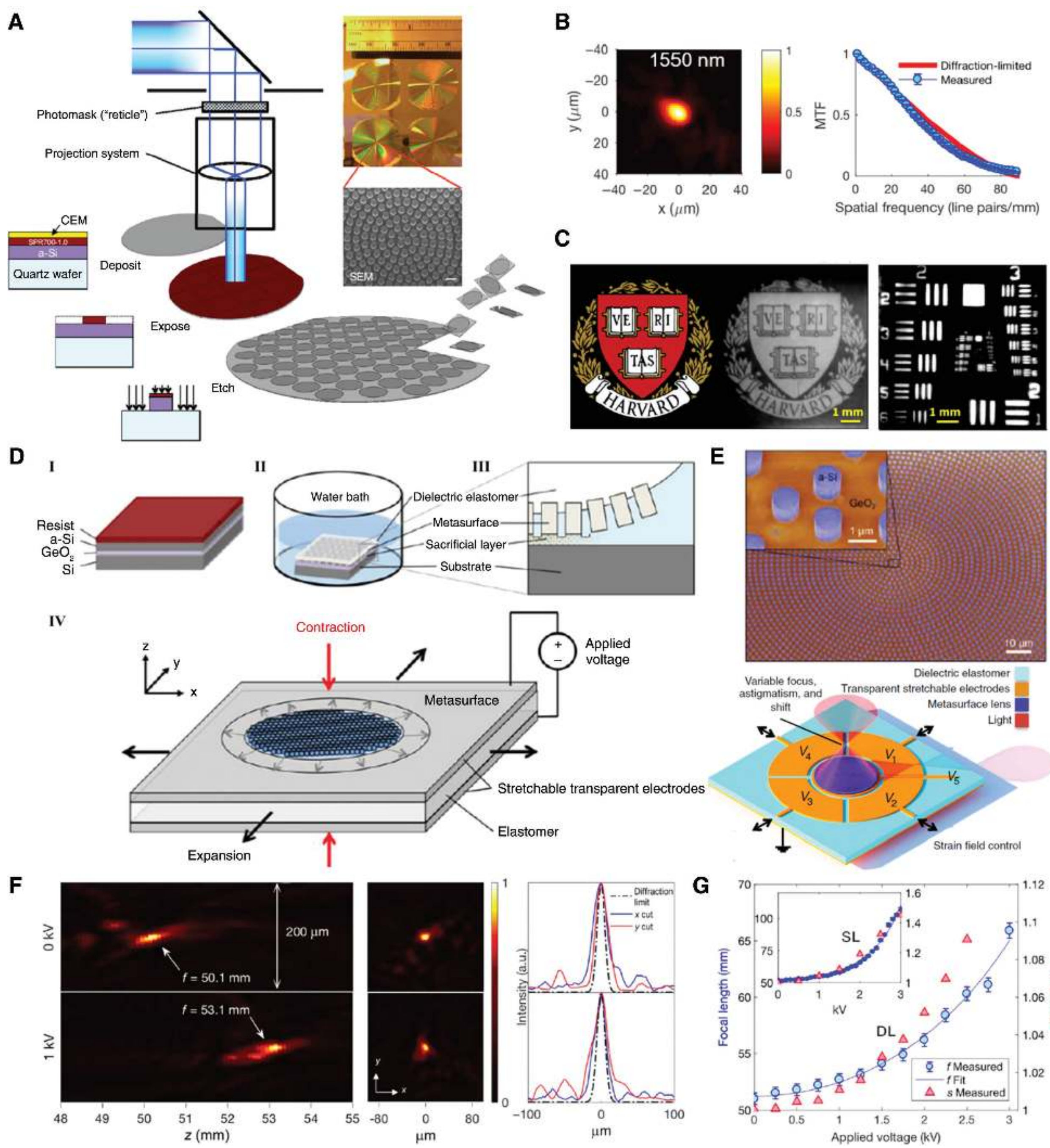

Figure 1: Metasurface-based devices working in near-IR patterned using a stepper with 365 nm light source.
(A) Schematic of the fabrication process for large-area metalens working at 1550 nm, including a fabricated metalens and an SEM image of the patterned nanopillars at the metalens center. (B) Focal spot at 1550 nm (left) and plot of the measured MTF together with the theoretical diffraction-limited MTF for comparison (right). (C) Harvard logo and USAF 1951 resolution chart formed by the metalens at 1550 nm. (A–C) Adapted with permission from [73]. © The Optical Society. (D) Fabrication process flow for the adaptive metalens, including the layer transfer process on the elastomer layer using a sacrificial layer GeO_2. (E) False-colored SEM image of the patterned nanopillars on GeO_2 layer (top) and schematic of the functional adaptive metalens showing metasurface lens attached to the elastomer and contacted through a stretchable electrode layer (bottom). (F) Focusing intensity along the *z*-direction under two different applied voltages (left), focusing spot intensity distribution at focal plane (middle), and intensity profile along the focal plane in compare with the theoretical diffraction-limited intensity profile (right). (G) Tuning of the focal length and stretch with respect to the applied voltage. (D–G) Adapted with permission from [72].

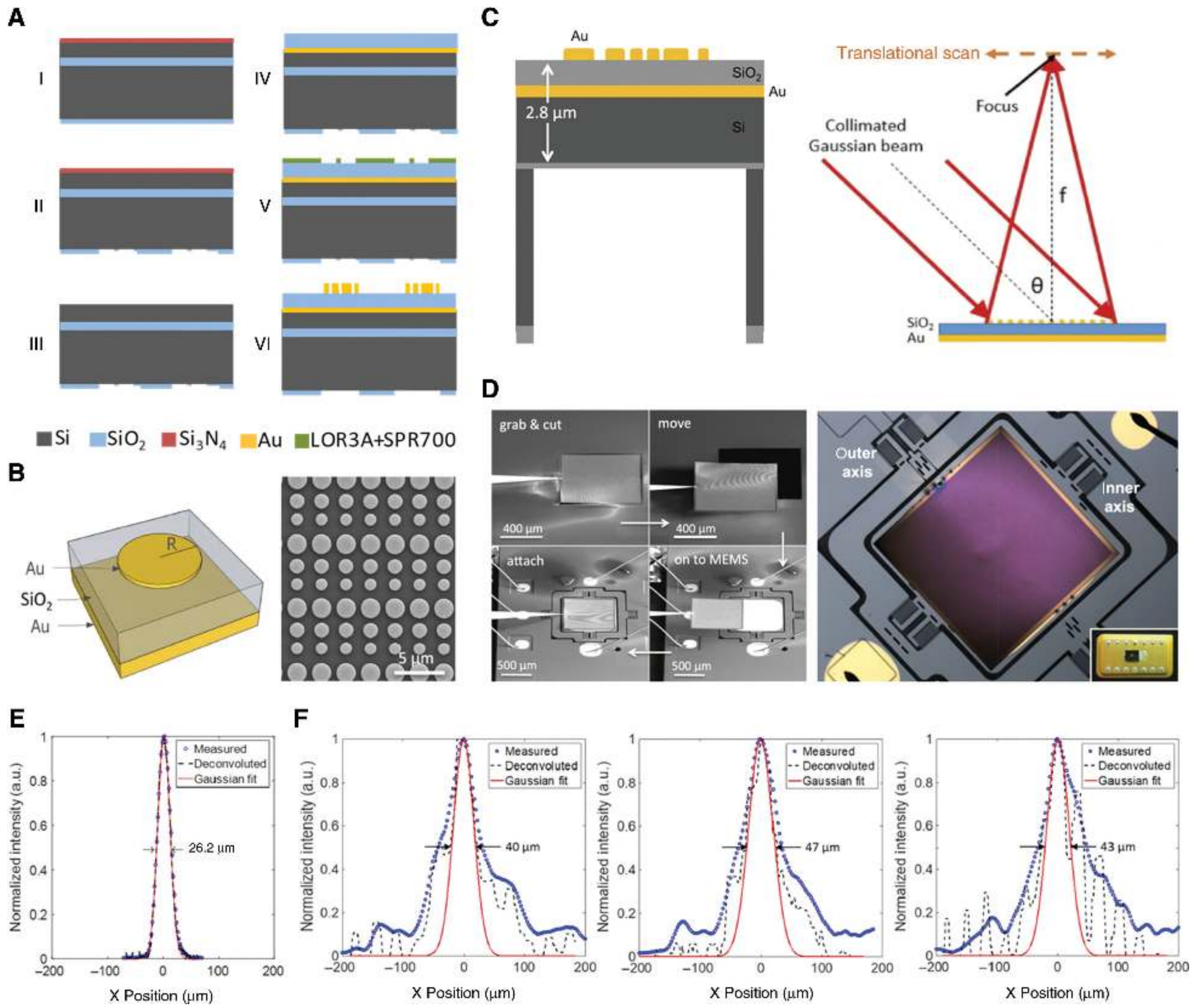

Figure 2: Metasurface-based devices working in mid-IR patterned using a stepper with 365 nm light source.
(A) Fabrication process flow of the metallic metalens on Si wafer. The back-etch window is opened by patterning the SiO_2 layer from the bottom of the Si wafer. Then, two Au layers are grown on the substrate with a layer of SiO_2 in between. The bottom Au layer acts as a reflection layer, and the top Au layer is patterned as a metasurface layer. (B) Schematic of metasurface unit cell (left) and top-view SEM image of the patterned Au nanodisk (right). (C) Schematic of the cross-section of the fabricated metalens on Si membrane after back-side etching of the substrate (left) and schematic of the functional metasurface (right). (D) Steps to integrate the metalens from membrane onto the MEMS for tuning (left) and microscopy image of the metalens on MEMS stage, with two rotational axis indicated (right). (E) Translational scan measurement of the reflected laser beam at the focal line center. (F) Translational scan measurement of the reflected laser beam at the focal line center with MEMS rotation angles of 0°, 1°, and 2.5° (left, middle, and right, respectively). (A–F) Adapted with permission from [78]. Licensed under a Creative Commons Attribution.

the MEMS stage is also presented in Figure 2D (right), with two moving axes indicated. The focusing effect of the metalens without tuning is illustrated in Figure 2E, showing the normalized reflected beam intensity at the center of the focal line. The full-width half-maximum (FWHM) is measured to be 26.2 μm, which is close to the designed value. Under the rotational tuning of the MEMS stage with angles of 0°, 1°, and 2.5°, the normalized reflected beam intensity at the focal line center are presented in Figure 2F (left, middle, and right, respectively). The corresponding FWHM of the profile are reported to be 40, 47, and 43 nm, respectively. The system demonstrates the 2D scanning along two orthogonal axes with ±9° angle, which enables the dynamic beam steering capability.

For the metasurface working in the visible wavelength range, a smaller patterning CD is required compare with the device working in the IR wavelength range. Therefore, a stepper with 248 nm source wavelength has been used to pattern the tapered nanopillars directly on 4-inch glass wafer [75]. SiO_2 pillars have a diameter range from 250 to 600 nm and a fixed edge-to-edge gap of 250 nm. The fabrication process flow is shown in Figure 3A. The Cr layer on glass substrate is dry etched using Cl_2 gas with the patterned photoresist at the top as etch mask. After stripping the photoresist, the glass wafer is then dry etched using fluoride gas with the patterned Cr as etch mask. Until the height of the glass pillar reaches 2 µm, the Cr layer is then removed using Cl_2 gas, leaving SiO_2 pillars on the substrate.

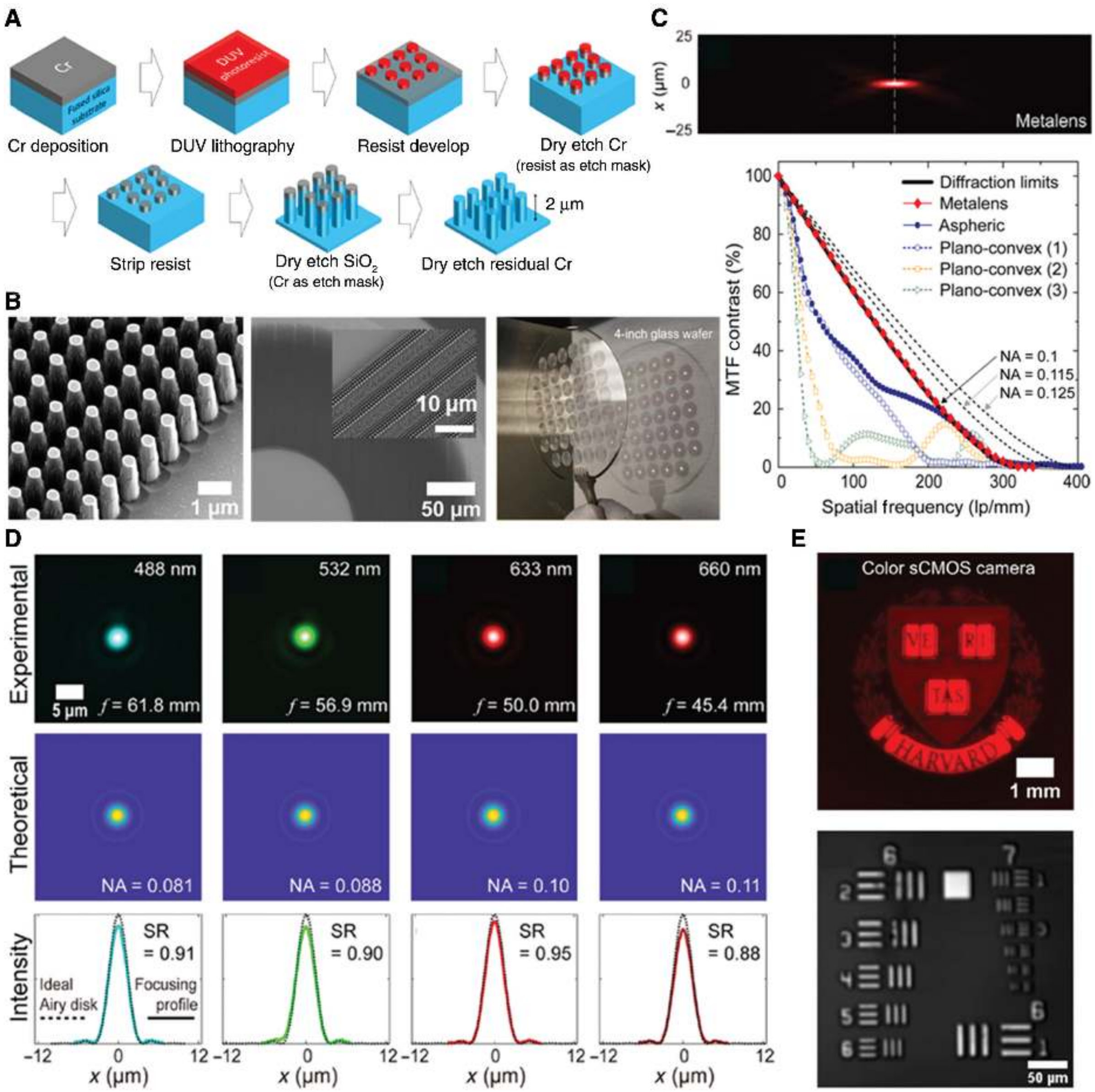

Figure 3: Metasurface-based devices working in visible patterned using a stepper with 248 nm light source.
(A) Fabrication process flow of the metalens through direct etching on glass wafer. A Cr layer is first patterned using photoresist as etch mask. The patterned Cr layer is then used as etch mask for the glass nanopillars through dry etch. (B) Tilted-view SEM image of nanopillars with 2 µm height (left), top-view SEM image of the metalens near the central area, with inset showing the nanopillars at the edge of the metalens (middle), and fabricated 4-inch glass wafer containing 45 metalens showing the focusing of the incident light in the visible wavelength range (right). (C) Intensity distribution along the *z*-direction measured at 633 nm wavelength (top) and comparison among the measured and idea MTFs for the lenses (bottom). (D) Measured intensity distribution at the focal plane under different wavelength in the visible wavelength regime (top row), theoretical intensity distribution at the focal plane (middle row), and measured intensity profile (solid line) in comparison to ideal intensity profile (dotted line) at the focal plane, showing SR values of 0.91, 0.90, 0.95, and 0.88, respectively (bottom row). (E) Colored Harvard logo obtained near the focal plane of the metalens by an sCMOS camera (top) and image of USAF resolution chart obtained using the metalens within a reflective scanning microscopy system (bottom). (A–E) Adapted with permission from [75]. © 2019 American Chemical Society.

Figure 3B (left) shows the tilted SEM image of the patterned nanopillars. Figure 3B (middle) shows the top view of the SEM image of the nanopillars near the center area of the metalens, with the inset illustrating the nanopillars near the edge of the metalens. Figure 3B (right) shows a fabricated glass wafer containing 45 metalens and the focusing of incident light from the metalens with a diameter of 1 cm.

The metalens has been characterized after the fabrication. The diffraction-limited focusing can be illustrated in Figure 3C. Figure 3C (top) shows the intensity distribution along the z-direction at 633 nm wavelength without spherical aberration. The MTF comparison between the measurement at the focal plane and the idea diffraction-limited focusing are presented in Figure 3C (bottom). The MTF of the metalens is very close to the ideal case based on the plot. This is not the case for aspheric lens and planoconvex lens due to the existence of spherical aberration. The focusing efficiency of the designed metalens has been reported to be 45.6% [75]. This number is obtained by taking the ratio of the measured power from the focal spot center to the first peak of the Airy disk and the total incident power. The focal plane intensity distributions at different wavelengths are measured and presented in Figure 3D (top row). The theoretical focal plane intensity distributions at different wavelengths are also included in Figure 3D (middle row). For comparison, the intensity profiles at the focal plane for different wavelengths are plotted together with the idea ones, as shown in Figure 3D (bottom row). The Strehl ratios (SRs) are calculated to be 0.91, 0.90, 0.95, and 0.88 for the wavelength of 488, 532, 633, and 660 nm, respectively. The imaging capability of the metalens has also been reported, as illustrated in Figure 3E. Figure 3E (top) is a direct colored image captured near the focal plane of the metalens by a scientific CMOS (sCMOS) camera. Furthermore, the metalens has also been mounted within a reflective scanning microscopy system, and an image of 1951 USAF resolution chart has been captured as shown in Figure 3E (bottom). Based on MTF results, the resolution line should be able to reach 1.58 μm. The limited image resolution is contributed by the optical components within the experimental setup.

To sum up, the functional devices reviewed in this section are proof of the effectiveness of using photolithography to pattern the metasurface. The devices can be integrated with an MEMS device or a flexible material to achieve tuning. Also, they cover a wide spread of working wavelength range from visible to mid-IR. The fabrications are based on 4-inch Si or glass wafer substrate using a 365 or 248 nm stepper photolithographic tool. To achieve higher pattern resolution and smaller CD on a larger wafer scale, a more advanced 193 nm 12-inch immersion lithography tool has been used and will be presented in the next section. It enables better metasurface device performance and larger fabrication scale.

2.2 Metasurface patterned by immersion scanner

In this section, the fabrication process flows to make metasurface-based devices on 12-inch Si wafer and glass wafer are presented. For the Si substrate, two approaches, including the direct etching on Si wafer and the patterning on top of a dielectric layer, are discussed. For the glass wafer substrate, two approaches, including the layer transfer from Si wafer to glass wafer and the direct patterning on glass wafer, are presented. The process flows have been developed within the IME using the state-of-the-art 193 nm 12-inch immersion scanner, and such technology enables the fabrication of metasurface-based devices with smaller CD and larger volume compared to the work in the previous section. The functional devices demonstrated on the corresponding platforms are also reviewed.

2.2.1 Si substrate

Figure 4A shows the fabrication process of the first approach: direct etching on 12-inch Si wafer. A 193 nm deep UV immersion scanner is used to pattern the photoresist followed by an inductively coupled plasma (ICP) etching process. A fabricated 12-inch Si wafer before dicing is presented in Figure 4B.

Depending on the applications of the metasurface-based device, the metaelements (unit cells for phase shifting) have different designs in terms of shape and dimension. The SEM images of pyramid metaelements fabricated from the direct etching process are shown in Figure 4C, representing the top and 45° tilted views, respectively. Also, the cross-sectional transmission electron microscopy (TEM) image of the pyramid is shown in Figure 4C. The height of the pyramid (h) is about 760 nm. Its top width along the X ($l_{x,\mathrm{top}}$) and Y ($l_{y,\mathrm{top}}$) directions are 163 and 384 nm, respectively. These pyramids are laid out as array with pitch size (p) of 1 μm to form the metasurface-based PBF, which is able to transmit the X-polarized light and reflect the Y-polarized light at 1660 nm. The PBF has another passband at 1360 nm, which can transmit Y-polarized light and reflect X-polarized light. The schematic of the PBF is shown in Figure 4D. The measured wafer-level device performance is illustrated in Figure 4E. Fifteen of 17 selected dies across the wafer have

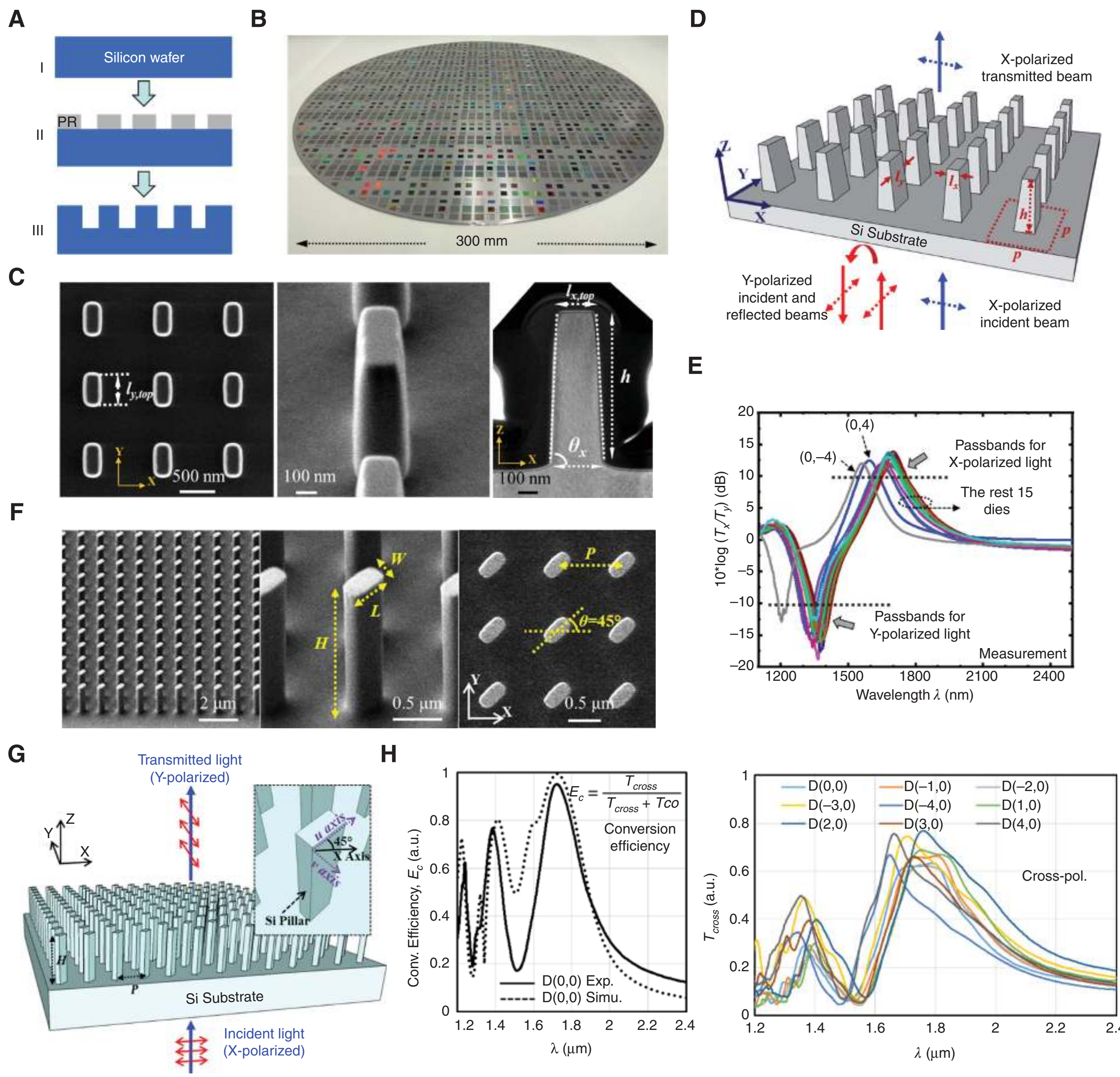

Figure 4: Metasurface-based devices demonstrated using immersion scanner and direct etching on 12-inch Si wafer.
(A) Fabrication process flow. (B) Fabricated 12-inch Si wafer. Adapted with permission from [69]. (C) SEM images of the pyramid nanopillar for PBF showing the top and 45° tilted views, respectively, and TEM image of the pyramid nanopillar showing the cross-sectional view. (D) Schematic of the PBF. (E) Measurement results of PBF selected across the wafer, showing 15 of 17 dies having 10 dB power distinction at designed wavelength. (C–E) Adapted with permission from [63]. © The Optical Society. (F) SEM images of the rectangular nanopillar for HWP, showing the 45° tilted view of pillar array, single pillar, and the top view of the pillar array, respectively. (G) Schematic of HWP. (H) Experimental and simulation results of HWP, showing polarization conversion efficiency (E_c) spectra at the central die and the wafer-level T_{cross}. (F–H) Adapted with permission from [69].

achieved power distinction between two polarizations of more than 10 dB considering two passbands at 1360 and 1660 nm. Hence, the wafer-level device yield is reported to be 82%. It is worth to note that the two dies at wafer locations of (0, 4) and (0, −4) are at the very edge of the wafer. The PBFs on these two dies have different nanopillar geometric dimensions compare with the dies located close to wafer central region. Furthermore, with the 193 nm ArF immersion lithography capability, the PBF feature size and passbands can both be precisely controlled and the working wavelength is extendable to visible range.

Another type of metaelement is shown in Figure 4F. The periodic square-latticed nanopillars have a pitch size (p) of 1000 nm. The height (H), width (W), length (L), and orientation (θ) of the pillar are 1700, 200, and 400 nm and 45°, respectively. The nanopillars with an aspect ratio (height over width) of more than 10:1 are achieved using a dedicated etching process developed at the IME on this platform. These metaelements form the HWP functional device, which is demonstrated using the same fabrication process but different metasurface layer height. Its schematic is shown in Figure 4G. The device performance can be represented by Figure 4H. The polarization conversion efficiency, which is defined in the inset of Figure 4H (left), can achieve 95% at the wavelength near 1.726 μm. The wafer-level device performance uniformity is performed by characterizing nine selected dies across the wafer. The result of cross-polarized transmittance (T_{cross}) is also included in Figure 4H (right). The wafer-level device performance achieves the polarization conversion efficiency of 95.6 ± 0.8%.

The process flow of the second approach is illustrated in Figure 5A. Compare with the first approach of direct

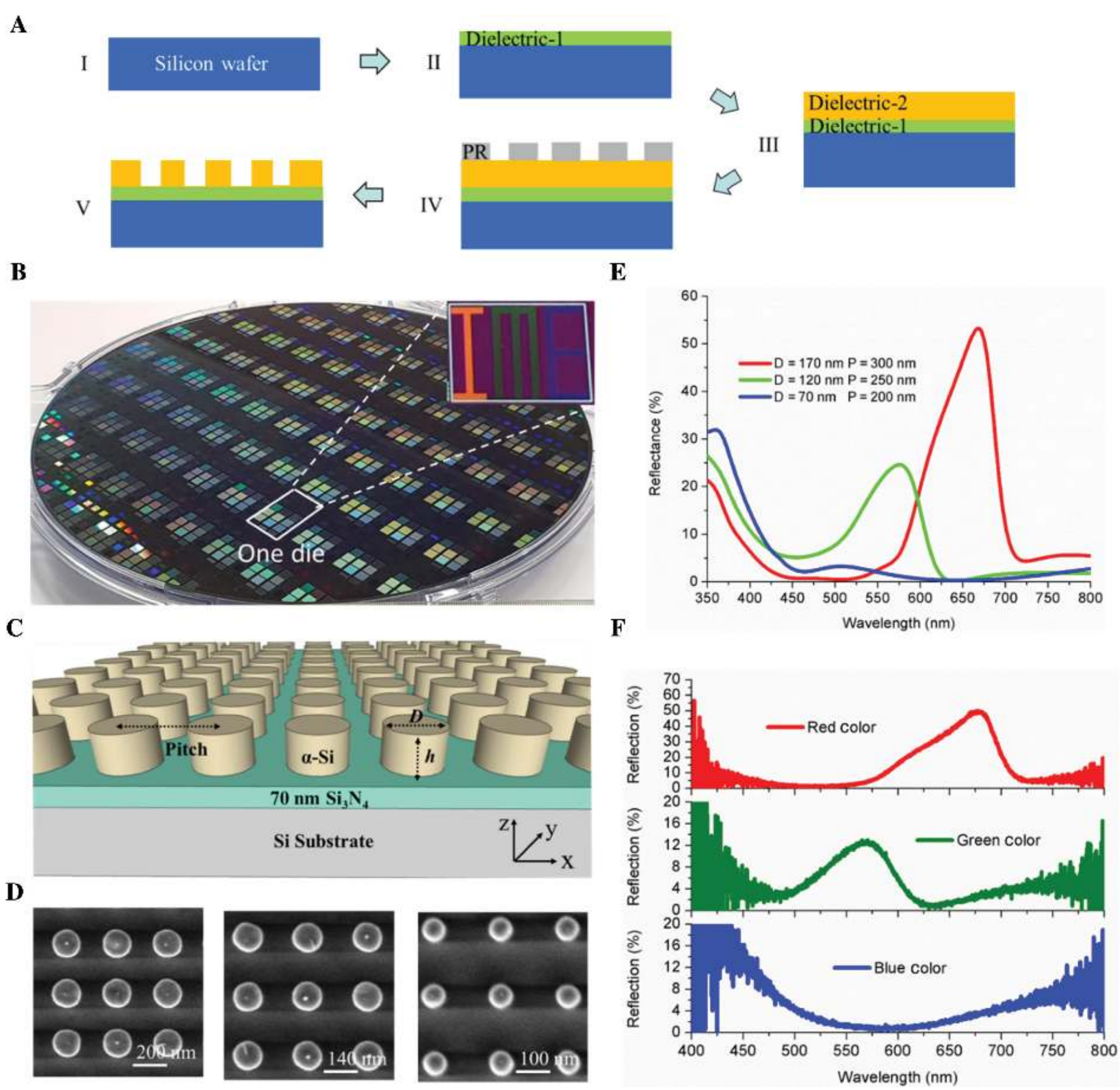

Figure 5: Metasurface-based devices demonstrated using an immersion scanner on 12-inch Si wafer with a dielectric layer on top. (A) Fabrication process flow. (B) Fabricated 12-inch Si wafer, with inset showing the color filtering from the metasurface layer in the visible wavelength range. (C) Schematic of the color display metasurface. (D) Top-view SEM images of the nanopillars patterned with pitch and diameter variations. (E) Design of the color filter, showing the reflection spectra of the nanopillar arrays with diameters of 170, 120, and 70 nm and pitch sizes of 300, 250, and 200 nm, respectively. (F) Measured reflectance spectra from the three letters “I”, “M”, and “E” from the wafer central die. (B–F) Adapted with permission from [62]. © The Optical Society.

etching, the second approach is doing patterning and etching at the top of a dielectric layer (dielectric-1 layer as indicated in Figure 5A). This dielectric layer should have lower refractive index than the dielectric-2 layer. The material for the dielectric-1 layer can be SiO_2, SiN, Al_2O_3, AlN, SiO_2/SiN multilayer, etc., whereas the material for the dielectric-2 layer can be chosen from a-Si, TiO_2, SiN, etc. In this way, the refractive index contrast can be created between the metasurface layer and the substrate layer.

The fabrication starts from Si wafer (step I). The dielelctric-1 and dielectric-2 are deposited by either CVD or physical vapor deposition (PVD) subsequently (steps II and III). The dielectric-2 is then patterned using the immersion photolithography followed by dry etching processes (steps IV and V) to form the nanostructure. One fabricated wafer is presented in Figure 5B, with the inset showing a reflective color filter in the visible wavelength range. The schematic of the metasurface-based color filter is shown in Figure 5C. The 70-nm-thick Si_3N_4 dielectric layer is used below the patterned a-Si nanopillars with a height of 130 nm. The color filtering effect is formed by varying the pillar diameters and pitch size. For letter "I", "M", and "E", the diameters are 170, 120, and 70 nm, respectively, and the pitch sizes are 300, 250, and 200 nm, respectively. The top-view SEM images of the pillars for the three letters are presented in Figure 5D, showing diameters of 166, 120, and 65 nm, respectively. These numbers are in good agreement with the designed values. The simulated and measured reflectance spectra for the three letters are presented in Figure 5E and F, respectively, showing a good match. The wafer-level uniformity of the lithography process has also been investigated in [62], reporting the range (max-min) to be 2.3, 4.5, and 4.1 nm for the three letters, respectively. The 3Sigma values have also been reported as 2.6, 5.3, and 3.5 nm for these three letters, respectively. Furthermore, the maximum CD variation of the nanopillars after ICP etching is reported to be 7.65%. Although the process can be further improved, the reported numbers can prove the effectiveness of 193 nm ArF immersion lithography and ICP etching for metasurface mass production on this platform.

2.2.2 Glass wafer substrate

For metasurface working in wavelengths above 1.1 µm, Si can be used as substrate, as it is transparent in this wavelength range and compatible with the CMOS fabrication platform. When the required working wavelength is shorter, glass/quartz wafer rather than Si wafer is needed due to its transparency in such wavelength range. Meanwhile, making nanostructures directly on glass/quartz substrate might be challenging, as most CMOS fabrication and in-line characterization facilities, e.g. CVD, PVD, photolithography, etching, and SEM, are designed to work on Si wafers. The fabrication and characterization tools need to be modified, and new recipes need to be developed to accommodate the glass/quartz wafer.

Here, we present the process for metasurface devices in wavelengths below 1.1 µm. The approach is to transfer the metasurface layer to a 12-inch glass wafer substrate. The process flow has been developed within the IME and is based on standard CMOS processing tools without any modification.

The developed fabrication process flow to make the metasurface layer on glass wafer substrate is shown in Figure 6A. The fabrication starts from Si wafer and at the beginning shares the same steps as presented in Figure 5A. After the patterning and etching of the top dielectric layer, a layer of transparent bonding glue is spin coated on top with a flat top surface, as shown in steps I and II of Figure 6A. The refractive index of the glue is close to the glass index. Next, the wafer is bonded with a glass wafer (Corning SG3.4), as shown in step III, followed by backside grinding to thin down the Si thickness from 750 to 20 µm. The remaining Si is then removed by wet etch or dry etch (step IV). The dielectric-1 layer acts as an etch stop layer. Using this approach, metalens [67], color filter [66], and pixelated beam deflector array [65] have been demonstrated, proving the concept of transferring the metasurface layer on glass wafer.

Figure 6B shows the photograph of the fabricated 12-inch glass wafer, with a blue Agency for Science, Technology and Research logo as background to illustrate its transparency at the area without patterned nanostructures. The schematic of a metalens demonstrated on this wafer is illustrated in Figure 6C. The top-view and 45° tilted-view SEM images of the nanopillars for this metalens after ICP etching are shown in Figure 6D (top left and top middle, respectively). The pillar height is 600 nm. The straight and smooth sidewall angle of the nanopillars indicates the good quality of the lithography and ICP etching processes. The intensity profile at the focal spot with an Airy function overlaid is shown in Figure 6D (top right). The spot size (FWHM) can be obtained as 1.26 µm. The metalens has been applied for imaging. Figure 6D (bottom left) shows the image of a standard 1951 USAF resolution chart. The line width of 2.19 µm in this chart has been resolved. Furthermore, the metalens is used for fingerprint imaging. By taking the multiple shots at different lens locations and combining the images, the proof-of-concept demonstration of high-quality fingerprint

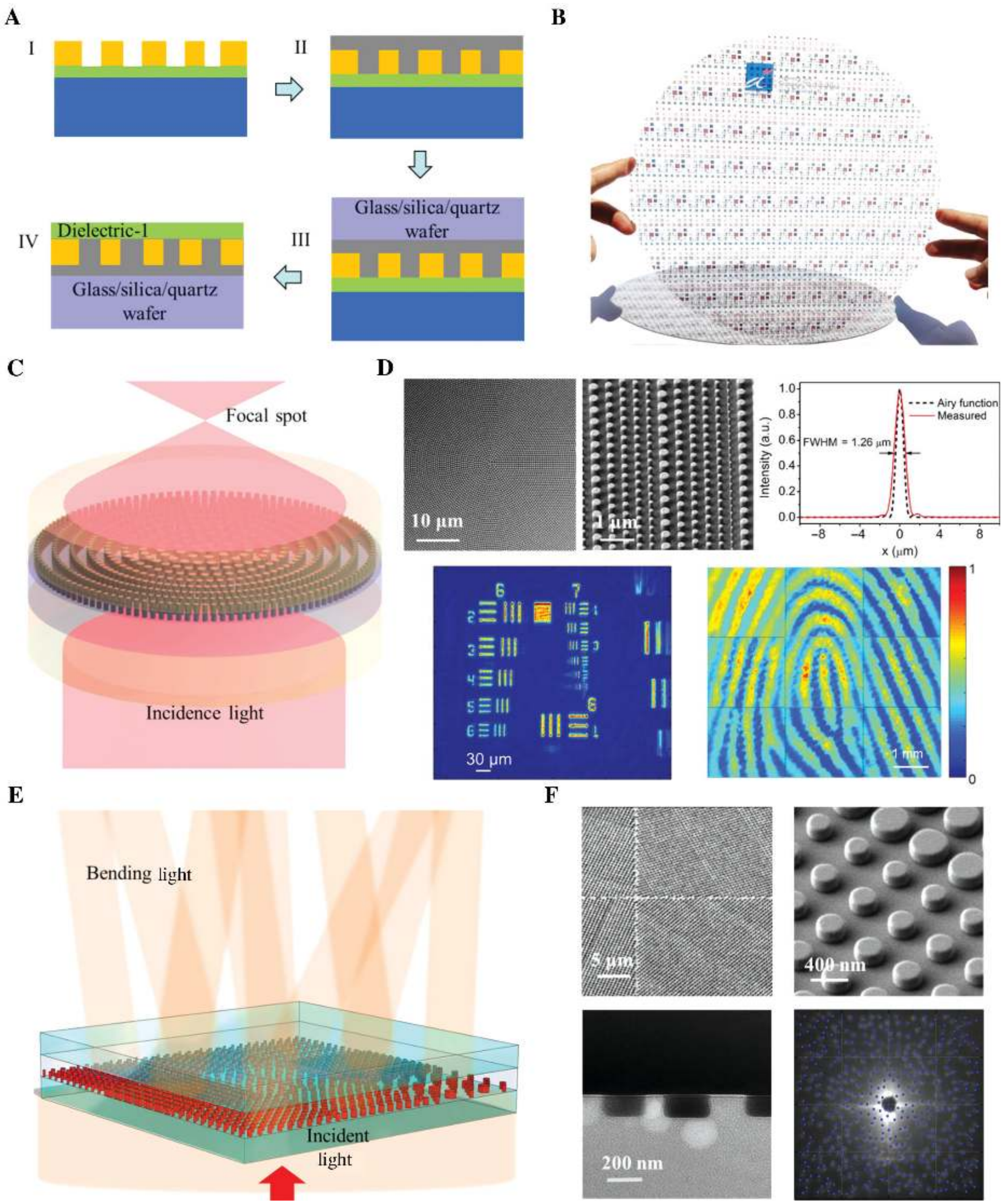

Figure 6: Metasurface-based devices demonstrated on 12-inch glass wafer using immersion scanner and layer transfer process. (A) Fabrication process flow to transfer metasurface layer on glass wafer. (B) Fabricated 12-inch glass wafer. (C) Schematic of metalens on 12-inch glass wafer. (D) Top-view (top left) and projected zoomed-in view (top middle) SEM images of the nanopillars with a height of 600 nm designed for metalens; intensity profile at the focal spot with an Airy function overlaid (top right); optical image of the 1951 USAF resolution chart formed using the metalens (bottom left); and fingerprint image formed using the metalens, proving the concept of metalens array for better imaging quality and compact system (bottom right). (B–D) Adapted with permission from [67]. (E) Schematic of pixelated deflector array on 12-inch glass wafer. (F) Projected-view SEM image of the pixelated deflector array showing the boundary between the pixels clearly (top left); projected zoomed-in view SEM image of the nanopillars for deflector array, with a pillar height of 100 nm (top right); TEM image of the nanopillar embedded in bonding glue (bottom left); and random spots (white dots) generated by the deflector array overlapping with the design (blue spots), showing a good match (bottom right). (E and F) Reprinted with permission from [65].

imaging with compact system size is reported, as shown in Figure 6D (bottom right). More experimental and characterization details can be found in [67].

The advantage of this platform is to pattern the large-area metasurface. Therefore, one more functional device demonstrated on this platform is a large-area pixelated beam deflector array to generate random points. Its functionality is illustrated in the schematic as shown in Figure 6E. The projected-view SEM image of the patterned nanopillars is shown in Figure 6F (top left), from which the boundary between each deflector pixel can be clearly observed. The zoomed-in view SEM image of the nanopillars with a height of 100 nm is also presented in Figure 6F (top right). The cross-sectional view of the nanopillars is illustrated in the TEM image as shown in Figure 6F (bottom left). The beam deflector array with 21×21 pixels and a dimension of 2.5×2.5 mm is demonstrated as a proof-of-concept [65]. The spot array generated at 940 nm wavelength is projected on the screen and captured by an IR camera, as illustrated as white spots in Figure 6F (bottom right). The blue spots overlapping with the white spots are the design of the random points. A good match can be found through the comparison between the design and the experiment.

The layer transfer process mentioned earlier requires the bonding glue, which has a refractive index close to glass and hence limits the refractive index contrast between nanopillars and the surrounding material. To increase the index contrast and also reduce the fabrication steps, patterning and etching directly on 12-inch glass wafer have been developed with functional devices demonstrated. The fabrication process flow is summarized and presented in Figure 7A. Starting from the glass wafer (Corning HPFS7980), as shown in step I, an opaque layer is deposited at the bottom of the glass wafer to make it nontransparent and hence detectable by the sensors of the fabrication tools. A layer of a-Si with a thickness of 400 nm is then deposited at the top of the glass wafer as metasurface layer, as shown in step II. Next, an opaque layer is deposited at the top surface for the immersion lithography process, which is later used to pattern the photoresist (step III). Lastly, the etching process is applied to the wafer to form the nanostructures for metasurface followed by the removal of the opaque layers at the top and bottom of the glass wafer (step IV).

A photograph of the fabricated 12-inch glass wafer through direct etching is shown in Figure 7B. On this wafer, functional devices, including large-area metalens [74], metalens array [83], and pixelated beam deflector array [84], have been reported. As a proof-of-concept demonstration, the large-area metalens is designed with a diameter of 8 mm. Its schematic drawing together with the single pillar on glass wafer substrate is presented in Figure 7C (left). The top-view SEM images near the fabricated metalens central region and the zoom-in view at the central region are shown in Figure 7C (middle and right, respectively). The circular shape of nanopillars directly patterned on glass wafer can be clearly observed at the central region of the metalens.

Upon the completion of the wafer-level fabrication and inspection, the wafer is diced into pieces with a dimension of 26×33 mm. The photograph of the diced metalens is shown in Figure 7D (left). To test the focusing functionality of the device, the fabricated metalens is mounted onto the characterization setup, with characterization methods reported in [67]. The optical intensity distribution along the propagation direction after the metalens is plotted as shown in Figure 7D (middle). The focusing effect can be clearly observed at the designed focal distance of 8 mm. The intensity distribution at the focal plane is plotted in Figure 7D (right), with a spot size (FWHM) of 1.5 μm observed. Meanwhile, the transmission of the whole metalens is measured to be about 57% due to the missing pillars at the edge of the metalens. Also, the diameters of the fabricated nanopillars on this wafer still have deviation from the designed dimension. Hence, the future work should be committed to optimize the fabrication process for directly patterning the metasurface layer on glass wafer.

To sum up, the works presented in this section using immersion scanner on 12-inch Si and glass wafer enable the large-scale mass production of the metasurface using industry standard fabrication tools. More optical materials with various properties, such as TiO_2, SiC, and AlN, can be demonstrated on existing platforms. The diversity and combination of functional devices, not limited to optical devices but also mechanical or piezoelectric devices based on this CMOS-compatible fabrication platform, can be explored.

3 Summary and outlook

In summary, the recent works on metasurface-based functional devices patterned by photolithography for large-area mass production have been summarized and presented. The metasurface devices patterned by 365 and 248 nm stepper photolithographic tool have been reviewed from fabrication and functionality perspectives. These works are based on 4-inch Si or glass wafer substrate, proving the effectiveness of using photolithography for metasurface-based devices with and without

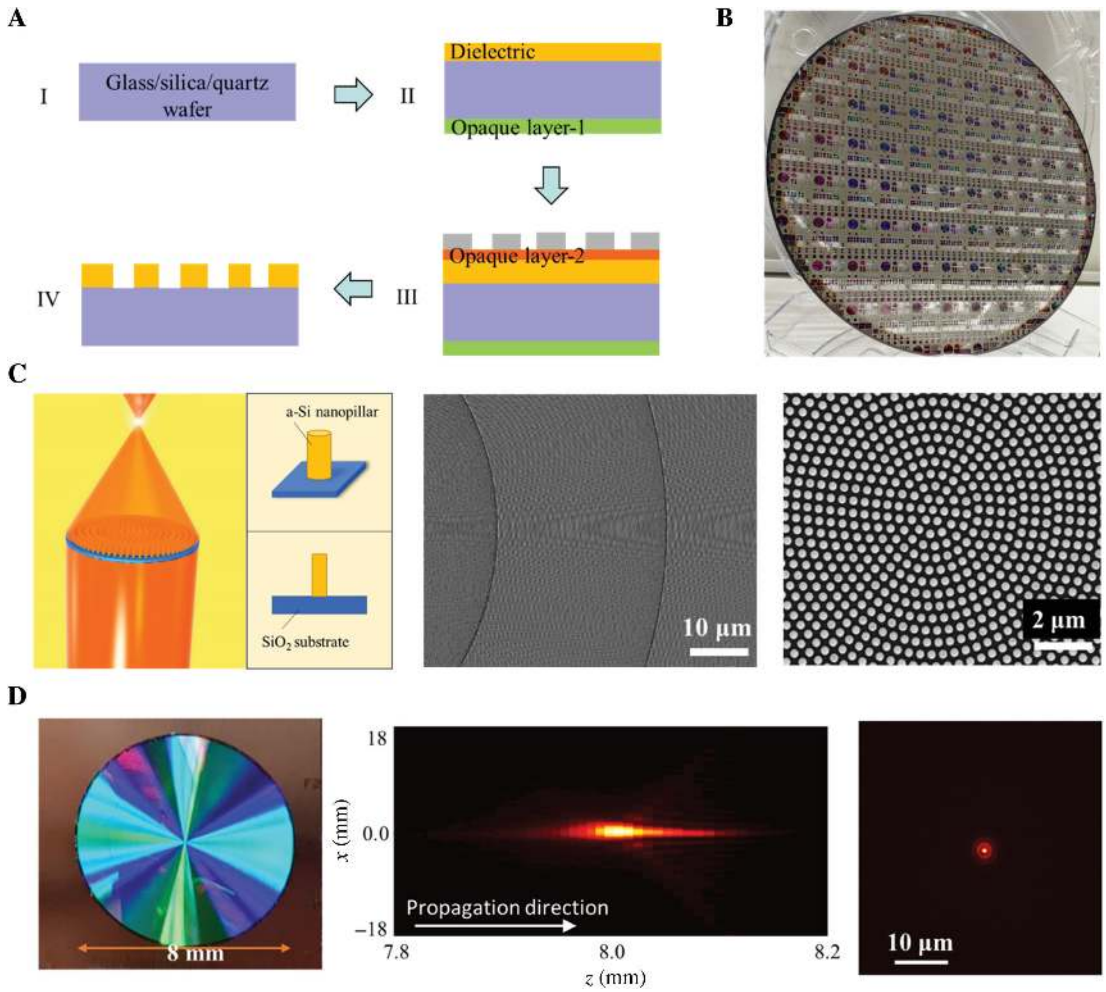

Figure 7: Metasurface-based devices demonstrated through direct patterning on 12-inch glass wafer.
(A) Fabrication process flow for direct patterning on glass wafer. (B) Fabricated 12-inch glass wafer. (C) Schematic of large-area metalens on glass substrate (left) and top-view (middle) and zoomed-in view (right) SEM images of the nanopillars with a height of 400 nm designed for metalens. (D) Fabricated 8-mm-diameter metalens on glass wafer (left); optical intensity distribution along the propagation direction after metalens, showing focusing effect (middle); and intensity distribution at the focal plane, showing spot size of 1.5 μm (right). (B–D) Adapted with permission from [74]. © The Optical Society.

tunability. Furthermore, the flat optics platforms developed at the IME using a 193 nm 12-inch immersion scanner lithographic tool on both Si wafer and glass wafer have been summarized, with wafer-level fabrication process presented and quality reported. The lithography enables higher pattern resolution on a larger wafer scale. The functional devices demonstrated on their corresponding platforms have also been included. The developed processes can be used for metasurface multipurpose wafer fabrication. This work provides a summary for the progress toward the mass manufacturing of flat optics devices using the CMOS-compatible fabrication technology.

In the near future, the research and development effort can be placed on the following four aspects. First, the limit of the nanostructure and gap size (CD) on IME platform using 12-inch 193 nm immersion lithography is 60 to 70 nm. Such CD size enables the realization of high-performance flat optics components working in the visible wavelength range. The CD can be further reduced by optimizing the photolithography process, for example, using multiple patterning. The smaller CD will enable the achromatic flat optics component designs as well as even shorter working wavelength of the device. Second, the fabrication process to pattern the metasurface directly on glass wafer can be further developed and optimized, with more materials to be explored on the platforms. Third, the possibility of monolithic integration of metasurface-based device with MEMS devices can be developed to achieve tunable metasurface on these fabrication platforms. Fourth, the focus can be on the module-level packaging of metasurface-based devices with components such as light-emitting diodes and photodetectors to form a functional module. The packaging process can be realized using the mature semiconductor device packaging technology. The applications of the functional modules include optical fingerprint, time-of-flight sensor, virtual reality, and augmented reality. Also, the development of wafer-level packaging can be conducted to achieve the mass production of the modules with further reduced fabrication cost.

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