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Large-scale organic nanowire lithography and electronics

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Controlled alignment and patterning of individual semiconducting nanowires at a desired position in a large area is a key requirement for electronic device applications. High-speed, large-area printing of highly aligned individual nanowires that allows control of the exact numbers of wires, and their orientations and dimensions is a significant challenge for practical electronics applications. Here we use a high-speed electrohydrodynamic organic nanowire printer to print large-area organic semiconducting nanowire arrays directly on device substrates in a precisely, individually controlled manner; this method also enables sophisticated large-area nanowire lithography for nano-electronics. We achieve a maximum field-effect mobility up to 9.7 $cm^2 V^{-1} s^{-1}$ with extremely low contact resistance ($<5.53\,\Omega$ cm), even in nano-channel transistors based on single-stranded semiconducting nanowires. We also demonstrate complementary inverter circuit arrays comprising well-aligned *p*-type and *n*-type organic semiconducting nanowires. Extremely fast nanolithography using printed semiconducting nanowire arrays provide a simple, reliable method of fabricating large-area and flexible nano-electronics.

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Processes have been developed that use inorganic nanomaterials for fabricating high-performance, large-area flexible electronic devices[1–3]. In particular, inorganic semiconductor nanowires (NWs) have been extensively studied because of their intriguing physical properties and great potential as building blocks for nanoscale electronics and optoelectronics[4,5]. Despite the many advantages of NWs, a reliable process for large-scale and controllable assembly of highly aligned NW parallel arrays based on 'individual control (IC)' of NWs must be developed, because inorganic NWs are mostly grown vertically on substrates and thus have been transferred to the target substrates by any of several non-IC methods, such as the random dispersion method with disordered alignment[4], and contact-printing technologies with unidirectional massive alignment[5]. In contrast to the significant efforts and in-depth research on inorganic NW devices, devices based on 'organic semiconducting' NWs (OSNWs)[6] have not been studied intensively, possibly because of the lack of a reliable IC process to fabricate highly aligned OSNW arrays[7–11], and to the lower charge-carrier mobility of OSNWs compared with inorganic semiconducting NWs. However, as organic semiconductors have many advantages, such as solution processibility, simplicity of designing molecules to tune electronic properties and the possibility of large-scale synthesis and multi-component systems at low cost, they are also promising for use in flexible electronic and optoelectronic devices[6,7,12,13]. For practical device application of OSNWs, they should be individually controlled for alignment and patterning at desired positions and orientations, and the number of OSNWs must be exactly defined. However, this objective has not yet been achieved to date for flexible organic nano-electronics, despite the significance. In addition, OSNWs should be fabricated directly on the device substrate without requiring any additional transfer process. Therefore, reliable and controllable processes to satisfy these requirements will provide large-area OSNW arrays and their applications to NW lithography, and electronic devices. In particular, large-scale organic NWs (ONWs) with circular shape can provide a facile route to nanolithography in large area. Existing inorganic NW lithography techniques to prepare nano-patterns for electronic devices use the randomly dispersed metal NW itself[14,15] or use randomly dispersed semiconductor NW as an etch mask[16]. However, with these non-IC processes, the position and orientation of individual NWs and nano-patterns are difficult to control, and thus sample-to-sample variation of device performance may not be avoided.

Here we report (i) high-speed, large-area printing of highly aligned, individually controlled OSNWs for NW electronics: the exact numbers of wires, their orientations and their dimensions are controlled directly on the device substrate without any transfer printing process; (ii) large-area ONW lithography (ONWL) using the highly aligned, individually controlled OSNWs; (iii) application of ONWL to fabricate large-area OSNW electronic devices with nanoscale channel length: we achieved unprecedented high field-effect mobility (μ_{FET}) from nano-channel ONW transistors with extremely low contract resistance; and (iv) the large-area complementary inverter circuit arrays comprising well-aligned *p*-type and *n*-type OSNWs. First, we used our own home-built ONW printer to print highly aligned, individually controlled OSNWs at desired positions on device substrates and to fabricate large-area OSNW transistor arrays. Then we used the aligned ONWs as a shadow mask to generate large-area nanoscale patterns very quickly, and fabricated large-area OSNW transistor arrays with nanoscale channel length and complementary inverter arrays, using well-aligned *p*- and *n*-type polymer semiconductor NWs; this scalable method can overcome the drawbacks of conventional electron-beam lithography, which is relatively slow, complicated and expensive. As our electrohydrodynamic ONW printing (ONP) technique can align the ONWs in continuous jet mode, unlike conventional drop-on-demand-type jet printing techniques[17], 'perfect circular' NWs can be generated. We obtained highly aligned ONWs (or organic nanofibres) from poly(9-vinyl carbazole) (PVK), semiconducting poly(3-hexylthiophene) (P3HT) and poly{[N, N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2, 6-diyl]-alt-5,5′-(2,2′-bithiophene)} (Polyera ActivInk N2200); we used PVK as a shadow mask for ONWL and P3HT as the semiconductor layer in transistors. By combining NW printing and ONWL, we achieved a very high maximum μ_{FET} up to $9.7\,cm^2\,V^{-1}\,s^{-1}$ (average $\mu_{FET} \sim 3.8\,cm^2\,V^{-1}\,s^{-1}$) in P3HT NW transistors, even with a very short channel length of $\sim$300 nm with extremely low contract resistance ($<5.53\,\Omega\,cm$). We finally demonstrated large-area complementary inverter circuit arrays comprising well-aligned *p*-type and *n*-type OSNWs.

Results

Fabrication of aligned ONWs. Our home-built ONW printer (Fig. 1a) consists of a high-speed linear motor x–y stage, a flat grounded collector, a micrometre to control the tip-to-collector distance, a nozzle (tip inner diameter: $\sim$100 μm), a syringe pump and a high-voltage generator. To form the ONWs, an electrohydrodynamic process is used like, similar to electrospinning[9–11]. This employs the electrostatic force to stretch the viscous polymer solution into NW: a viscous polymer solution is injected into the nozzle and high-voltage is applied to the nozzle. Because of the electric field, the repulsive force within the charged solution and the attractive force between the solution at the nozzle tip and a grounded collector shape the droplet into a Taylor cone at the nozzle tip. When these forces are larger than the surface tension of solution, a jet is ejected from the tip of the Taylor cone and deposited onto the grounded collector with rapid elongation. Unlike conventional electrospinning processes, we approached the nozzle tip near to the collector (less than 1 cm), which resulted in suppression of the chaotic whipping motion of jetted polymer solution: as the tip-to-collector distance decreases, perturbation of jetted solution decreases[18]. By moving the motorized x–y stage while the NWs are ejected, we can align the ONWs with desired orientation.

To verify the capacity of ONP to print ONWs quickly with precise alignment, we used a solution of 3.96 wt% PVK in styrene. PVK NWs were printed while the collector moves laterally at $13.3\,cm\,s^{-1}$ (maximum speed $100\,cm\,s^{-1}$). The resulting patterns had totally parallel orientation; the NWs had regular spacing of 50 μm and diameter of 289.26 ± 35.37 nm (Fig. 1b). The NW diameter can be controlled by adjusting polymer concentration (Supplementary Fig. S1a,b). Therefore, the ONW diameter can be further reduced to <100 nm (Supplementary Fig. S1c). Optical microscope (Fig. 1b) and scanning electron microscope images (inset of Fig. 1b) demonstrate the formation of uniform and continuous ONWs. The tip-to-collector distance was $\sim$2.5 mm; if it was <2.5 mm, the jets arrived at the substrate in liquid form and merged readily without forming solid-state wires, because the solvent did not have sufficient time to evaporate. In cross section, the PVK NWs were perfectly circular (Fig. 1c), implying successful formation of ONWs. When the collector was stationary, self-entanglement of NWs ('local spiraling') was observed (Supplementary Fig. S2); this is further evidence of successful formation of wires, because it occurs when the polymer jet is fully solidified. Aligned PVK NWs (Fig. 1b) were formed by writing a long single strand of wire laterally. The total length of the aligned NWs was as long as $\sim$15 m; printing them required only $\sim$2 min.

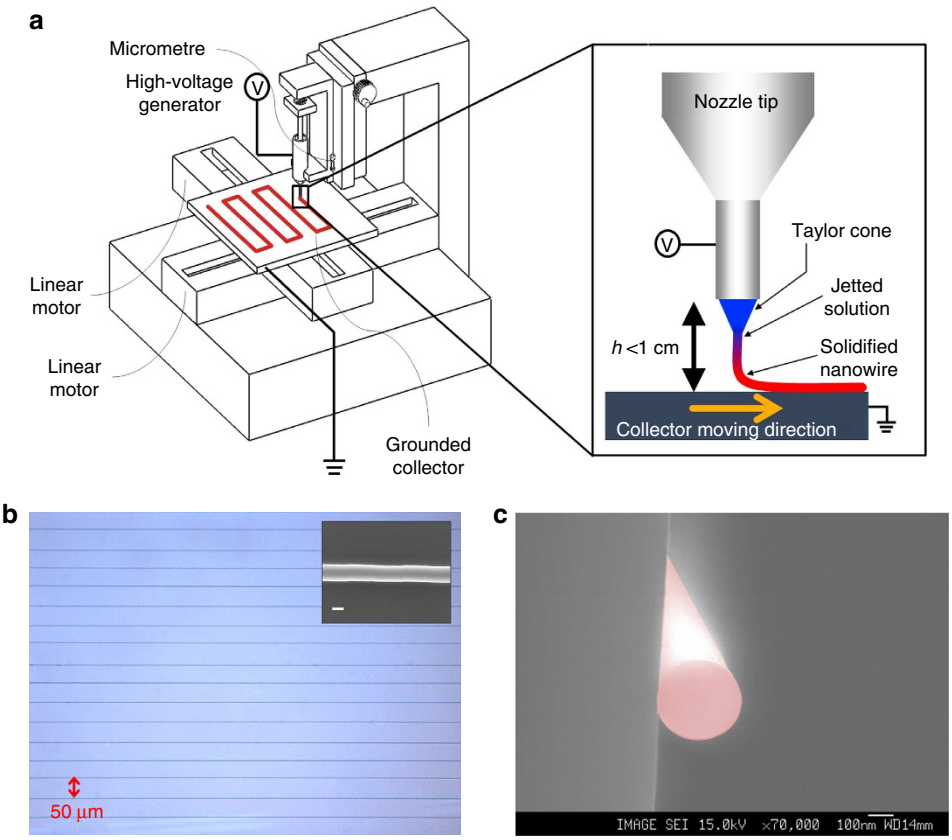

Figure 1 | Organic nanowire printing. (**a**) Schematic diagram of ONW printer and NW printing process. (**b**) Optical micrograph of well-aligned PVK NWs. The diameter of PVK NW is 290 nm (inset, scale bar, 200 nm). (**c**) Field emission scanning electron microscope image showing cross section of well-aligned PVK NW, which forms a perfect circle.

Highly aligned ONW field-effect transistors. When fabricating transistors using OSNWs, forming the wires at the desired position in an individually controlled fashion is usually very difficult[6,7,9–12]. Using ONP, we fabricated well-aligned P3HT NW field-effect transistors (FETs) very simply and quickly. P3HT was used as the active material for large-area organic wire electronic device arrays, and poly(ethylene oxide) (PEO) (Aldrich, $M_w \sim 400{,}000$) was added to the P3HT solution (P3HT:PEO = 80:20, w/w) to increase its viscosity. To fabricate the OSNW FETs, we printed the blend wires on the Si/SiO_2 (100 nm) substrate and deposited Au (100 nm) for the source and drain electrode. Although the Si/SiO_2 substrate has an insulating surface, ONWs can be successfully printed by ONP, because the insulating layer is very thin enough to maintain a high electric field between the nozzle tip and the grounded collector. Therefore, even if the substrate has a thin insulating layer, we can print the ONWs on any kind of substrate: on an insulating SiO_2 layer (300 nm) and even a paper (108 µm; Supplementary Fig. S3).

The P3HT:PEO-blend NWs were successfully printed between source and drain electrodes (Fig. 2a inset). The drain-current (I_D) to gate voltage (V_G) transfer characteristic measured at drain voltage $V_D = -50$ V for V_G swept from 15 to -60 V shows the behaviour of typical *p*-type FETs (Fig. 2a). The gate effect was also observed in the output ($I_D - V_D$) characteristic (Fig. 2b), which means that an effective channel was formed despite the presence of PEO.

In NW FETs using a thin-film gate dielectric, μ_{FET} is calculated as[19]:

$$\mu_{FET} = \frac{L^2 g_m}{V_D C} = \frac{L^2}{V_D C} \cdot \frac{d(I_D)}{d(V_G)}, \quad (1)$$

where $L = 50$ µm is its channel length and C is its capacitance (F) determined using the cylinder-on-plate model[20],

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}\left(\frac{h+r}{r}\right)}, \quad (2)$$

where $\varepsilon_0 = 8.85 \times 10^{-12}$ F m^{-1} is vacuum permittivity, $\varepsilon_r = 3.9$ is the relative permittivity of the SiO_2 gate dielectric layer, $h = 100$ nm is the thickness of the SiO_2 gate dielectric layer and r is NW radius ($\sim$275 nm for the NW with 30% PEO and $\sim$780 nm for P3HT blend NW with 20% PEO).

The calculated μ_{FET} of the P3HT:PEO-blend (80:20, w/w) NW FET (bottom-gate) was 0.015 cm^2 V^{-1} s^{-1}, which is comparable to that of pure P3HT NW FET[11] ($\mu_{FET} = 0.03$ cm^2 V^{-1} s^{-1}). In P3HT:PEO-blend (70:30, w/w) NW FETs, NWs were more easily printed due to increased viscosity, but μ_{FET} was lower: 0.0047 cm^2 V^{-1} s^{-1} (Supplementary Fig. S4a), because insulating PEO phases in a P3HT matrix hinder charge transport and block the stacking of P3HT chains; these effects degrade μ_{FET}. To increase electrical properties of NW FETs, we also demonstrated a top-gated device using poly(methyl methacrylate) (PMMA) as a gate dielectric (Supplementary Fig. S4b). The calculated μ_{FET} of the top-gated P3HT blend NW FET with 30% PEO was 0.012 cm^2 V^{-1} s^{-1}, similar to the bottom-gated P3HT:PEO-blend (80:20, w/w) NW FET. We have also examined the bias stress stability of P3HT:PEO-blend NW FETs (Supplementary Fig. S4c,d and Supplementary Note S1). After initial gate bias stress for 1 h to fill the trap states, μ_{FET}, on/off ratio and threshold voltage (V_{th}) shift were saturated and then did not show significant degradation for 11 h.

We fabricated *n*-type NW FETs by ONP using a N2200:PEO-blend (80:20, w/w) as an *n*-type semiconducting polymer.

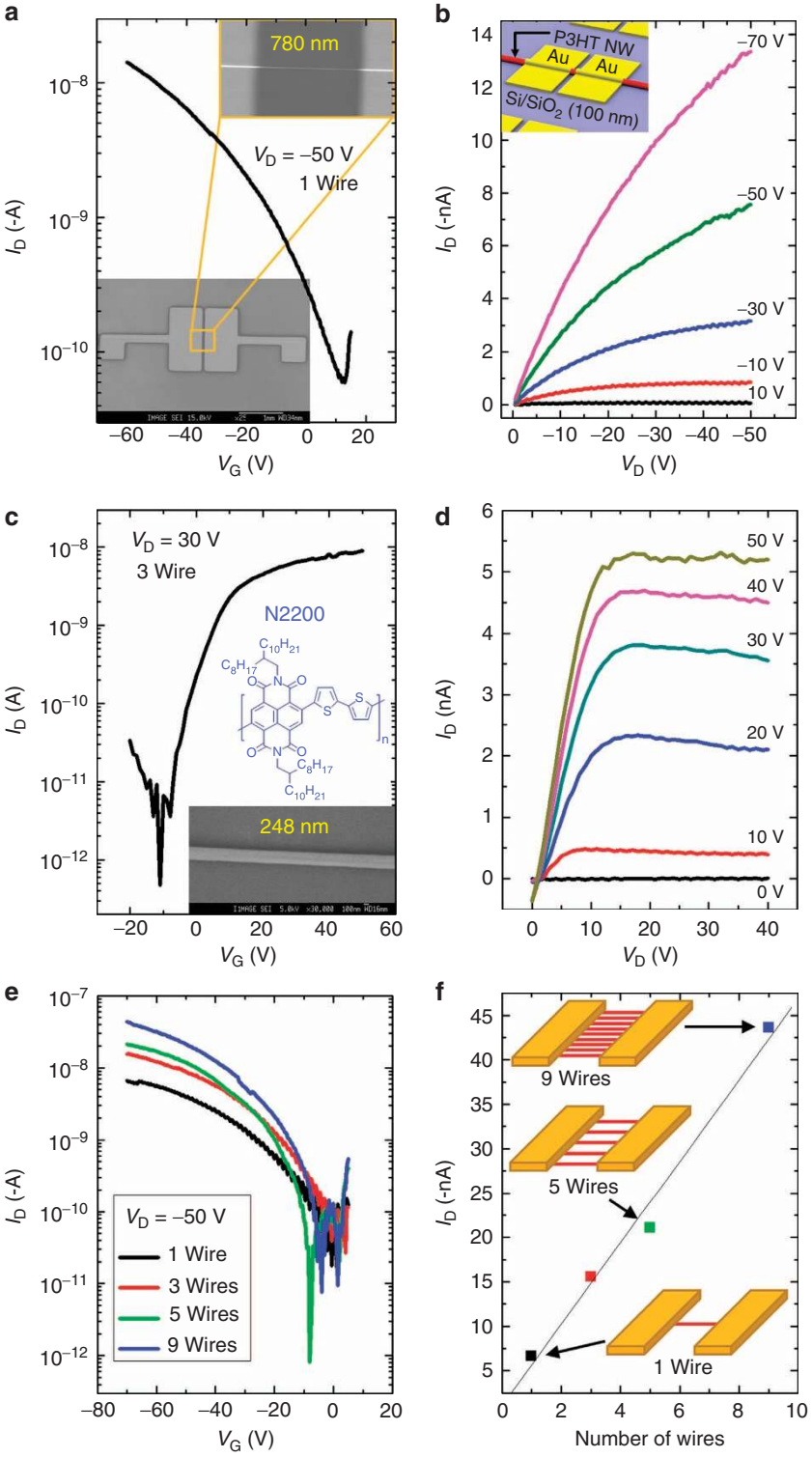

Figure 2 | Highly aligned NW FETs. (**a**) Transfer characteristics (I_D-V_G) (inset: device appearance and channel region) and (**b**) output ($I_D - V_D$) characteristics of P3HT blend NW FET with 20% PEO (inset: device structure). (**c**) Transfer characteristics and (**d**) output characteristics of poly{[N, N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} (N2200) blend NW FET with 20% PEO. (**e**) Transfer characteristics of P3HT blend NW FET with 30% PEO at different numbers of wires. (**f**) Maximum on-current versus the number of wires.

The *n*-type NW FET (bottom-gate) showed typical *n*-type transfer and output characteristics (Fig. 2c,d) with the electron μ_{FET} of $0.012\,cm^2\,V^{-1}\,s^{-1}$. The N2200:PVK-blend (80:20, w/w) exhibited electron μ_{FET} of $0.03\,cm^2\,V^{-1}\,s^{-1}$ (Supplementary Fig. S5), which is slightly lower than that of a pure N2200 thin-film FET in a bottom-gate geometry with a SiO_2 gate dielectric ($\mu_{FET} = 0.06\,cm^2\,V^{-1}\,s^{-1}$)[21]. Achievement of both well-aligned organic *p*-channel and *n*-channel NW FETs provides fundamental resources for various large-area electronic applications.

Another important advantage of ONP is that the number of aligned NWs can be easily controlled. The P3HT:PEO-blend (70:30, w/w) NW FETs with one, three, five and nine wires were fabricated. According to the $I_D - V_G$ relationship (Fig. 2e), the maximum on-current level increased linearly with the number of wires in FETs (4.6×10^{-9} A per wire) (Fig. 2f); this relationship indicates that device characteristics can be controlled by adjusting the number of wires with the ONP technique. Calculated μ_{FET} values of NW FETs were almost the same irrespective of the number of wires (0.0047, 0.0054, 0.0053 and 0.0039 $cm^2 V^{-1} s^{-1}$ for one, three, five and nine wires, respectively).

According to transmission electron microscopy (Supplementary Fig. S6a) and elemental analysis results (Supplementary Fig. S6b,c and Supplementary Note S2), a P3HT:PEO-blend NW has a core-shell structure along the wire axis. The origin of the core-shell structure of printed NW is explained by phase separation of polymer blends, which can be caused by the incompatibility or the large solubility parameter difference in solution[22]. On the basis of grazing-incidence X-ray diffraction (GIXRD) and polarized photoluminescence analysis for the aligned OSNWs, we found that the aligned NWs had long-range ordered nano-domains along the wire axis (Supplementary Figs S7 and S8, and Supplementary Notes S3 and S4). This is mainly related to the directed self-assembly between π-conjugated backbone chains extended along the wire axis by the tip-to-collector electric field, during jetting. It was also found that the extended P3HTs had strong intermolecular π-overlap as a result of ultraviolet-visible spectroscopy analysis (Supplementary Fig. S8a). Such extended orientation of P3HTs along the source/drain electrode and enhanced intermolecular π–π overlap facilitates charge transport in NW FETs. However, phase separation between P3HT and PEO is not perfect. Small randomly distributed PEO-rich phases occur very sparsely inside the P3HT core (red circle in Supplementary Fig. S6a,b). These small phases scatter the charge transport in the channel and cause the variation of μ_{FET} in P3HT:PEO-blend NW FETs.

ONWL and nano-channel FETs. We also applied ONP to form large-area nano-sized patterns. Using ONWL, well-aligned nano-gap metal patterns can be fabricated very quickly at a desired position. In the ONWL process (Fig. 3a), aligned PVK NWs fabricated using ONP are used as a shadow mask of deposited metal films. After printing PVK NWs on a substrate, followed by deposition of metal films, the ONWs are removed either by sonicating the solvent to dissolve them, or by using adhesive tapes to detach them. As the contact area between PVK NWs and substrate is minimal, and as the deposited metal film is thinner than the NW radius ($\sim$150 nm), resulting in no physical contact between the NW mask and deposited metal film, wires can be easily removed (Fig. 3b). Conventional drop-on-demand-type jet-printing techniques produce only continuous lines with very low aspect ratio formed via the connection of each drop (not circular wires) so that the lift-off of printed mask lines to achieve nanoscale patterns is quite difficult. Using ONWL, parallel patterns of gold nano-gaps were successfully formed, which had the same orientation and spacing as those of PVK NWs (Fig. 3c). The size of the gaps can be easily controlled by adjusting NW diameter (Fig. 3d).

ONWL can be used to fabricate complicated patterns on large area simply. With perpendicularly aligned NW patterns (Fig. 3e), grid-structured nano-gap patterns were obtained over an area of $\sim$300 cm^2 on an 8-inch wafer (Fig. 3f and Supplementary Fig. S9). Furthermore, ONWL can be also used to fabricate organic nano-gap pattern and to fabricate nano-pattern on flexible substrate. Using ONWL, aluminum tris (8-hydroxyquinoline) (Alq_3) layer was successfully patterned with the gap

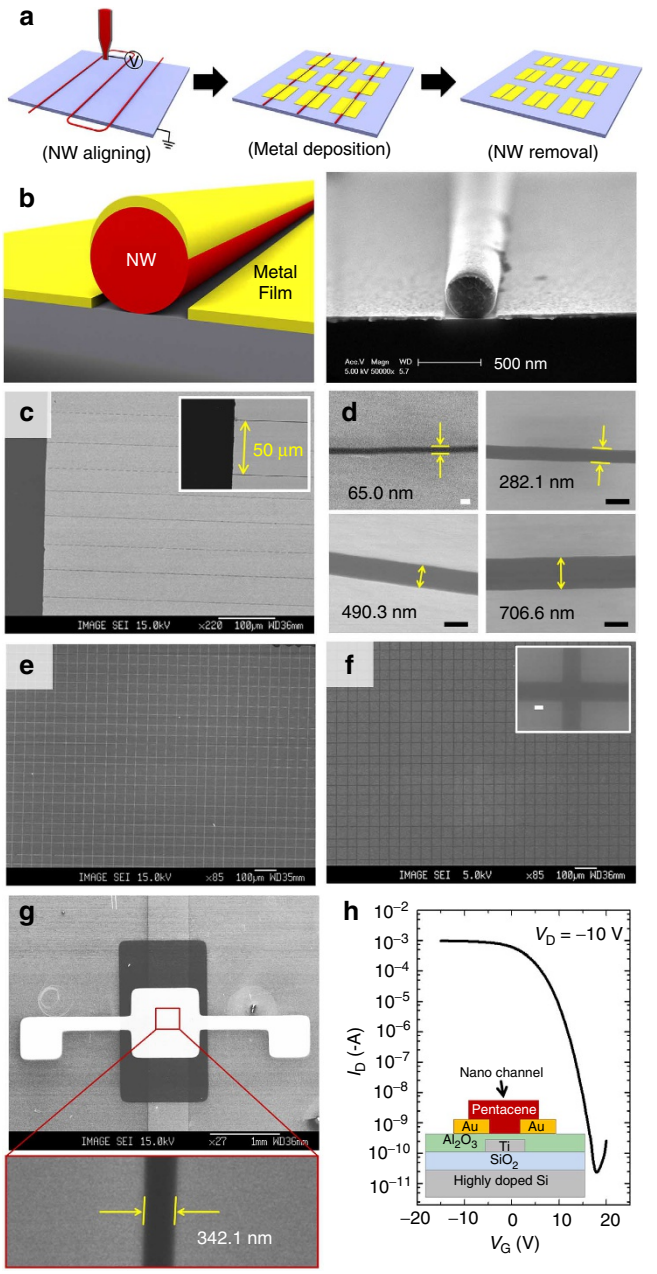

Figure 3 | ONWL to fabricate the nano-gap metal pattern. (**a**) Schematic illustration of the process for ONWL. (**b**) Schematic illustration (left) and scanning electron microscope image (right) showing the cross section of an ONW after metal deposition process in ONWL. There is no contact between NW and deposited metal film. (**c**) Parallel array of nano-sized gold gap with 50-μm spacing. (**d**) Size of gold gap can be controlled by diameter of NWs. Scale bar, 100 nm (white), 500 nm (black). (**e**) Perpendicular pattern of PVK NWs with 50-μm spacing and (**f**) corresponding grid-structured pattern of gold nano-gap (inset: region of intersection, scale bar, 200 nm). (**g**) Device appearance and nano-sized electrode gap of pentacene thin-film FET with nano-channel. (**h**) Transfer characteristic ($I_D - V_G$) of pentacene thin-film FET (inset: device structure).

width of $\sim$350 nm (Supplementary Fig. S10). When ONWs were printed on flexible polyarylate substrate, they were easily detached by adhesive tape after metal deposition and nano-sized electrode gap patterns were formed (Supplementary Fig. S11). It means that ONWL is very applicable to fabricate the flexible nano-electronics. Therefore, ONWL is a potential alternative method to

replace E-beam lithography, which has been usually used to fabricate the nano-patterns.

ONWL can be used to fabricate nano-channel transistors. Using the nano-gap pattern as an electrode gap, pentacene thin-film transistors with nano-channels were fabricated. A nano-gap of $\sim$340 nm was successfully formed (Fig. 3g). The calculated μ_{FET} was 0.041 $cm^2 V^{-1} s^{-1}$ and the on/off current ratio was very high: 4.18×10^7 (Fig. 3h). This result in the nano-channel device is comparable with general properties of bottom-contact pentacene thin-film transistors[23].

By combining ONP and ONWL, we fabricated organic FETs with nanoscale channel length and channel width (Fig. 4a). ONP produced well-aligned P3HT:PEO-blend NWs as the active channel, and ONWL produced a gold electrode with a nano-gap on top of them (Fig. 4b). In these FETs, I_D increased linearly with V_D and showed no saturation regime (Fig. 4c); this lack of a saturation regime is due to the short channel effect[15,24], which occurs in FETs that have sub-micrometre channel length. If the magnitude of V_D was $\geq$30 V, the device broke down as the channel length is so short. Calculated μ_{FET} was 0.0093 $cm^2 V^{-1} s^{-1}$.

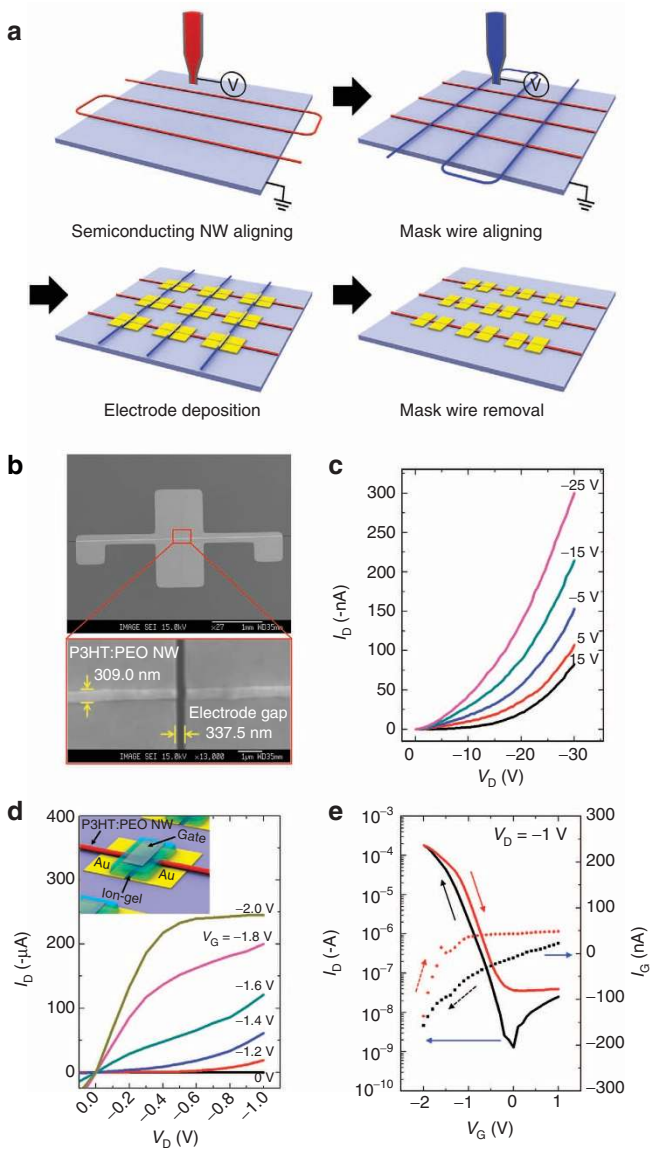

Figure 4 | Organic FET with nano-channel length and width. (**a**) Schematic illustration of the process to fabricate organic FET with nanoscale channel length and channel width. (**b**) Scanning electron microscope images of P3HT:PEO-blend (70:30, w/w) NW and nano-sized electrode gap. (**c**) Output characteristics ($I_D - V_D$) of P3HT blend NW FET with nano-channel length. (**d**) Output characteristics (inset: device structure) and (**e**) transfer characteristic ($I_D - V_G$) (solid line) and gate current versus gate voltage ($I_G - V_G$) characteristics (dot line) of P3HT:PEO-blend (70:30, w/w) NW and nano-channel FET based on the polyelectrolyte gate dielectric.

To reduce the operating voltage of ONW FETs, high-capacitance ion-gel polyelectrolyte was used as a gate dielectric material. Ion-gel films were formed on the P3HT:PEO-blend NW by gelation of poly(styrene-b-methylmethacrylate-b-styrene) (PS-PMMA-PS) triblock copolymer in an ionic liquid, 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide[25]; in the single-NW FET based on ion-gel (Fig. 4d inset), μ_{FET} and the on-current were dramatically enhanced (μ_{FET} $\sim$3.67 $cm^2 V^{-1} s^{-1}$, I_{on} $\sim 1.81 \times 10^{-4}$ A) compared with SiO_2 gate dielectric device (Fig. 4d,e), in spite of low V_D (-1 V) and V_G (-2 V); the on/off current ratio was also increased (to 1.38×10^5); the best device showed μ_{FET} up to 9.7 $cm^2 V^{-1} s^{-1}$ (Supplementary Fig. S12). Furthermore, a saturation regime was observed, which did not appear in SiO_2 gate dielectric devices. These observations indicate that the short channel effect was dramatically reduced in the ion-gel-gated FETs. This apparent reduction of operating voltage occurs, because the ionic electrolyte introduces a large number of charge carriers into the channel. In accumulation mode, electrical double layers are formed at the interfaces of the gate-ionic electrolyte and the ionic electrolyte-semiconductor[26], and electrochemical doping occurs because of penetration of ions into the semiconductor[27]. Unlike typical insulating materials, no potential drop occurs in ionic electrolytes; hence, a large number of holes are induced at very low V_G. These results are consistent with previous reports[25,27]. Extremely low contact resistance ($<$5.53 Ω cm) also contributes to the remarkable reduction of short channel effect (Supplementary Fig. S13 and Supplementary Note S5).

To calculate μ_{FET} in ion-gel-gated NW FETs, we used two different equations: the conventional thin-film FET equation[21,23] and the equation based on the gate-displacement current and induced charge density[28,29]. First, μ_{FET} was calculated from the simple 'thin-film FET model' (equation 3)[21,23].

$$\mu_{FET} = \frac{2L}{W \cdot C} \cdot \left(\frac{d(I_D^{1/2})}{d(V_G)} \right)^2 \quad (3)$$

where W is the channel width. However, this equation is used for FET device with a two-dimensional (2D) metal-insulator semiconductor geometry and is derived on the basis of gradual channel approximation (refer to Supplementary Table S1, Supplementary Fig. S14 and Supplementary Note S6). It also gave unacceptably high values (average μ_{FET}: $\sim$31.00 $cm^2 V^{-1} s^{-1}$) for our devices. Therefore, thin-film FET model is not valid for the ionic-electrolyte-gated NW FET.

Instead of thin-film FET model, μ_{FET} can be computed using gate-displacement current and induced carrier density (P_i),[28,29]

$$\mu_{FET} = \frac{L}{W} \cdot \frac{I_D}{V_D \cdot eP_i} \quad (4)$$

where e is the elementary charge. The μ_{FET} calculated from gate-displacement current gave more reasonable values (average μ_{FET}: $\sim$3.8 $cm^2 V^{-1} s^{-1}$) than that calculated from equation (3). Although the induced carrier density is inversely proportional to μ_{FET}, the calculated μ_{FET} is much higher than those of general P3HT FET devices (Supplementary Table S1), because the large induced hole density fills the trap of the P3HT channel and smoothes the electrostatic potential variation that occurs in the

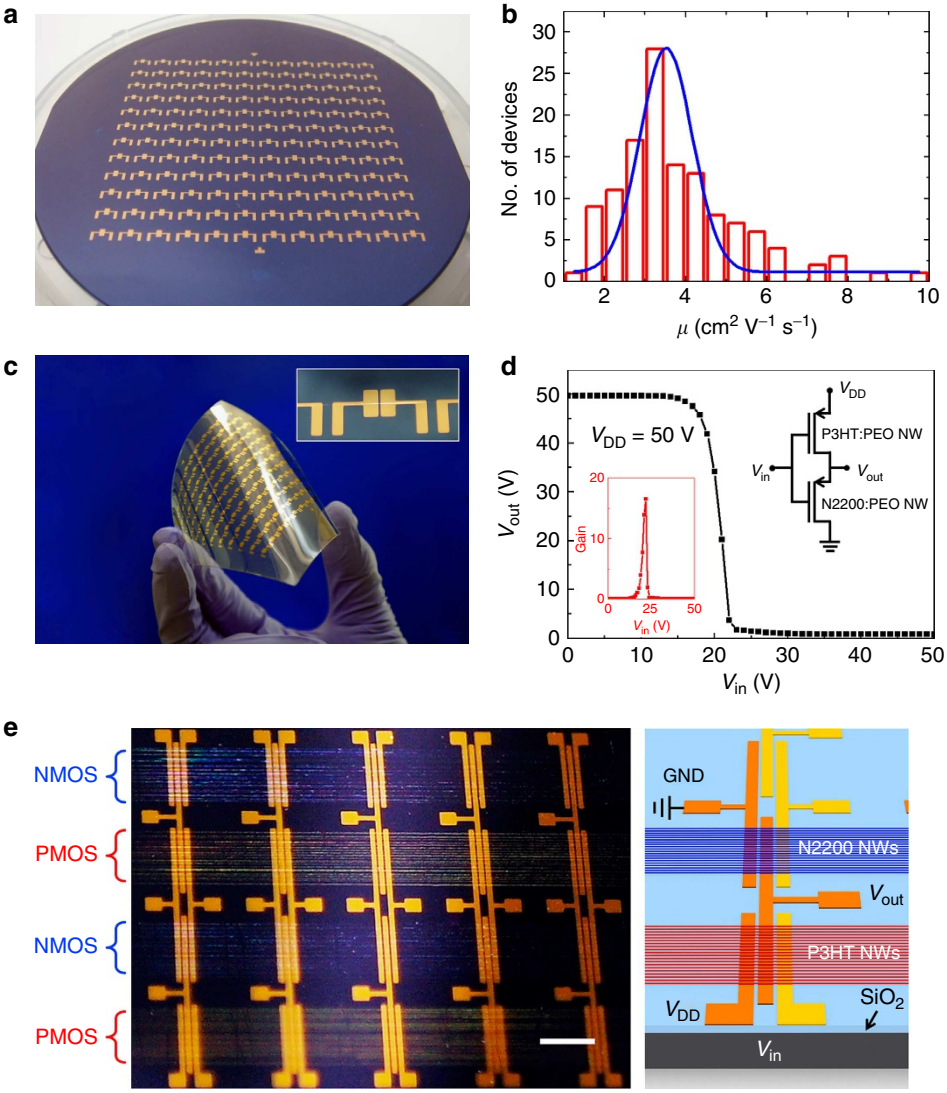

Figure 5 | Large-area single P3HT:PEO-blend NW FET and complementary inverter circuit arrays. (**a**) Large-area single P3HT:PEO-blend (70:30, w/w) NW FET array (7 cm × 7 cm) with ~300-nm channel length (144 bottom-contact devices). (**b**) Histogram of the mobility for large-area P3HT:PEO-blend NW FET array with an average of $3.8 \pm 1.6\,cm^2\,V^{-1}\,s^{-1}$. (**c**) Large-area single P3HT:PEO-blend NW FET array on polyarylate (PAR) substrate. (**d**) Input–output voltage characteristic for complementary inverter circuit based on P3HT:PEO-blend NWs and N2200:PEO-blend NWs (inset: gain characteristics). (**e**) Optical image of inverter array (left, scale bar, 2 mm) and schematic illustration of an inverter (right).

channel due to trapped charges[29]. In addition, we found that the core-shell structure of P3HT:PEO-blend NWs and extended chain orientation of P3HT along the wire axis contributed to the high μ_{FET} of ion-gel-gated NW FETs (Supplementary Figs S6–S8, S15 and S16, and Supplementary Notes S7 and S8).

We achieved a large-area (7 cm × 7 cm) NW FET array on a 4-inch wafer. This array consists of 144 short-channel FETs that use a continuous single-stranded P3HT:PEO-blend (70:30, w/w) NW (Fig. 5a). ONWL was used to form source/drain gaps ~300 nm, and ion-gel was used as the gate dielectric material. Fabricating the single strand of P3HT NW on the wafer scale array took only ~7 s. The figures of distribution of the field-effect mobility and maximum on-current (Fig. 5b and Supplementary Fig. S17) show an extremely high μ_{FET} of $9.7\,cm^2\,V^{-1}\,s^{-1}$ (average $\mu_{FET} = 3.8 \pm 1.6\,cm^2\,V^{-1}\,s^{-1}$), an extraordinarily high average current level of 0.31 ± 0.13 mA and a high average on/off current ratio (1.70×10^6). We also used ONP to fabricate a large-area NW transistor array on a flexible plastic substrate (polyarylate; Fig. 5c).

We finally fabricated the complementary inverter array using well-aligned P3HT:PEO-blend NWs and N2200:PEO-blend NWs (Fig. 5d). The photograph of inverter arrays based on printed NWs is shown in Fig. 5e. A number of N2200:PEO-blend (70:30, w/w) NWs and P3HT:PEO-blend (70:30, w/w) NWs were aligned on the pre-patterned Ti/Au electrodes with $L = 50\,\mu m$ on a Si/SiO_2 (100 nm) substrate. The transistor output currents were readily matched by controlling the number of NWs using ONP. The NW complementary inverter showed the typical switching characteristic with gain of ~17. The dynamic switching behaviour of P3HT/N2200 NW complementary inverters was also demonstrated (Supplementary Fig. S18 and Supplementary Note S9).

Discussion

We first demonstrated practical large-area electronic device applications of individually-controlled OSNWs using ONP, which can be used to print, align and pattern circular ONWs in desired positions and orientations directly on large-area device

substrates. We also developed a large-area ONWL technique to fabricate nano-electronic devices quickly; this technique has the potential to replace conventional E-beam lithography. By combining ONP and ONWL, we fabricated ONW FETs with nanometer channel length in large area, which exhibited unprecedented maximum μ_{FET} of 9.7 $cm^2 V^{-1} s^{-1}$ (average μ_{FET} ~3.8 $cm^2 V^{-1} s^{-1}$), high on/off current ratio (~10^6) and extremely low contact resistance (~5.53 Ω cm). ONP and ONWL can be applied to fabricate large-area nano-structured electronic device arrays very simply and quickly. Moreover, we demonstrated large-area complementary inverter circuit arrays composed of highly aligned *p*-type and *n*-type OSNWs. Although inverters with randomly oriented ONWs[30] were previously introduced, our result demonstrates the first arrays of complementary inverters in which the orientation, position and numbers of ONWs are well-controlled individually in large area. Our strategy to fabricate ONWs in an individually-controlled fashion and their large-area nano-electronic devices in a precisely controlled manner is a promising approach to realize large-area flexible nano-electronics and provides important bases for future textile electronics using long-stranded wires or fibres.

Methods

Equipment setup. The ONW printer consists of a syringe pump (NanoNC) mounted vertically over the collector, a gas-tight syringe (Hamillton), a 25–32 gauge stainless steel nozzle, a micrometre to control the tip-to-collector distance, a high-voltage generator (NanoNC) and a grounded flat-type collector (20 cm × 20 cm) moved by a linear motor stage (Yaskawa).

Fabrication of aligned PVK NW. PVK (M_w ~1,100,000, Aldrich) in styrene solution (37.5 mg ml^{-1}) was injected through the metal nozzle at a feed rate of 500 nl min^{-1}. For production of PVK NWs, the ONW printer was used; 3–4 kV was applied to the nozzle and tip-to-collector distance was set at 2.5 mm. While the NW was being collected on the substrate, the collector moved in a zigzag at 13.3 cm s^{-1}.

Highly aligned NW FET and complementary inverter. P3HT (Regioregularity ~90%, M_w ~45,570, Aldrich) and PEO (M_w ~400,000, Aldrich) were used to prepare 70:30 and 80:20 (w/w) blend solutions of P3HT:PEO. Trichloroethylene (TCE) and chlorobenzene were mixed in appropriate ratio and used as the co-solvent of the P3HT:PEO-blend solution. The blended P3HT solution was injected into the metal nozzle and P3HT:PEO-blend NWs were fabricated and aligned on the substrate using the ONW printer. To fabricate the N2200:PEO-blend NWs, the blend solution of N2200 (Polyera) and PEO was prepared using TCE and chlorobenzene as the cosolvent. A bit of isotactic polystyrene (M_w ~400,000, Aldrich; ~1 wt% of PEO) was added into solution, and then N2200:PEO-blend NWs were fabricated using our ONW printer.

For FET fabrication, highly doped silicon wafers and thermally grown SiO_2 (100 nm) were used as gate electrodes and gate dielectrics, respectively. After semiconducting NWs were aligned on the substrate, a thermal evaporator was used to deposit Au (100 nm) for the source and drain electrodes. The channel length was 50 μm.

For inverter fabrication, highly-doped silicon wafer and thermally grown SiO_2 (100 nm) were used as gate electrodes and gate dielectrics, respectively. Inverter electrode patterns of Ti (3 nm) and Au (30 nm) with a channel length of 50 μm were thermally deposited on the substrate. N2200:PEO-blend NWs and P3HT:PEO-blend NWs were printed on the pre-patterned substrate.

ONWL and nano-channel FETs. Au (100 nm) or Ti (3 nm)/Au (30 nm) or Alq_3 (30 nm) was deposited on the aligned PVK NW pattern using a thermal evaporator. PVK NW was removed using adhesive tape or by sonication in a solvent (chloroform or TCE), then the nano-gap metal pattern was formed.

For fabrication of transistors with nanoscale channel length, thermally evaporated Ti (30 nm) on the Si/SiO_2 (100 nm) wafer was used as a gate electrode, and Al_2O_3 (50 nm) served as a gate dielectric, which was formed by atomic layer deposition. ONWL was used to fabricate a nano-gap Au pattern on the substrate for source and drain electrodes. Finally, pentacene (50 nm) was thermally deposited on the nano-gap Au pattern. For the NW and nano-channel transistor, aligned P3HT:PEO-blend NWs were fabricated instead of pentacene.

P3HT NW FETs with ion-gel dielectric. ONWL was used to fabricate nano-gap patterns; after PVK NWs were printed on Si/SiO_2 (100 nm) wafer, Ti (3 nm)/Au (30 nm) was deposited atop the PVK NWs, which were then removed to form source and drain electrodes with nano-gap patterns. A P3HT:PEO-blend NW was aligned on the Ti/Au source–drain patterns using ONP. For ion-gel gate dielectric formation, poly(styrene-block-methyl methacrylate-block-styrene) (PS-PMMA-PS) synthesized[31]) triblock copolymer, with block molecular masses M_n = 6.2 kg mol^{-1} for PS and M_n = 105 kg mol^{-1} for PMMA, and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (solvent innovation) ionic liquid were dissolved in ethyl acetate at a 0.7:9.3:90 ratio (w/w) and then drop-cast onto a P3HT NW pattern that had an Au source and drain contact. After removing the solvent, an ion-gel film was formed by physical association of the PS blocks in the ionic liquid. To form a gate electrode, the substrate was flipped over and placed on a PEDOT:PSS (Baytron P) thin film. PEDOT:PSS layer was clearly transferred to the top surface of the ion-gel.

NW morphology was observed by scanning electron microscope imaging using a Jeol JSM-6330F at an acceleration voltage of 15 kV and by transmission electron microscopy imaging using a JEOL JEM-2200FS (with Cs-corrector) (National Center for Nanomaterials Technology, Korea) at an acceleration voltage of 200 kV without staining. Optical microscope and fluorescence microscope images were recorded using a Zeiss Axioplan 2 optical microscope. 2D GIXRD experiments on P3HT, P3HT:PEO-blend films and arrayed P3HT:PEO-blend NWs on Si substrates were performed at beam line 9A of Pohang Acceleration Laboratory (Korea). The sample was mounted on a two-axis goniometer on top of an x–z stage and the scattered intensity was recorded by a Mar charge-coupled device detector. The incident-beam angle was *ca.* 0.15° for all 2D GIXRD patterns. Photoluminescence spectra were measured by JASCO FP-6500. Ultraviolet absorption spectra were recorded by ultraviolet-visible spectrophotometer (S-3100, Scinco). The electrical measurements of SiO_2-gated devices were conducted under nitrogen atmosphere at room temperature using an *I–V* tester (Keithley 4200, Keithley Instruments Inc.). The electrical measurements of ion-gel-gated devices were conducted under vacuun condition at room temperature using an *I–V* tester (Keithley 238 and 6517A, Keithley Instruments Inc.). The dynamic characteristics of NW inverters were measured using a pulse generator (Model 214B, Hewlett-Packard Co.) and a digital oscilloscope (Model 54832B, Agilent Technologies Inc.).

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Author contributions

S.-Y.M. conducted most of experiments, including the setup of equipment, development of ONP and ONWL techniques, fabrication of devices and analysis of the data, and prepared the manuscript for the paper. T.-S.K. contributed to the fabrication of NW FETs and analysis of the chain orientation in ONWs using ultaviolet-visible and photoluminescence spectroscopy. B.J.K. and J.H.C. fabricated ion-gel-gated transistors and analysed the data. H.C. contributed to the fabrication of NW FETs and complementary inverters. H.Y. contributed to the analysis of the chain orientation in ONWs using GIXRD. Y.-Y.N. contributed to the fabrication of inverters. T.-W.L. initiated the research, designed all the experiments, analysed all the data and prepared the manuscript. All authors discussed the results and contributed to the paper.

Additional information

Supplementary Information accompanies this paper at http://www.nature.com/naturecommunications

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