Large Step Ratio Input-Series-Output-Parallel Chain-Link DC-DC Converter

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***Abstract*—High-voltage and high-power dc-dc conversion is key to dc transmission, distribution and generation, which require compact and efficient dc transformers with large step ratios. This paper introduces a dc-dc converter with the input-series-output-parallel (ISOP) arrangement of multiple high step ratio sub-converter units. Each sub-converter unit is an isolated modular dc-dc converter with a stack of half-bridge cells chopping the dc down to low voltage level. The transformer provides galvanic isolation and additional step ratio. The converter achieves a large step ratio due to the combination of the series-parallel configuration, the modular cells, and the isolation transformer. The proposed dc-dc converter is analyzed in a 30 kV to 1 kV, 1 MW application to discuss the operation performance, trade-offs, power efficiency and selection of components. Finally, the converter is validated through a laboratory down-scaled prototype.**

***Index Terms*—Large step ratio, medium voltage converter, dc transformer, modular multilevel converter.**

I. Introduction

VOLTAGE Source Converter (VSC) is considered as the suitable technology for the future HVDC applications, among which the modular multilevel converter (MMC) is the most promising architecture [1]–[5]. The MMC has a modular design using series-connected sub-modules (SMs) that form a stack to provide high voltage generating capability. Therefore, each stack can be operated as a controlled voltage source and the MMC can be implemented in high voltage dc-dc and dc-ac applications.

There are several applications of dc-dc converters in dc grids. The most common example is the point-to-point connection, where the dc-links are likely to operate at different voltage levels. Therefore, a dc transformer is required to connect them with relatively small voltage difference, providing a low step ratio on the dc voltage and full power capacity at high efficiency. Suitable converters, using a front-to-front arrangement of two VSCs linked by an ac transformer, have been discussed in [6]–[11]. The galvanic isolation can also be used to provide firewalling capabilities between two dc networks and isolate dc faults on one network to not affect the other [12]–[15]. Alternatively, using hybrid architectures with modular cells and switches are also proposed for low cost purpose, particularly suitable for interconnecting dc links with small voltage difference [16].

High voltage power systems have to feed medium or low voltage dc networks, and typically only require a fraction of the power rating of the high-voltage line, which is normally rated below 10% [17]. However, the converter must provide high step ratios of $10:1$ or more. Some topologies and general modular dc-dc converters have been proposed to address these challenges [18], [19]. Additionally, in some other applications such as offshore wind farms, the collector system can be done with pure dc-dc conversion [20]–[22]. These growing needs for high step ratio dc-dc conversion bring new challenges to the configuration and control of power electronics based system.

This paper proposes a large step ratio dc-dc converter topology composed of several medium power sub-converters connected in series-input-output-parallel (ISOP) configuration using isolation transformers. Each sub-converter is an isolated dc-dc converter with a MMC topology in the high voltage side and a bridge rectifier in the low voltage side. The MMC is a stack of half-bridge cells that generates a three level voltage under fixed frequency resonant operation mode, using phase-shift control to regulate the output voltage [23], [24]. Therefore, the step ratio in the sub-converter is achieved through three factors: the stack step ratio, the phase-shift modulation, and the turn ratio of isolation transformer. Moreover, the sub-converters are connected with the ISOP arrangement, which implements a large step ratio converter architecture. The following sections present the topology, the operation principle, the theoretical analysis, the converter application example and the laboratory scale prototype to validate the proposed converter.

II. Configuration of ISOP Chain-Link DC-DC Converter

This section presents the circuit configuration of the proposed converter and explains the sub-converter topology and the ISOP configuration. The proposed converter is conceived for HVDC tapping applications, which are normally rated below 10% of the link's power rating. Therefore, the entire converter will be considered as a VSC for the analysis.

A. Circuit Topology of Isolated Chain-Link DC-DC Converter

The basic step ratio of the proposed configuration is accomplished by sub-converter units. Each sub-converter has a stack

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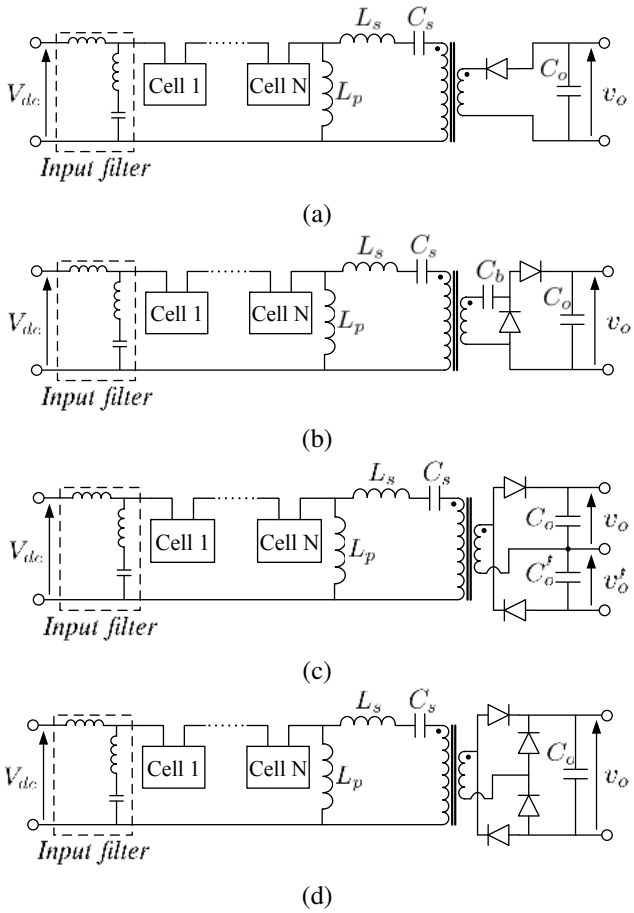


Fig. 1. Circuit topology of the N-cell isolated chain-link dc-dc converters with (a) half-wave rectifier. (b) voltage doubled half-wave rectifier. (c) half-bridge rectifier. (d) full-bridge rectifier.

of cells that supports high-voltage differences and provides excitation to a resonant tank connected to the transformer. A series-parallel resonant tanks is used where the resonance is between the series inductors L_s, series capacitors C_s and parallel inductors L_p (Fig. 1). The parallel inductor L_p can provide a path for the stack dc current flowing back to the high voltage side. On the other hand, the series capacitor can block any dc voltage component causing the isolation transformer saturation. These components are essential to guarantee the normal function of the sub-converter. The cells can be implemented by half or full bridges, or a combination of both types. The transformer isolates and steps down the voltage which output is rectified and filter by the output capacitor C_o. As a result, the output voltage v_o is stepped down from V_{dc} by the operation of chain-link stack, resonant tank and the isolation transformer. The selection of the rectifier topology depends on the requirement of the application. Fig. 1(a) shows a basic fly-back topology with a half-wave rectifier. Fig. 1(b) shows an additional diode-capacitor stage on the secondary side of the topology in Fig. 1(a). This gives a doubled dc output voltage v_o. Furthermore, the topology in Fig. 1(a) can be modified to have bipolar output, as is shown in Fig. 1(c). Finally, Fig. 1(d) shows the topology with full-wave rectifier, with reduced voltage and current stresses on the rectifier devices.

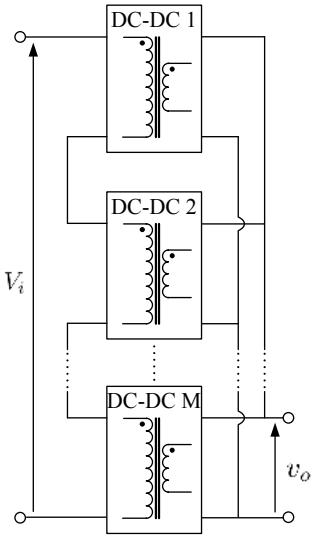


Fig. 2. Circuit configuration of the M-unit ISOP chain-link dc-dc converter.

B. Circuit topology of ISOP Connection of Sub-converters

The ISOP connection of the isolated sub-converters further increases the entire step ratio and power rating of the converter [25]. The circuit configuration of the ISOP connected sub-converters are shown in Fig. 2, where the isolated sub-converter unit illustrated in Fig. 1 is represented by a dc-dc converter block. There are M units in series-parallel connection in the entire converter. On top of the conversion ratio from a single sub-converter, the step ratio of the entire converter is multiplied by a factor of M.

C. Large Step Ratio of the Entire Converter

The large step ratio of the converter $\gamma_{\rm ISOP}$ is fulfilled by the series-parallel connection ratio M, the voltage ratio of the sub-converter stack cells γ_S, the resonant conversion step ratio γ_R, and the transformer voltage ratio γ_T:

$$\gamma_{\rm ISOP} = \gamma_S \gamma_R \gamma_T M. \tag{1}$$

The ISOP ratio M is the number of sub-converter units used. The stack voltage step γ_S is the ratio between V_{dc} and V_p, where V_p is the amplitude of the voltage across the parallel inductor v_p. The maximum step ratio of $\gamma_S = 2N - 1$ can be achieved by using two-level stack voltage modulation [26], which resonant operation also gives a step ratio of $\gamma_R = 1$. However, compared to the converter in [26], the proposed converter has a different arrangement of the resonant tank to guarantee normal operation of transformer. Moreover, with the modified modulation generating multilevel stack voltage, the step ratio of γ_S is different. The step ratio γ_R can also be regulated by the pulse width of the stack voltage [27].

III. Operation Principal and Step Ratio of Chian-Link DC-DC Sub-Converter Unit

A. Fixed Frequency Modulation of Chain-Link DC-DC Sub-Converter Unit

Modulation and control of the chain-link can determine the operation mode of the sub-converter unit, achieving a flexible

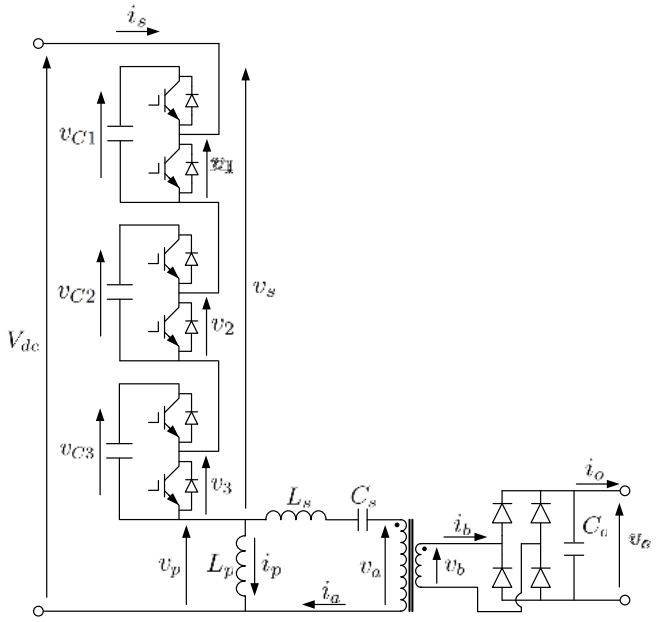


Fig. 3. Circuit diagram of the three-cell chain-link dc-dc sub-converter.

step ratio. Although there could be many control schemes, the fixed-frequency series-parallel resonant operation with fixed voltage levels is demonstrated in this paper.

The control method generating drive signals is demonstrated based on a sub-converter unit with three cells and a full-wave rectifier. The circuit diagram of the sub-converter unit is shown in Fig. 3.

For the sub-converter unit in Fig. 3, the stack operates with a three-level voltage. The general voltage waveforms of the three-cell converter in time-domain is shown in Fig. 4. In one switching cycle T_s, each cell output voltage has two "one states" with the cell's upper switch turned on and two "zero states" with the cell's lower switch turned on. The voltage waveforms of the cells v_1, v_2, and v_3 are phase-shifted by $120°$. This results in a stack voltage v_s with tripled ripple frequency. The transformer voltage on the primary side v_a is therefore obtained by deducting v_s from V_{dc}. The equivalent operating cycle T_e of v_a is a third of the cycle T_s.

The fixed-frequency phase-shift gating scheme is used for power regulation. By regulating the time duration of "one states" of v_1, v_2, and v_3 in Fig. 4, the pulse width of v_s can be controlled. If the difference between the time durations of two adjacent "one states" is increased, the pulse width of v_s will be increased. The maximum pulse width that v_s can achieve is shown in Fig. 5, where v_s is almost a two-level voltage with two cell capacitor voltages swing. This modulation waveform gives the maximum power to the low voltage side. The equivalent operating cycle is still the same as that in Fig. 4.

To reduce the pulse width of v_s, the difference between time durations of the two adjacent "one states" of v_1, v_2, and v_3 has to be reduced. The minimum pulse width of v_s and v_p is obtained when time durations of the two "one states" of each cell output voltage has negligible difference. The time-domain voltage waveforms of the three-cell converter is shown in Fig. 6. In that case, the power transmitted to the low voltage side is minimized.

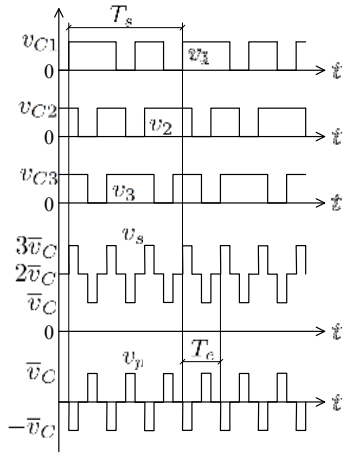


Fig. 4. The general time-domain voltage waveforms of the three-cell chain-link dc-dc converters.

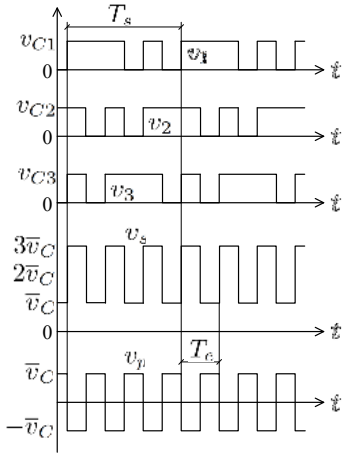


Fig. 5. Time-domain voltage waveforms of the three-cell chain-link dc-dc converters with maximum pulse width.

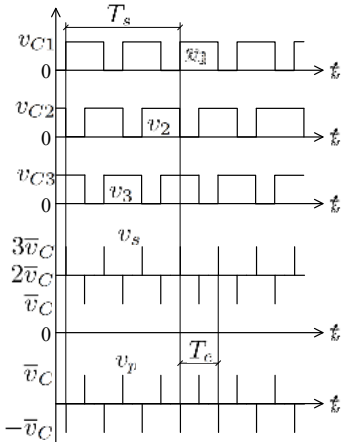


Fig. 6. Time-domain voltage waveforms of the three-cell chain-link dc-dc converters with minimum pulse width.

The "zero states" of v_1, v_2, and v_3 in Fig. 4, Fig. 5, and

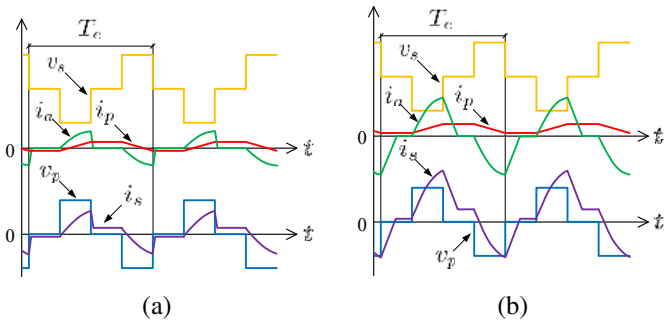


Fig. 7. Time-domain key waveforms of the converter with (a) a light load and (b) a heavy load.

Fig. 6 are all keeping the fixed time duration. Under all circumstances with different pulse width, the cell capacitors join and quit the operation following a uniform sequence. As the amplitude V_p is related to the output voltage directly, each cell capacitor voltage is clamped by V_p. Therefore, the inherent-balancing of the SM capacitors in a sub-converter unit is achieved. The detailed analysis will be presented in the following subsections.

B. Resonant Operation of Chain-Link Unit with Fixed Frequency

The equivalent operating frequency of the sub-converter unit is selected to be close to the resonant frequency. The fixed frequency resonant operation of the chain-link unit is analyzed in this subsection.

The time-domain voltage waveform in Fig. 4 is used as a general case. The stack voltage v_s of the sub-converter unit results in a three-level ac voltage v_a on the parallel inductor L_p. The parallel current i_p has a trapezoidal waveshape with equivalent cycle T_e. The current i_p rises when $v_p > 0$ and falls when $v_p < 0$. It has a flat slope when $v_p = 0$. The average value of i_p depends on the dc input power of the unit. If the load current is low, the dc component of i_p is close to zero. Fig. 7(a) shows the voltage and current waveforms of a sub-converter unit with a light load. The transformer primary side current i_a has a resonant waveshape. If the voltage v_p is a two-level square wave, the current i_a is completely sinusoidal. With fixed frequency modulation, the pulse width of v_p is adjusted. When v_p reaches zero, i_a is forced to zero. As a result, the waveform of i_a can be obtained as shown in Fig. 7(a). Therefore, the stack current i_s is a sum of i_a and i_p, which is also shown in Fig. 7(a).

If the load current is high, the parallel current i_p has a higher average value but keeps the same ac amplitude. However, owing to the high power transmitted, i_a has a high amplitude as well. This results in a stack current i_s with higher dc and ac components. The voltage and current waveforms of the sub-converter unit with a heavy load can be observed in Fig. 7(b).

C. Step Ratio Analysis

To study the step ratio of the sub-converter unit, the voltage on the resonant capacitor C_s is defined as v_r. The current i_a and the voltage v_r in the resonant tank can be written as

$$\frac{d}{dt}\begin{bmatrix} i_a(t) \\ v_r(t) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_s} \\ \frac{1}{C_s} & 0 \end{bmatrix}\begin{bmatrix} i_a(t) \\ v_r(t) \end{bmatrix} + \begin{bmatrix} \frac{V_p - V_a}{L_s} \\ 0 \end{bmatrix}. \quad (2)$$

At the time t_0 when i_a starts to resonate, the value of i_a is equal to zero (Fig. 7). This resonant operation terminates at the time t_1 when v_p falls to zero. As a result, the initial condition for this system is $i_a(t_0) = 0$ and $v_r(t_0)$, where V_a is the voltage amplitude of primary side of the transformer. Hence, the time-domain current and voltage from t_0 to t_1 can be derived as

$$i_a(t) = \frac{V_p - V_a - v_r(t_0)}{Z_0}\sin\omega(t - t_0) \quad (3)$$

and

$$v_r(t) = (V_p - V_a)(1 - \cos\omega(t - t_0)) + v_r(t_0)\cos\omega(t - t_0) \quad (4)$$

with $Z_0 = \sqrt{L_s/C_s}$ and $\omega = 1/\sqrt{L_sC_s}$ the characteristic impedance and angular frequency of the resonant tank, respectively. From t_0 to t_1, the average power flowing into the resonant tank over an operating cycle can be derived as

$$P_1 = \frac{V_p(V_p - V_a - v_r(t_0))}{\pi Z_0}(1 - \cos\alpha) \quad (5)$$

with α varying from 0 to π radians to represent the pulse width of v_p. After t_1, the voltage v_p equals to zero while the current i_a still resonates until it reaches zero at the time instant t_2. According to (2), with the initial conditions of $i_a(t_1)$ and $v_r(t_1)$. The time-domain current and voltage from t_1 to t_2 are written as

$$i_a(t) = i(t_1)\cos\omega(t - t_1) - \frac{v_r(t_1) + V_a}{Z_0}\sin\omega(t - t_1) \quad (6)$$

and

$$\begin{aligned} v_r(t) = &- V_a(1 - \cos\omega(t - t_1)) + v_r(t_1)\cos\omega(t - t_1) \\ &+ i_a(t_1)Z_0\sin\omega(t - t_1). \end{aligned} \quad (7)$$

The power flowing into the resonant tank from t_1 to t_2 averaged over an operating cycle can be derived as

$$\begin{aligned} P_2 = &\frac{V_p(V_p - V_a - v_r(t_0))[\cos\alpha - \cos(\alpha + \beta)]}{\pi Z_0} \\ &+ \frac{V_p^2(\cos\beta - 1)}{\pi Z_0} \end{aligned} \quad (8)$$

with $\beta = (t_2 - t_1)/\pi$. Hence, the total power flowing into the resonant tank can be obtained as

$$\begin{aligned} P = &\frac{V_p(V_p - V_a - v_r(t_0))[1 - \cos(\alpha + \beta)]}{\pi Z_0} \\ &+ \frac{V_p^2(\cos\beta - 1)}{\pi Z_0}. \end{aligned} \quad (9)$$

To simplify the analysis, the converter is assumed to be lossless. The power flowing into the resonant tank is equal to the output power, yielding

$$P = \frac{V_o^2}{R}. \quad (10)$$

The transformer step ratio is $\gamma_T = V_a/V_o$ and the step ratio of resonant conversion is $\gamma_R = V_p/V_a$. By substituting

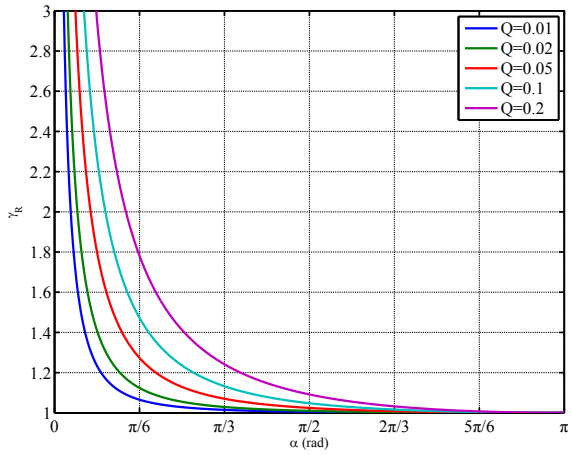


Fig. 8. Regulation of resonant conversion ratio γ_R under different quality factors.

$i_a(t_2) = 0$ and $v_r(t_2) = -v_r(t_0)$ into (6) and (7), respectively, with the elimination of $v_r(t_0)$ by combining (9) and (10), the step ratio of resonant conversion γ_R can be obtained as

$$\begin{bmatrix} \cos(\alpha+\beta) & -\cos(\beta) \\ \sin(\alpha+\beta) & -\sin(\beta) \end{bmatrix} \begin{bmatrix} \gamma_R^2 - \gamma_R + \frac{Q}{2} \\ \gamma_R^2 \end{bmatrix} = \begin{bmatrix} -\frac{Q}{2} - \gamma_R \\ 0 \end{bmatrix} \tag{11}$$

with $Q = \frac{\pi Z_0}{\gamma_T^2 R}$ the quality factor. The change of γ_R versus the pulse width of v_s under different quality factors is shown in Fig.8. It can be seen that a flexible step ratio γ_R can be achieved by adjusting the pulse width of v_s, i.e., regulating α from 0 to π.

Moreover, with a larger Q, the step ratio γ_R has a lower sensitivity versus the variance of α. As a result, a small Z_0 will be more applicable to meet the voltage regulation requirement with intensive load change.

On the other hand, a smaller characteristic impedance will result in a larger resonant current i_a (according to (3)), which increases unnecessary losses in the resonant tank. The selection of Z_0 should also take the transformer turn ratio into account to achieve the entire required step ratio. The detailed design of the dc-dc converter will be presented in next section.

IV. Large Step Ratio Conversion of ISOP Chain-Link DC-DC Converter

In order to achieve large step ratio dc-dc conversion, different configuration options can be used. In this section, the application of a 30 kV to 1 kV, 1 MW dc-dc converter is demonstrated and the trade-offs between two different configurations are discussed.

A. Selection of Series-Parallel Units and Sub-Modules

A step-down ratio of $\gamma_{\text{ISOP}} = 30$ from the high voltage dc to the low voltage dc is required. Taking the voltage and current ratings in commercial power devices into account, the series-parallel units and bridge modules should be capable of withstanding the high voltage dc. For an N-cell chain-link dc-dc converter illustrated in Fig. 3, the average dc voltage of v_s is equal to $(N-1)\overline{v}_C$. Hence, the cell capacitor voltage is written as $\overline{v}_C = V_{dc}/(N-1)$. The voltage amplitude V_p is equal to $\overline{v_C}$, yielding the stack step ratio of the N-cell chain-link

$$\gamma_s = N - 1. \tag{12}$$

For M units connected in input-series-output-parallel manner, the dc voltage across the sub-converter unit is

$$V_{dc} = \frac{V_i}{M}. \tag{13}$$

Therefore, the voltage across a single switch is observed by the cell capacitor voltage, namely

$$\overline{v}_C = \frac{V_i}{M(N-1)}. \tag{14}$$

It can be seen from (14) that with larger numbers of M and N, the switch voltage stress is lower. However, a high conversion ratio of γ_S may result in a high current flowing through the stack. This increases the current stress and semiconductor losses, leading to a lower conversion efficiency. To reduce the conversion losses, the cell number N is usually selected to be small to achieve a low γ_S.

The step-down ratio and voltage stress of the available configurations of the series-parallel sub-converter units and cells are listed in Table I. The configuration of $N = 3$ and $M = 6$ is used, based on which the transformer turn ratio is selected.

TABLE I
Configuration of the ISOP DC-DC Converter

N	M	$\gamma_S M$	V_C	Total cell number
3	6	12	2.5 kV	18
4	4	12	2.5 kV	16
5	3	12	2.5 kV	15
6	2	10	3.0 kV	12
7	2	12	2.5 kV	14

B. Step Ratio of the Resonant Tank and Isolation Transformer

The step ratio of the sub-converter unit is dependent on stack step ratio γ_S, the turn-ratio γ_T of the transformer and the resonant conversion ratio γ_R. Assume that the chain-link voltage v_s is controlled to step between $N-2$ levels to N levels with the equivalent operating frequency f_e. If the resonant frequency of the resonant tank is equal to the equivalent frequency,

$$f_e = \frac{1}{2\pi\sqrt{L_s C_s}}. \tag{15}$$

It can be seen that with higher equivalent operating frequency, the inductance and capacitance in the resonant tank will decrease. The volume of the passive components in the converter can be reduced with a slight sacrifice on switching losses.

The isolation transformer affects the total step ratio γ_{ISOP}. With a larger transformer turn ratio γ_T, a higher step ratio of the sub-converter unit can be achieved. However, high insulation grade and coupling coefficient may result in low efficiency and large volume of the transformer. Meanwhile,

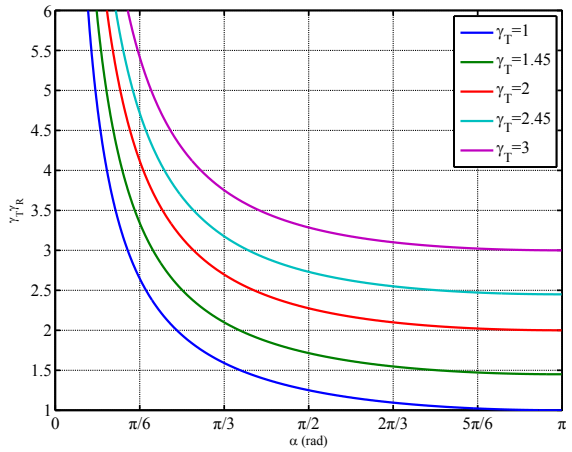


Fig. 9. Step-down ratio of the resonant tank and isolation transformer.

TABLE II
CURRENT STRESS VERSUS TRANSFORMER TURN RATIO

Turn ratio	1.0	1.45	2.0	2.45
Current stress	488 A	380 A	262 A	105 A

the turn ratio γ_T needs to have a appropriate value for the output voltage being in an adjustable range to meet the voltage regulation requirement. To achieve the given step-down ratio $\gamma_{\text{ISOP}} = 30$, apart from the step ratio of the chain-link stack and series-parallel configuration ($\gamma_S M = 12$), an extra adjustable step-down ratio of $\gamma_T \gamma_R = 2.5$ should be achieved by the conversion.

Fig.9 illustrates the step-down ratio of the resonant conversion with different transformer turn ratios. It can be seen that with the turn ratio higher than 3, the step ratio $\gamma_T \gamma_R$ is always above 2.5. Therefore, the transformer turn ratio is chosen to be lower than 3 to achieve the required entire step ratio $\gamma_{\text{ISOP}} = 30$.

Moreover, the pulse width of v_p is regulated to achieve the required $\gamma_T \gamma_R$. The variable α needs to increase from 0.18π to 0.78π when the turn ratio ranges from 1 to 2.45. Table II lists the current stresses of the switches with different transformer turn ratio while $\gamma_T \gamma_R = 2.5$. It can be seen that a larger turn ratio of transformer can mitigate the current stress. On the other hand, owing to the available isolation transformer in the experimental test, the turn ratio of $\gamma_T = 2.45$ is selected.

For multiple sub-converter units with high voltage dc sides connected in series, the input current flowing through all units is unique. The sub-converter units should be controlled to have the same voltage step ratios. As the low voltage dc sides of the sub-converter units are connected together with the same voltage, there dc voltages V_{dc}^k $(k = 1, 2, ..., M)$ on the high voltage sides are almost equal. The input high voltage V_i are therefore uniformly spread on the high voltage sides of the sub-converter units. With the unique input current, thanks to the regularity of the step ratio γ_U of the series-parallel units, a balanced input power is guaranteed.

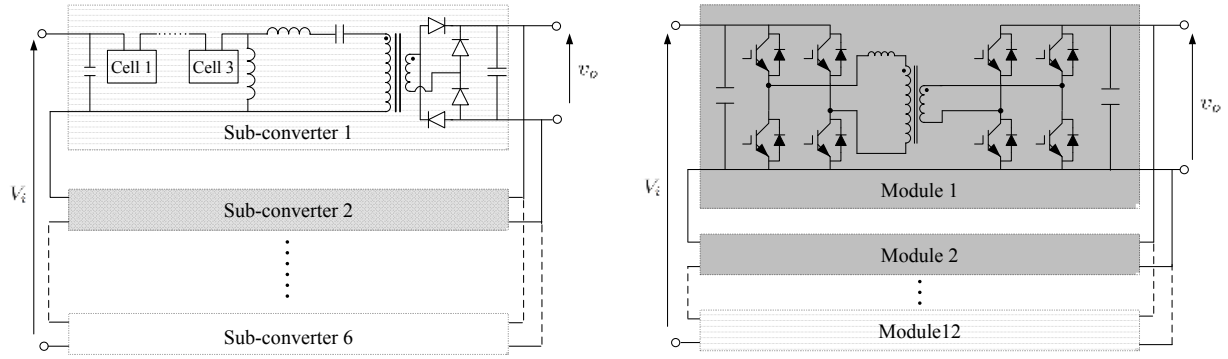
TABLE III
COMPARISON OF THE CONVERTER SCHEMES

	Proposed Scheme	ISOP DAB Scheme
Number of series-parallel modules	6	12
Number of 5SNG 0150P450300	36	48
Voltage stress on 5SNG 0150P450300	2500 V	2500 V
Current stress on 5SNG 0150P450300	137 A	84 A
Number of 5SDA 11D1702	24	0
Voltage stress on 5SDA 11D1702	1000 V	N/A
Current stress on 5SDA 11D1702	260 A	N/A
Number of 5SNG 0300Q170300	0	48
Voltage stress on 5SNG 0300Q170300	N/A	1000 V
Current stress on 5SNG 0300Q170300	N/A	209 A
Number of transformers	6	12
Transformer turn ratio	2.45	2.45
Number of HV side capacitors	6	12
Number of LV side capacitors	6	12
Number of series capacitors	24	0
Number of series inductors	6	12
Power losses	14766 W	9368 W
Efficiency	98.5%	99.1%

C. Comparison of Converter Schemes

This subsection shows the comparison of two converter schemes for the high voltage high step ratio application. The common ISOP architecture with multiple dual-active-bridges (DABs) are used [28], [29]. The proposed ISOP chain-link converter and the conventional ISOP DAB converter with phase-shift control are studied and compared. Both systems step down the dc voltage from 30 kV to 1 kV with the power rating of 1 MW. The ISOP chain-link converter consists of six sub-converters with three cells in each sub-converter, whereas the ISOP DAB converter has twelve isolated modules with series-parallel connection. The circuit configurations of the two converter schemes are shown in Fig. 10. In order to achieve the step down dc-dc conversion requirement, the detailed parameters of the two converter schemes are listed in Table III.

For the proposed ISOP chain-link converter, there are 18 cells in total. As a result, there are 36 IGBTs (ABB 5SNG 0150P450300) used on the high voltage side and 24 diodes (ABB 5SDA 11D1702) used on the low voltage side. In contrast, the ISOP DAB topology has 12 DAB modules connected in series-parallel arrangement. There are 48 IGBTs (ABB 5SNG 0150P450300) used on the high voltage side and 48 IGBTs (ABB 5SNG 0300Q170300) on the low voltage side. The turn-ratio of the transformers in the two schemes are the same. According to the operation and performance, the voltage and current stresses and losses are calculated. These results are also compared as shown in Table III. It can be seen that under the same voltage rating condition, the current rating of the high voltage side IGBTs in the proposed converter is higher than that of the ISOP DAB converter. However, the number of the IGBTs used in the proposed converter is relatively lower. Hence, with less IGBTs and series-parallel units, the proposed topology has advantages over the conventional DAB topology in terms of the cost and complexity. Moreover, involving less active switches and isolation transformers can lower the failure rate of the entire system which achieves more reliable



(a) (b)

Fig. 10. Circuit configurations of the two converter schemes for comparison. (a) Proposed ISOP chain-link converter. (b) Conventional ISOP DAB converter.

TABLE IV
EXPERIMENTAL PARAMETERS

Symbol	Description	Value
V_i	Nominal input dc voltage	1000 V
V_o	Nominal output voltage	100 V
L_p	Parallel inductor	3310 μH
L_s	Series inductor	165 μH
C_s	Series capacitor	50 μF
L_a	Primary side leakage inductor	50 μH
L_b	Secondary side leakage inductor	8 μH
L_m	Magnetizing inductor	460 mH
C_o	Output capacitor	250 μF
C_{dc1}, C_{dc2}	Converter input side capacitor	550 μF

operation.

On the other hand, the total conduction losses in the ISOP DAB converter are lower than that of the proposed ISOP chain-link converter. Moreover, the chain-link converter archives zero-voltage-switching (ZVS). In contrast, each DAB converter achieves ZVS and zero-current-switching (ZCS). The ISOP DAB converter achieves a high efficiency of 99.1% while the efficiency of the proposed converter is 98.5%.

According to the comparison result, although the ISOP DAB converter has some advantages over the proposed converter in low voltage applications, when the dc voltage is increased to a certain high level, the complexity of the ISOP DAB converter may result in incompetence in higher voltage applications. In that case, the proposed converter will turn into a good trade-off. Hence, the proposed ISOP chain-link converter is preferable in high voltage, high step ratio applications. However, when it comes to low voltage, low step-ratio applications, ISOP DAB converter may be a better choice.

V. EXPERIMENTAL RESULTS

A down-scaled experimental prototype with two sub-converter units in series-parallel connection was built to demonstrate the operation. Each sub-converter unit has three sub-modules so in total there are six half bridges. A digital signal processor and an FPGA were deployed to control the converter. The sub-modules were implemented using capacitors with a nominal capacitance value of 50 μF. A series inductor and a series capacitor is placed between the parallel inductor and the rectifier. The isolation transformer has a measured step ratio of 2.45. A 15 Ω resistive load was connected at the low voltage dc side. The detailed prototype parameters are listed in Table IV. The magnetizing inductance is very large compared to the parallel inductance. As a result, the affect of the magnetizing inductor to the resonant operation is negligible.

The operation of the ISOP chain-link dc-dc converter is demonstrated with the pulse width conditions of $\alpha = \pi/5$, $\alpha = 3\pi/5$, and $\alpha = \pi$. The Experimental waveforms of the required sub-module output voltages and stack voltage of Unit 1 are shown in Fig. 11. With well controlled logic sequences, each sub-converter unit is realizing theoretical waveforms in Fig. 4 and Fig. 5. The pulse widths of v_s is adjusted regularly with the change of the control reference.

The currents flowing through the stacks and parallel inductors of the sub-converters are shown in Fig. 12. When the factor α is low, the resonant tank currents have a long time duration for discontinuous conducting. Meanwhile, the stack peak currents are high and the parallel inductor currents have a trapezoidal waveshape, (Fig. 12(a)). When α increases, the stack current stress reduces and the parallel inductor currents exhibit a longer rising and falling edge (Fig. 12(b)). It can be seen from Fig. 12(c) that when $\alpha = \pi$, the parallel inductor current in each sub-converter turns into a triangle waveshape. The stack current is a sum of the triangle parallel inductor current and the full wave resonant tank current.

The stack voltages and currents of the two sub-converter units are shown in Fig. 13. The experimental waveforms of the two units are interleaved uniformly. It can be observed from Fig. 13 (a) that during the time when v_{s1} and v_{s2} overlap, the stack currents are almost constant. When the pulse width increases, the stack currents have a longer time duration for resonating (Fig. 13 (b)). Meanwhile, the stack current amplitudes decrease as well. For the complete square waves of v_{s1} and v_{s2} (Fig. 13 (c)), the stack currents are fully resonating in the entire operating cycle. Under all conditions of α, the stack voltages as well as the stack currents in the two units are sharing the same amplitudes.

Fig. 14 shows the experimental waveforms of the parallel inductor voltages and stack currents of the two units. The parallel inductor voltages are complementary to the stack voltages. However, the average voltages of v_{p1} and v_{p2} are

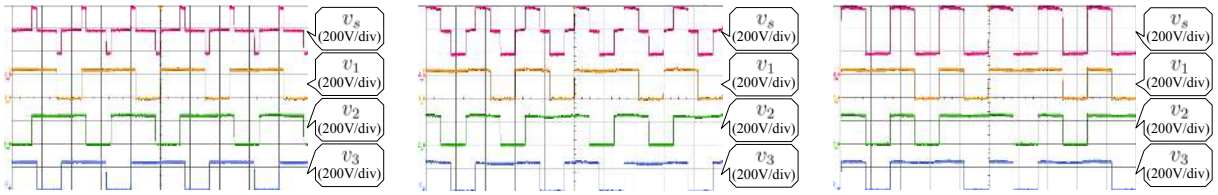


Fig. 11. Experimental waveforms of the sub-module output voltages and stack voltage in Unit 1 (X–axis: Time, 200 μs/div; Y–axis: Magnitude of voltages, 200 V/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

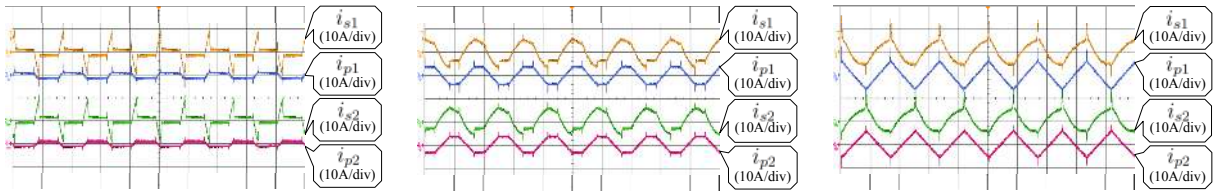


Fig. 12. Experimental waveforms of the stack currents and parallel inductor currents. (X–axis: Time, 200 μs/div; Y–axis: Magnitude of currents, 10 A/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

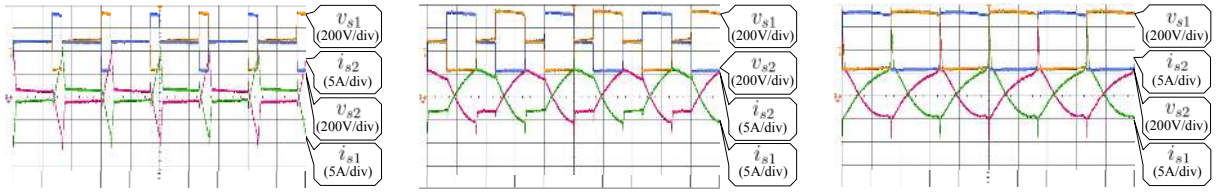


Fig. 13. Experimental waveforms of the stack voltages and stack currents in the two units (X–axis: Time, 100 μs/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

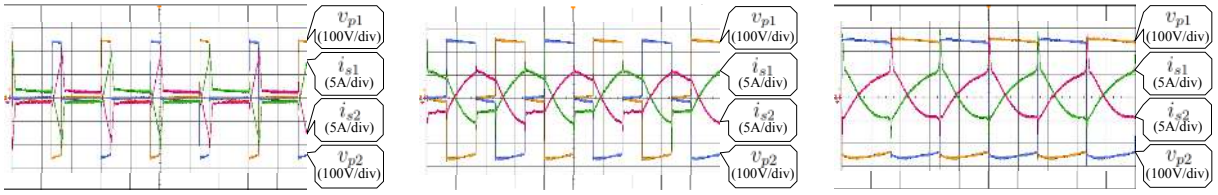


Fig. 14. Experimental waveforms of the parallel inductor voltages and stack currents in the two units (X–axis: Time, 100 μs/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

zero. With a small pulse width of parallel inductor voltage, the stack current has higher rising slope. The voltages v_{p1} and v_{p2} together with ac components of i_{s1} and i_{s2} determine the power transferred to the low voltage side. With well tuned step ratios of the two units, the parallel inductor voltages as well as the stack currents have the same amplitudes. A balanced power between the two units is achieved. Moreover, it can be seen that v_{p1} and v_{p2} drop slightly when they overlap. This is because the cell capacitors have a limited capacitance. The impact on current waveform is significant when $\alpha = 3\pi/5$. As the time duration of v_{p1} and v_{p2} overlapping is long, the parallel inductor current is prominent resulting an unsymmetrical stack current waveform.

Fig. 15 shows the experimental voltage and current waveforms on the primary sides of the isolation transformers. When α is small, the discontinuous resonant currents have a high peak value (Fig. 15(a)). The primary side voltage v_{a1} and v_{a2} share the same peak value. The peak value of the voltage is relatively low as the sub-converters achieve a high step ratio. When $\alpha = 3\pi/5$, the step ratio decreases and the primary side voltage v_{a1} and v_{a2} share a higher peak value, as is shown in Fig. 15(b). Due to the junction capacitors of the rectifier, the voltage resonance appears during discontinuous conduction time. Such resonance disappears when $\alpha = \pi$ (Fig. 15(c)). The primary side voltage v_{a1} and v_{a2} are square waves with the same peak value. The transformer input currents are close to sinusoidal waveforms. It can be observed that the transformer input currents are also well shared.

Fig. 16 shows the experimental voltage and current waveforms on the secondary sides of the isolation transformers.

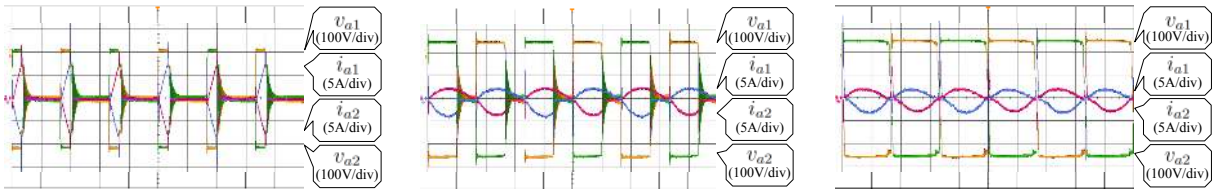


Fig. 15. Experimental waveforms of the transformer primary side voltages and currents in the two units (X–axis: Time, 100 μs/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

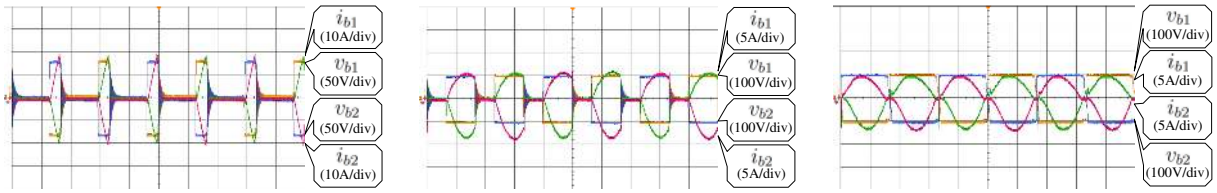


Fig. 16. Experimental waveforms of the transformer secondary side voltages and currents in the two units (X–axis: Time, 100 μs/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

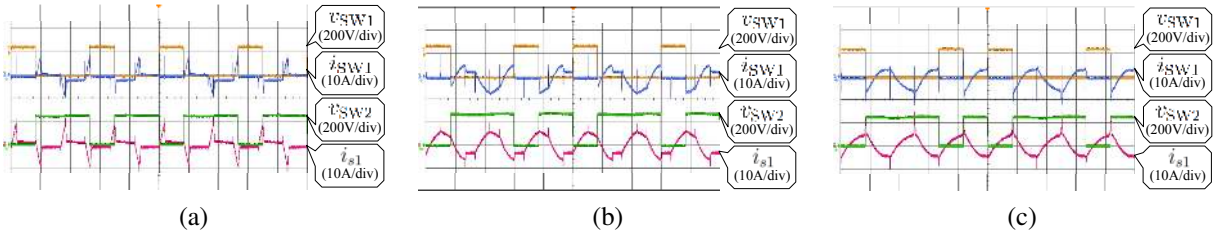


Fig. 17. Experimental waveforms of the switch voltages and currents in the cell (X–axis: Time, 200 μs/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

When $\alpha = \pi/5$, the transformer secondary side voltages have a narrow pulse width and the currents are highly discontinuous (Fig. 16(a)). When $\alpha = 3\pi/5$, the secondary side voltages v_{b1} and v_{b2} have wider pulse width and share the same amplitude. Meanwhile, the secondary side currents i_{b1} and i_{b2} have a discontinuous resonant waveshape, as is shown in Fig. 16(b). When α reaches the maximum value π, the voltages v_{b1} and v_{b2} turns into square waves. The currents i_{b1} and i_{b2} are close to sinusoidal waveforms (Fig. 16(c)). The voltages and currents of the transformer secondary sides are equally shared between the sub-converters.

Fig. 17 shows the experimental waveforms of the two switches in a cell. The upper traces show the upper switch voltage and upper switch current of the cell. The lower traces show the lower switch voltage and the stack current. It can be seen from Fig. 17 that under different values of α, the upper switch and lower switch of the cell achieve ZVS. However, the turn-off currents in the switches are positive.

The experimental efficiency results versus the pulse width is shown in Fig. 18. Under general power level, the maximum efficiency is achieved when α is close to $\pi/2$. Moreover, it can be seen from Fig. 18 that when the operating power increases, the utilization of the devices in the converter is improved. As a result, a higher efficiency is achieved. Owning to the limitation of experimental power source, the operating power is not high enough to reach the highest approachable

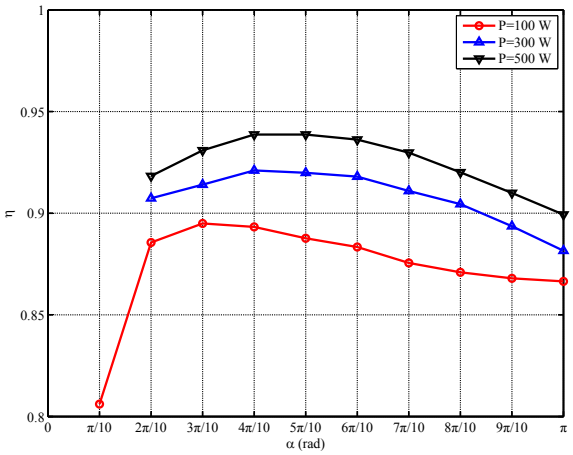


Fig. 18. Experimental efficiency when α varies.

efficiency. However, when the power level increases and the devices are well utilized, a good trade-off between conversion ratio and efficiency can be obtained.

The experimental efficiency of the entire dc-dc converter versus the input high voltage is shown in Fig. 19. The efficiencies are measured under different values of α. It can be seen from Fig. 19 that when the input voltage increases, the efficiency is improved. This is achieved by a better utilization

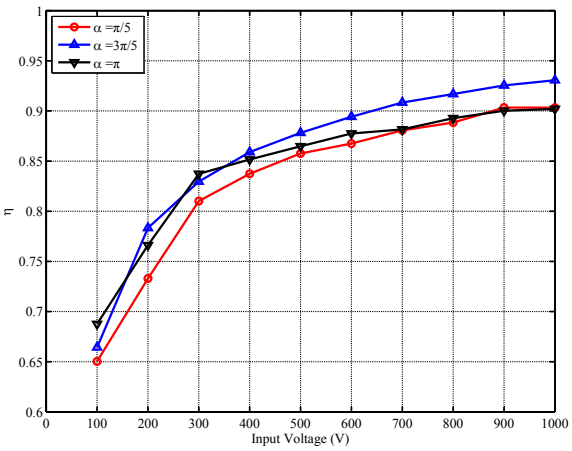


Fig. 19. Experimental efficiency versus the input high voltage.

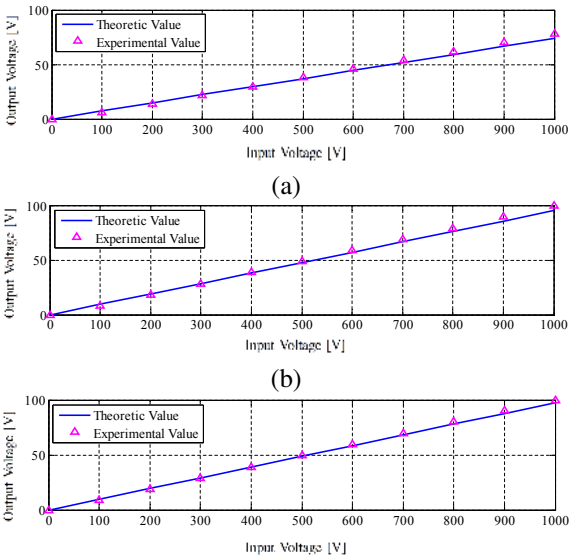


Fig. 20. Experimentally measured output voltages versus input voltages (X–axis: Time, 100 μs/div) with (a) $\alpha = \pi/5$. (b) $\alpha = 3\pi/5$. (c) $\alpha = \pi$.

of the devices in the converter. With increased voltage level, the experimental efficiency which is even higher than the measured values can be achieved. Compared to the traditional DAB scheme [30] where the maximum efficiency is achieved in the middle of the input voltage range, the proposed converter achieves the highest efficiency within high input voltage range. The proposed converter is more suitable for high voltage large step ratio application.

The step ratios were experimentally verified by measuring the output voltage of the converter versus the input voltage. The results are shown in Fig. 20. The experimental results are in good accordance with the theoretical results under different α conditions. The theoretic analysis of the step ratio has been validated. As analyzed previously, when $\alpha = 3\pi/5$ and $\alpha = \pi$, the output voltage has small difference. Significant output voltage decrease happens when α decreases to $\alpha = \pi/5$. The step ratio of the converter can be regulated by changing the pulse width α.

The voltages on cell capacitors and the sub-converter unit

TABLE V
CAPACITOR VOLTAGES

	Voltages in Unit 1 (V)				Voltages in Unit 2 (V)			
α	V_{dc1}	V_{C1}	V_{C2}	V_{C3}	V_{dc2}	V_{C1}	V_{C2}	V_{C3}
$\frac{\pi}{5}$	500	249	250	249	500	249	249	249
$\frac{3\pi}{5}$	499	249	249	249	500	250	250	250
π	499	248	249	248	500	249	249	249

input side capacitors are measured and listed in Table V. It can be seen that the voltages are well balanced. Thanks to the consistency of the step ratios of the sub-converter units, a good balancing is guaranteed.

The ISOP MMC dc-dc converter is a combination of chain-link converter and ISOP converter. It uses several ISOP sub-converter units with relative low voltage on each isolation transformer. The low number of series-parallel units can reduce the control complexity of the system. Although in most medium voltage applications either ISOP converter or traditional chain-link converter can be the good solution, for some applications the proposed ISOP chain-link dc-dc converter is a good trade-off option. It merges the merits of the two conventional schemes such as modularity, simplicity and good balancing ability for high step ratio application, but without bringing huge disadvantages from those schemes.

VI. CONCLUSION

This paper presents an ISOP chain-link converter for large step-down ratio dc-dc conversion. The converter has multiple identical sub-converter units connected in series-parallel arrangement. Each unit is an MMC-style isolated dc-dc converter. Fixed frequency modulation with three voltage levels are used for resonant conversion. The conversion ratio is a product of the sub-converter unit number, stack step ratio, transformer turn ratio and the resonant conversion ratio. As a result, a high total step ratio can be achieved. The resonant step ratio can be regulated to balance the step ratio of the sub-converter units. The operation of the converter has been demonstrated by an 1 kV laboratory scale prototype with a total step ratio of ten. The prototype tests have verified the operation of the converter and the accuracy of the theoretical step ratio. The cell capacitor voltages are inherently balanced and the power of the units are also well balanced in the tests. This converter can be used as a large step ratio high voltage tap.

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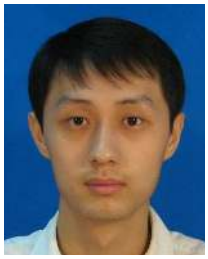

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