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Laser Fault Injection into SRAM cells: Picosecond versus Nanosecond pulses

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***Abstract*—Laser fault injection into SRAM cells is a widely used technique to perform fault attacks. In previous works, Roscian and Sarafianos studied the relations between the layout of the cell, its different laser-sensitive areas and their associated fault model using 50 ns duration laser pulses. In this paper, we report similar experiments carried out using shorter laser pulses (30 ps duration instead of 50 ns). Laser-sensitive areas that did not appear at 50 ns were observed. Additionally, these experiments confirmed the validity of the bit-set/bit-reset fault model over the bit-flip one. We also propose an upgrade of the simulation model they used to take into account laser pulses in the picosecond range. Finally, we performed additional laser fault injection experiments on the RAM memory of a microcontroller to validate the previous results.**

I. Introduction

Fault attacks are a subset of the wide array of physical attacks existing against secure circuits. Their goal is to disturb a circuit and then to exploit the resulting computation errors. Perturbations can be induced by different means: optical attacks [1], voltage [2] and clock glitches [3], electromagnetic pulses, etc.

Methods such as Differential Fault Analysis (DFA) [4]–[7] use the differences between the faulted and correct outputs of encryption algorithms to recover the encryption keys. The success and efficiency of the DFA is highly dependent on the fault model [8], as such, knowing that a specific fault model is relevant and usable for a given target is important. Faults injected into memory cells are usually modeled using either the bit-set/bit-reset or the bit-flip fault model. A bit-set is the case where the cell state is changed from "0" towards "1" but unchanged if the cell state is already "0", while a bit-reset is the case where the cell state is changed from "1" towards "0" but unchanged if the cell state is already "1". In the case of a bit-flip, the cell state is inverted (i.e. flipped) regardless of its initial state.

In previous works, Sarafianos et al. [9] and Roscian et al. [10] both studied the fault models that apply to SRAM cells for laser-induced faults. They drew maps of the laser-sensitive areas of a 5 transistors SRAM cell using a 50 ns laser pulse duration. It showed that one of the theoretical sensitive areas was hidden and did not allow to inject faults. They also came to the conclusion that the bit-set/bit-reset fault model is the relevant one as they did not obtain any bit-flip type fault. They also validated their results through simulation using the electrical model of transistors exposed to laser stimulation described in [9], [11], [12]. Finally, they obtained further validation of their results by performing fault injection experiments on the RAM memory of a microcontroller.

Having a robust simulation model to anticipate the behavior of a chip when submitted to fault injection attempts may permit to reveal a security weakness before actual production (hence saving the cost and time of a redesign).

In this paper, we report similar experiments carried out with 30 ps laser pulses. It revealed a laser-sensitive area which was masked at 50 ns laser pulse duration. We also confirmed the relevance of the bit-set/bit-reset fault model. These results are backed by experimental results obtained on a dedicated SRAM prototype and on the RAM memory of a microcontroller. We then improved the simulation model to fit with our new results. Note that a nanosecond range pulse duration is common for hardware security testing, whereas a picosecond range duration is mandatory for emulating radiation effects caused by ionizing particles [13].

This article is organized as follows: First, we remind the mechanisms of laser fault injection, going from a PN-junction to a SRAM cell. Second, we review the results of previous works. Third, we present our experimental results and work in designing a simulation model. Finally, we draw a conclusion.

II. Laser Fault Injection Mechanism

A. Physical Phenomenon

Laser fault injection is achieved using the photoelectric effect [14]. When a laser beam passes through silicon, if the photon energy is greater than the band-gap of the silicon, electron-hole pairs are created. In most cases, the pairs then just recombine and nothing happens. However, when the laser beam is targeted at a PN-junction, electrons and holes are drifted in opposite directions by the PN-junction electrical field, thus creating a transient current across the junction.

The phenomenon happens in three phases highlighted in figure 1:

1) Charges are created along the path of the beam,
2) Charges are drifted away by the PN-junction electric field, stretching the depletion region along the laser beam path. The charges nearby are then promptly collected, creating a current spike,
3) The remaining charges are then slowly collected in a diffusion phase: the current magnitude decreases slowly until all charges have been collected or have recombined.

B. Effect on an Inverter

Despite creating a transient current, laser illumination of a PN-junction may not be sufficient to alter the logic state

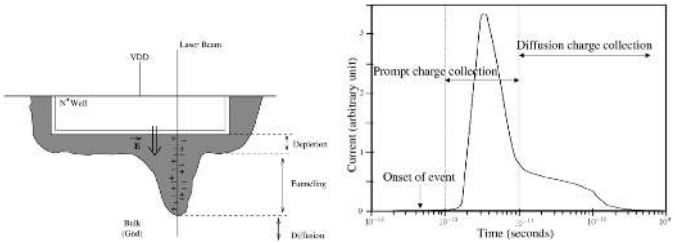


Fig. 1: Laser-induced photocurrent generation in PN-junctions [10] [15].

of a target. Using an inverter as an example, there are 4 PN-junctions with an electrical field capable of creating a transient current, both drains and sources of the two transistors.

In the case where the input state of the inverter is "0", the PMOS transistor is "ON" and the NMOS transistor is "OFF" resulting in a "1" logic state output (as depicted in the left part of figure 2). A laser pulse targeting the NMOS' drain will have an effect on the output of the inverter. In this situation, the transient current goes from the drain towards the substrate, discharging the load capacitance. As a result, the output state of the inverter temporarily changes to a low-level until the transient current ends. Then, the load capacitance is re-charged through the "ON" PMOS transistor and the output state of the inverter goes back to a high state. This transient output voltage can propagate itself further in the logic. It is called a Single Event Transient (SET) [15].

Targeting the inverter's other PN-junctions would not create any SET. Indeed, transient currents created in the PMOS' drain or source would create leakage paths towards the N-Well which is biased at Vdd and therefore would not discharge the load capacitance. Any transient current induced in the NMOS source would also have no effect since it is isolated from the output by the "OFF" NMOS.

A similar reasoning may be done in the case where the input is in a "1" state (right part of figure 2), only a transient current created in the "OFF" PMOS' drain would create a SET and alter the inverter's output. The laser-sensitive areas for each state of the inverter are highlighted in red in figure 2. They match the drain of the "OFF" transistor.

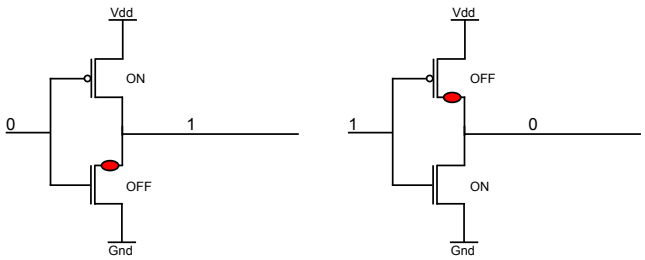


Fig. 2: Laser-sensitive areas (red) of an inverter depending on its state.

C. Effect on a SRAM Cell and Fault Model

The core part of a SRAM cell is made of two cross-coupled inverters (figure 3a). If a SET is induced in one of the two inverters (figure 3b), it propagates through the second one (figure 3c), driving the cell in its opposite steady state. When the transient current vanishes, since the cell is in a steady state it doesn't revert to its previous state and the stored value is altered (figure 3d). This phenomenon is called a Single Event Upset (SEU) [15].

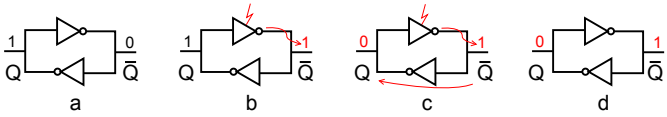


Fig. 3: Single Event Upset mechanism.

As a result of the inverter analysis, we can assume that for each state of a SRAM cell ("0" or "1") the drains of the OFF transistors of the two core inverters can produce an SEU when targeted. This means that a SRAM cell should have 4 SEU-sensitive areas linked to its inverters (there are also laser-sensitive areas linked to the access transistors). Figure 4 displays the laser-sensitive areas of the 5 transistors SRAM cell we used during our experiments. In this instance, we define a bit-set (resp. bit-reset) as the switching of the cell's output node (Data_out) from "0" to "1" (resp. from "1" to "0") as a result of a laser shot.

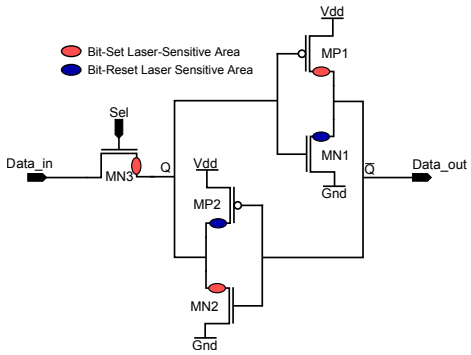


Fig. 4: Schematic of the 5T SRAM cell with its sensitive areas.

D. SRAM Cell Layout and Sensitive Areas

The cell, which measures 4 μm by 9 μm, is embedded in a 0.25 μm CMOS technology chip. The chip was specifically designed for laser testing, with as few metal layers as possible above the cell to allow front side laser fault injection (metal paths reflect laser light, hence shielding a device against laser exposure). Figure 5a shows the layout of the cell along with the positions of its different laser-sensitive areas. Consider the drain of transistor MP1 (upper left part of figure 5a). It is laser-sensitive only if the SRAM is in its "0" state: targeting it with a laser may induce a bit-set. In figure 5a, laser sensitive areas causing bit-sets are highlighted in red. Those corresponding to bit-resets are highlighted in blue. If the bit-set and bit-reset areas do not overlap (due to laser settings that limits its effect area) it should be impossible to inject bit-flip faults.

However, if the effect area of a laser shot is sufficiently large, the bit-set/reset areas may extend and overlap as exemplified in figure 5b. A laser beam targeted at an overlap area

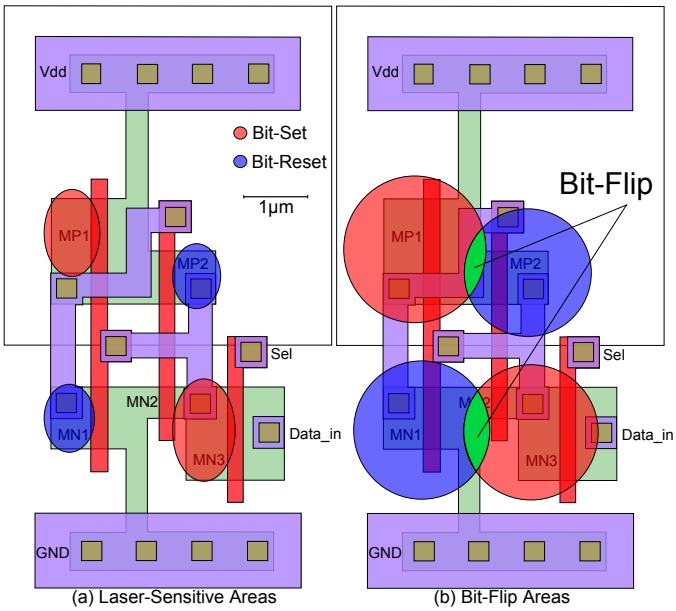


Fig. 5: 5T SRAM cell layout.

(a bit-flip area) may be able to induce a SEU regardless of the SRAM's state: this corresponds to the bit-flip fault model.

III. Previous Works for 50 ns Pulse Duration

During their experiments Roscian et al. [10] used a 1064 nm laser source, a 1 μm spot size, and a pulse duration of 50 ns. Their target was a 5 transistors SRAM cell designed in CMOS 0.25 μm technology (see figure 4).

The first point that came out from their experiments is that only three of the four expected sensitive areas created SEUs. The drain of MP2 did not react as expected: the sensitive area was masked. In [9] Sarafianos et al. made the hypothesis that this phenomenon was due to the comparatively small surface of the drain of MP2 compared to a counter-balancing effect of the photocurrent induced in the shared drain of transistors MN2 and MN3, MN3 is the access transistor of the SRAM (see figure 5a). Note that MP2's drain has a drain surface smaller than that of MN2/MN3 which makes this phenomenon happen (the photocurrent magnitude is proportional to the drain surface). Figure 6 from [10] reports the obtained laser-sensitivity map of the SRAM cell at 0.42 W laser power.

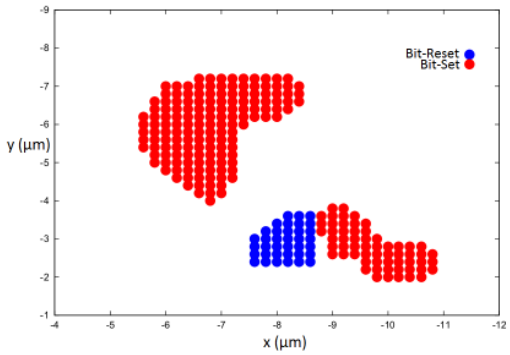


Fig. 6: 5T SRAM laser-sensitivity map for 50 ns pulses [10].

The second point in these results was that no bit-flip type faults were obtained. Contrary to their previous hypothesis, no laser position allowed to create both a bit-set and a bit-reset faults.

A. Simulation Results

Using the electrical model introduced by Sarafianos et al. in [9], [11], [12], they were able to validate their results on simulation basis: the obtained map of laser-sensitive areas is given in figure 7 for a laser pulse duration of 50 ns. This laser-sensitivity map matches the experimental results (see figure 6): no bit-flip faults were obtained (there is no overlap between bit-set and bit-reset areas, given in red and blue respectively), the fourth laser-sensitive area of transistor MP2 is also missing. The electrical models they built was tuned for laser pulses ranging from 50 ns to 20 μs. It allowed the authors of [9] and [10] to explain the counterbalancing effect that leads to the masking of the MP2 drain sensitive area and also to explain the infeasibility of bit-flip type faults.

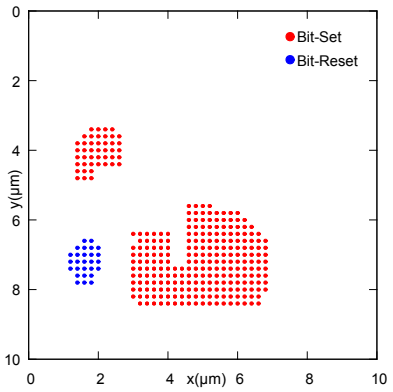


Fig. 7: Simulation-based laser-sensitive map of a 5T SRAM at 50 ns laser pulse duration.

B. Application to a Commercial Microcontroller

[10] reports similar experiments conducted on the RAM of a 0.35 μm CMOS technology commercial microcontroller using the same laser settings. The results are shown in figure 8 (the size of one SRAM cell is highlighted with a black square). Similarly, no bit-flip type faults were obtained and two sensitive areas per cell were missing.

Although they didn't have any knowledge of the RAM layout, this result is coherent with their previous hypothesis of a counterbalancing effect due to the access transistors. Standard SRAM cells used in microcontroller RAM usually have two access transistors, leading to a masking effect in one additional sensitive area (remember that the 5T SRAM has only one access transistor).

IV. Results for 30 ps Pulse Duration

A. Laser Test Bench

The laser source we used has the following characteristics: 1030 nm wavelength, a laser pulse duration of 30 ps and an energy ranging from 0 to 100 nJ. The optical path outputs a

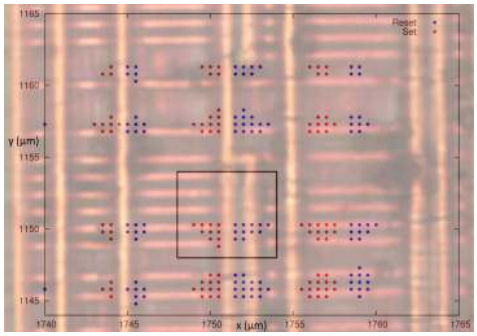


Fig. 8: Laser-sensitivity map of a portion of the memory of a microcontroller using 50 ns pulses [10].

spot of 1 μm, 5 μm or 20 μm depending on the chosen lens. An infra-red camera was used to adjust the focus of the spot.

Fault injection was performed through the front-side of the chip. The optical lens is attached to a motorized XYZ stage with a minimum step of 0.1 μm.

B. Laser-Sensitivity Map Drawing Process

Using a PC to automate the process, we moved the laser over the area of the cell by steps of 0.2 μm. For each position we shot the laser after writing the cell to 0, then shot again after writing it to 1 and read the stored value after each shot. This allowed us to draw a map of the results where for each X/Y position of the laser spot on the cell where a fault has been recorded, we draw a colored dot depending on the fault type (red for a bit-set and blue for a bit-reset). Lastly, if we can obtain a bit-set and a bit-reset on the same position it means that bit-flips are possible on this specific position.

Such laser-sensitivity maps were drawn at various laser energies.

C. Experimental Results

We carried out our laser-induced fault injection experiments on the 5T SRAM cell already described (see figure 4) using similar settings. However, we used a 30 ps laser pulse duration. Our intent was to test whether the bit-set/reset fault model and the absence of some laser-sensitive areas were still valid or not.

Figure 9 displays the laser-fault sensitivity map we obtained at 3.2 nJ laser energy (higher energies led to the destruction of the cell). Four laser-sensitive areas were obtained, which is consistent with the laser-sensitivity assumptions depicted in figure 5a. The previously hidden laser-sensitive area of transistor MP2 is no longer missing. Moreover, similarly with the results of Roscian et al., no bit-flip faults were induced.

We drew the assumption that the use of a 30 ps laser pulse reduces the effect area of a laser spot as compared with a nanosecond range laser pulse. As a result, a picosecond range laser shot may not permit the existence of the counterbalancing effect at the origin of the masking of laser-sensitive areas. We studied further this assumption on the basis of simulations and experiments as reported in the next subsections.

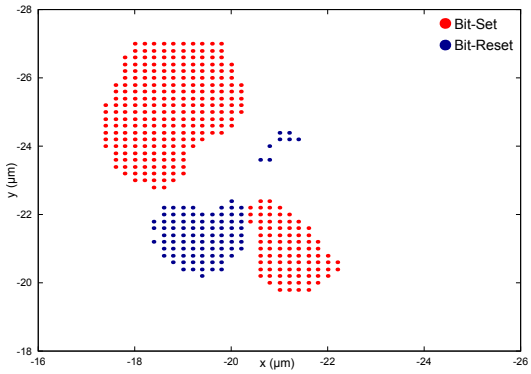


Fig. 9: Laser-fault sensitivity map of a 5T SRAM at 30 ps.

D. Adaptation of the Simulation Model to Picosecond Pulses

Douin et al. [16] reported the most complete research work in modeling at electrical level the effect of pulse duration on laser fault injection into a SRAM cell. They introduced two different electrical models: one for short laser pulses and the other for long laser pulses (the threshold between short and long pulses was around one nanosecond). We chose another approach: using the electrical model already introduced by Sarafianos et al. [9], [11], [12] for laser pulses in the nanosecond range. However, we changed several parameters of their model in order to take into account the laser pulse duration and our assumption of a reduced effect area for shorter laser pulses.

For the sake of brevity we refer the reader to the corresponding bibliography [9], [11], [12] for a complete description of this electrical model. It is mostly built to take into account the laser-induced photocurrents. To that end, PN-junction photocurrents are modeled with voltage controlled current sources, which are added to the electrical model of the target. The laser-induced photocurrent model they built is given in Eq. 1:

$$I_{ph}(t) = [a(E).V_r + b(E)].A.\alpha_{topology}.\Omega_{shape}(t) \quad (1)$$

The laser-induced current pulse is shaped in the time domain thanks to the term $\Omega_{shape}(t)$ in Eq. 1 which takes into account the laser shot duration. At 30 ps laser pulse duration, $\Omega_{shape}(t)$ has the shape of a double exponent lasting 100 ps. The other three multiplicative terms model the photocurrent pulse magnitude according to the other parameters of interest:

- $a(E).V_r + b(E)$: where V_r is the junction's reverse voltage, and $a(E)$, $b(E)$ are coefficients depending on the laser energy E. This term models the impact of both the laser energy and the reverse bias voltage of the PN-junction,
- A: the junction's area,
- $\alpha_{topology}$: this coefficient models the influence of the topology, i.e. the fact that the photocurrent magnitude decreases as the laser spot distance from the PN-junction increases.

As mentioned, the term $\alpha_{topology}$ is used to model the effect area of a laser shot, i.e. the effect of the distance between the laser spot and a given PN-junction on the magnitude of

the corresponding laser-induced photocurrent. Sarafianos et al. obtained its value experimentally for laser pulse durations in the nanosecond range. It is depicted in deep blue in figure 10 for a 50 ns laser pulse duration: the effect of the laser extents over several micrometers.

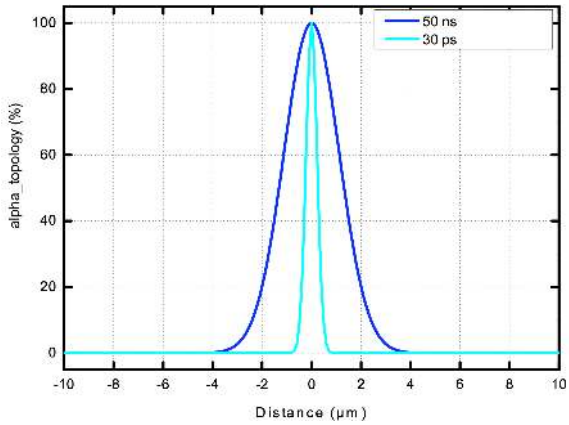


Fig. 10: $\alpha_{topology}$ curves for 50 ns (deep blue) and 30 ps (light blue) laser pulses.

Following our assumption of a reduced effect area at 30 ps laser pulse duration, we adjusted $\alpha_{topology}$ to a narrower shape as depicted in light blue in figure 10 (the photocurrent magnitude is halved as the laser spot is moved of a distance of 0.5μm away from the PN-junction of interest). The resulting laser-sensitivity map is given in figure 11: it has four distinct laser-sensitive areas (similarly to the experimental map displayed in figure 9). The laser-sensitive area corresponding to the drain of transistor MP2 is no longer missing. In addition, because bit-set and bit-reset areas do not overlap in figure 11, it is a further validation that the bit-set/reset fault model is valid for picosecond range laser pulse duration.

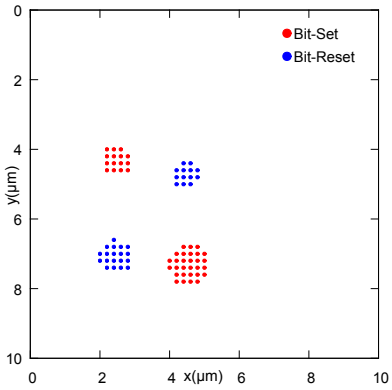
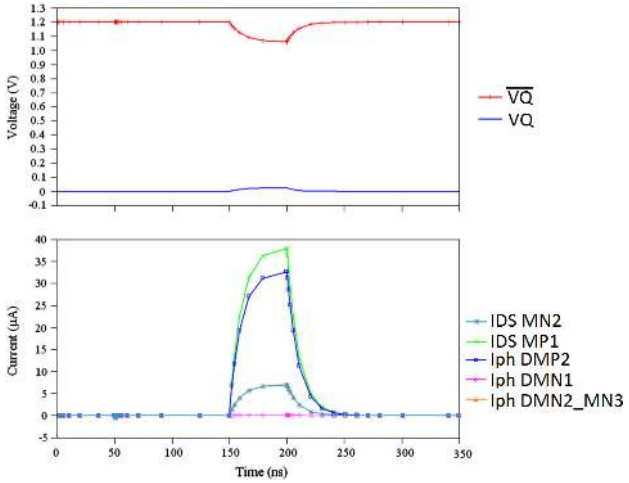


Fig. 11: Simulation-based SRAM cell laser-sensitivity map for 30 ps laser pulse duration.

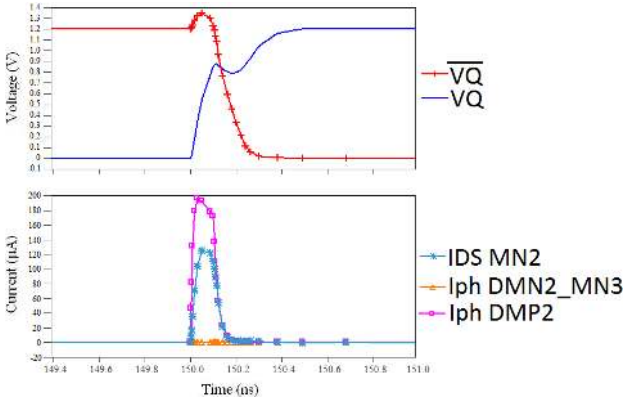
Note that the experimental sensitivity maps were drawn from frontside laser injection, as a result the shielding effect of the SRAM's metal interconnections is discernable in the shape of the sensitive areas. This phenomenon is not taken into account at simulation level, this partly explains the discrepancies between experimental and simulation-based sensitivity maps.

E. Analysis at Electrical Level

Figure 12a from [9] displays the internal nodes voltages and currents of the SRAM cell in state "1" for a 50 ns laser pulse targeting the drain of MP2. The photocurrent induced in the drain of MP2 (Iph DMP2) that should be the root cause of a SEU is too weak to lead to a flip of the SRAM cell: the photocurrent simultaneously induced in the common drain of transistors MN2 and MN3 (Iph DMN2_MN3) has a decisive counterbalancing effect. For a 30 ps laser pulse the counterbalancing photocurrent (Iph DMN2_MN3 in figure 12b) is almost equal to zero because the effect area of the laser spot targeting MP2 is reduced. The photocurrent induced in the drain of MP2 (Iph DMP2) goes rapidly above the current flowing through transistor MN2 (IDS MN2): a SEU is induced.



(a)



(b)

Fig. 12: Extracted waveforms from the electrical simulator at the drain of MP2 for (a) 50 ns [9] and (b) 30 ps pulse duration.

F. Application to a Commercial Microcontroller

We also performed laser fault injection in the RAM memory of the same microcontroller used by Roscian et al. [10]. We used the laser bench previously described, but contrary to the test performed on a single cell, the injection was performed through the backside of the chip. We drew a 40 μm by 40 μm laser-sensitivity map of a part of its memory plane.

Figure 13 displays the obtained laser-sensitivity map (a black rectangle delimits the surface of a single cell). 4 laser-sensitive areas per cell are clearly observable, which is coherent with our previous results. This map also seems to confirm the hypothesis of Roscian et al. that the two access transistors of 6T SRAM cells were masking two sensitive areas per cell when using a 50 ns pulse duration.

Moreover, no occurrence of any bit-flip type fault was observed. While some bit-set and bit-reset areas on the map appeared to overlap, these cases are actually a bit-set occurring on one cell and a bit-reset occurring on an adjacent cell for the same laser spot position.

Note that a recent work from Courbon et al. [17] conducted on a CMOS 90 nm D flip-flop also confirms the relevance of the bit-set/reset fault model over the bit-flip fault model.

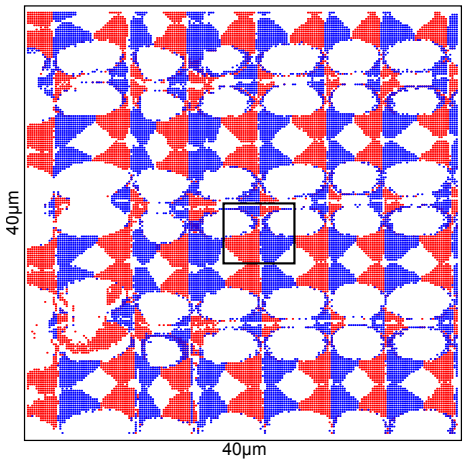


Fig. 13: Cartography of a portion of the memory of a microcontroller using 30 ps and 3.2nJ pulses.

V. Conclusion

In this paper, we showed that pulse duration has to be carefully considered when performing laser fault injection tests on SRAM cells. Be it during simulations at design time, or post-production during tests on actual chips, limiting the study to nanosecond range pulse durations may hide vulnerabilities.

The experimental results showed that the masking effect which was leading to the disappearance of a sensitive area in [10] does not occur with shorter pulses. This has for notable consequence that the robustness improvement relying on this masking effect presented in [18] may not be valid for picosecond range pulses.

Our results are consistent with those of [10]: the bit-set/reset fault model is relevant to describe laser-fault injection in SRAMs.

We then improved the simulation model presented in [9], [11], [12] by adapting it to picosecond range pulse durations. The new model fits correctly with our experimental results. Such a picosecond range model has also the interest to be usable to emulate the effect of ionizing particles on ICs. This extends the scope of this work.

Finally, these results were confirmed by running laser-fault injection campaigns on the RAM memory of a commercial microcontroller.

In future works we will aim to apply and extend these works to more complex structures such as full standard cells with the end goal of integrating the simulation process in the standard design workflow.

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