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LATCH-UP CONTROL IN CMOS INTEGRATED CIRCUITS

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ABSTRACT

The potential for latch-up, a pnpn self-sustaining low impedance state, is inherent in standard bulk CMOS-integrated circuit structures. Under normal bias, the parasitic SCR is in its blocking state but, if subjected to a large voltage spike or if exposed to an ionizing environment, triggering may occur. This may result in device burn-out or loss of state. The problem has been extensively studied for space and weapons applications. Prevention of latch-up has been achieved in conservative design (~9 μm p-well depths) by the use of minority lifetime control methods such as gold doping and neutron irradiation and by modifying the base transport factor with buried layers. The push toward VLSI densities will enhance parasitic action sufficiently so that the problem will become of more universal concern. This paper will survey latch-up control methods presently employed for weapons and

space applications on present (~9 μm p-well) CMOS and will indicate the extent of their applicability to VLSI designs.

INTRODUCTION

Latch-up in bulk, CMOS-integrated circuits occurs due to parasitic four layer pnpn paths. The transistors involved in such a path are identified in Figure 1. Under normal operation, the emitter-base junctions of both transistors conduct only leakage current and the structure is in its blocking state. If enough lateral current can be made to flow, the transistors become forward-biased and regeneration can be initiated. Once attained, functionality is lost and device destruction may follow--metallization or junction failure. The smaller structures required for higher packing densities will enhance the problem. Bulk CMOS having an ~9 micron p-well depth (hereinafter referred to as standard CMOS) has been made free of the latch-up problem by the generic solution of reduction of minority lifetime. The same techniques, however, will not by themselves be sufficient to guarantee workable, latch-up free CMOS circuits in reduced design rule structures. This paper will review latch-up prevention in present standard CMOS, in particular, discuss a CMOS process on an epitaxial substrate that made a test device free of latch-up. A simple

analysis is presented to explain the obtained protection. With the prevention methods in mind, we then present a process outline that should be latch-up free for the smaller structures.

LATCH-UP CONTROL IN STANDARD CMOS

In Figure 1 we show a cross-section of the standard bulk CMOS structure with the parasitic bipolar devices involved in the latch-up process identified. Also shown is a lumped, first-order equivalent model. Latch-up is possible only if (1) the transistors become biased into the forward active mode, (2) the transistor current gain product ($\beta_{npn} \cdot \beta_{pnp}$) exceeds a required minimum for regeneration to occur, and (3) the bias supply is capable of sourcing a current greater than the holding current. Prevention of any of these requirements will prevent latch-up.

At present, the principal methods used concern requirement two above. Since the current gains of the standard CMOS structure are usually base transport limited, minority lifetime control proved to be a useful parameter to focus upon. Diffusing gold at temperatures greater than 800°C to obtain concentrations of 10^{15}/cc of gold was found to produce the desired results (1)--minority lifetimes less than 100 nS and $\beta_{npn} \geq 1$. Fast neutron irradiation to a level of 10^{14} N/cm^2

of energies greater than .1Mev (2,3) produced similar results. These methods were attractive because little process modification was required and few undesirable additional effects were introduced.

Current gain is also reduced by appropriate base concentration profiling. A buried layer morphology has been shown to reduce the base transport by use of an increased base Gummel number and a retarding electric field (4). Except for the extra processing required for the buried layer itself, again the standard CMOS process was unaltered. A buried layer of 30 $\Omega/\square$ and $\approx$13 μm deep prior to the epitaxial layer deposition was used. The structure, shown in Figure 2, was immune to latch-up, a β_{npn} of approximately 1 was obtained. R_s and R_w in Figure 1 were substantially reduced by this process. The effect of these shunt resistors is itself a potential control of latch-up as will now be discussed.

If the available power supply current is below the holding current of the pnpn path, even if latch-up is initiated, it cannot be sustained. Processing standard CMOS on Epi-wafers (n on n^+) will reduce R_s and raise the holding current as described in Eq. 1.

$$I_H = \frac{I_{Rs}\ \beta_p\ (\beta_n + 1) + I_{Rw}\ \beta_n (\beta_p + 1)}{\beta_n\ \beta_p - 1} \qquad (1)$$

I_{Rs} = Current flowing through R_s

I_{Rw} = Current flowing through R_w

I_H = Holding current

Since I_{Rs} increases substantially for an Epi structure, the holding current becomes quite large. For CMOS 4007 devices fabricated on Epi wafers, the holding current was made to exceed the level at which device destruction was obtained (junction failure). Caution is warranted here, however, as the structure is not immune to latch-up except under normal bias. If inputs are raised above V_{DD}, the conditions leading to Eq. 1 are not met, thus nullifying the results. Latch-up can occur, but the device was found to exit from latch upon returning to normal bias conditions, $V_{SS} \leq V_i \leq V_{DD}$. A CMOS 4007 circuit processed upon an epitaxial substrate will latch-up if V_{DD} is left floating and an input is held positive with respect to V_{SS}. Making V_{DD} equal to the most positive potential applied to the circuit keeps the device out of latch-up as shown in Figure 3b. In figure 3a a standard device is shown. Note that tying V_{DD} to the most positive potential here raises the holding current but latch-up is still observed. The functional relationship expressed in Eq. 1 is shown in Figure 4.

Addition of a parasitic emitter resistor indicates an additional favorable effect. The holding current now becomes

$$I_H = \frac{(V_{\beta E})_{pnp} + r_{ep} I_{DD}\ \beta p(\beta n+1) + \dfrac{(V_{\beta E})_{npn} + r_{en} I_{DD}\ \beta_n(\beta_p+1)}{R_w + r_{en}}}{R_s + r_{ep}} \qquad (2)$$
$$\beta n \beta p - 1$$

with r_{ep} = emitter series resistance of the pnp

r_{en} = emitter series resistance of the npn.

This effect is shown graphically in Figure 5.

Another useful effect of the epitaxial process concerns the current gain product requirement for latch-up. This is generally expressed as $\beta_{npn}\ \beta_{pnp} \geq 1$ (6). If the supply current is limited, this requirement is too restrictive and should be replaced by

$$\beta_n\ \beta_n \geq \frac{I_{Dmax} + I_{Rw}\ \beta_n}{I_{Dmax} - I_{Rw} - I_{Rs}\ \dfrac{\beta_n + 1}{\beta_n}} \qquad (3)$$

where I_{Dmax} is the maximum available supply current.

Gain products greater than one can be tolerated. The Fpi CMOS structure, for example, $\beta_{npn} \doteq 140$, and $\beta_{pnp} \doteq .25$, a gain product of 35, did not latch. Note that an infinite available

source current will result in a β product of 1. Again, the emitter resistance will change Eq. 3 considerably for large values.

A particular latch-up path that is easily eliminated concerns the input protection circuitry. A p diffused region is generally used for series impedance and shunt diode clamping. Surrounding this region with a grounded p ring as shown in Figure 6 forms a pseudo collector that alters the path drastically. The β_{pnp} reductions by factors of 140 have been obtained (7). Since these lateral devices normally exhibit gains of .25 or less, the vertical npn must now have a gain in excess of 500 for the input circuitry to participate in latch-up.

REDUCED DESIGN RULE CMOS

To obtain increased packing densities, shallower p-wells and smaller surface separations must be used. Following general MOS scaling rules (8), a 2 micron gate scaled transistor with a 40 nM gate oxide will have a density of 40,000 gates/cm^2. For such circuits, both parasitic transistors will have increased current gains and latch-up susceptability will increase. A test circuit with 4 μm channel length and a 3.0 micron, 3500 $\Omega/\square$ p-well was found to

latch after 2 x 10^{14} N/cm^2. Extrapolation of the gain fall-off with neutron irradiation, assuming a base transport dominated model indicates that a dose of 3-5 x 10^{15} N/cm^2 will be required for unity gain to be obtained in the vertical npn transistor. Such a fluence level is unacceptable as it would require long exposures (approximately 16 hours at Sandia's Pulse Reactor) and be accompanied by total gamma dose in excess of 10^5 Rads(Si). Gold densities of 10^{16}/cm^2 would be needed--enough to cause compensation problems.

A structure that will render shallow p-well CMOS free from latch-up has evolved from these considerations. The p-well, 1.5-3 microns deep, will have a reduced surface concentration produced by use of a counter doped shallow As implant. A larger Gummel number is thus obtained while maintaining a low 10^{16}/cm^2 surface concentration. The substrate will be n on n^+ Epi to reduce R_S (increase I_H). To further reduce the current gain of the vertical npn, an arsenic implant will be used followed by processing of less than 900°C. This will result in a shallow poor emitter (9). Pseudo collectors about the input protection circuit could be included.

SUMMARY

Latch-up in standard CMOS designs is controllable by use of minority lifetime reduction, gold diffusion or neutron irradiation. Other techniques that have shown control are epitaxial substrates, buried layer structures, and layout changes. The effects of smaller dimensions required for increased density will be controllable only by combinations of these and, possibly, the addition of emitter efficiency reduction afforded by the use of incomplete annealed arsenic n-channel source/drains.

Figures

1a. Cross-section of a standard CMOS section showing a four layer path and the parasitic transistors.

1b. Lumped equivalent model of pnpn parasitic.

2. Cross-section of the buried layer CMOS.

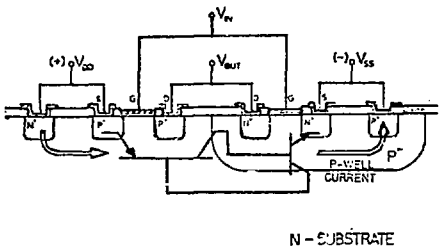
3a. Latch in standard CMOS. Lower holding current is for latch between an input and V_{SS}, the higher holding current is for V_{in}, parallel with V_{DD} to V_{SS}.

3b. Latch in Epi-CMOS device. Latch-up occurs only if V_{DD} is open. Putting V_{DD} to the most positive potential prevents SCR action.

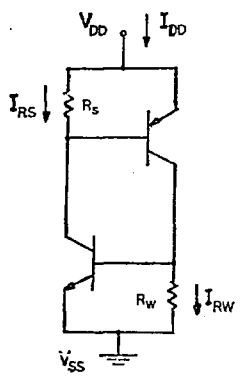
4. Holding current as a function of Substrate Resistance, R_s.

5. Holding current as a function of Emitter Series Resistance, r_e.

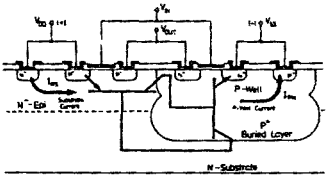
6. Example of layout prevention of latch-up. The psuedo collector shunts any emitted current to ground preventing participation in latch-up.

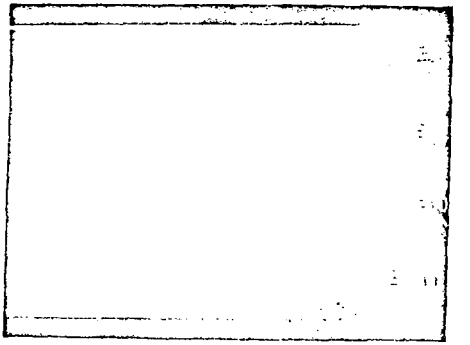


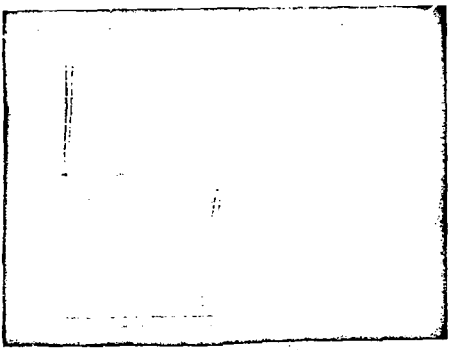
Standard bulk CMOS cross-section showing parasitic bipolar devices involved in SCR action.

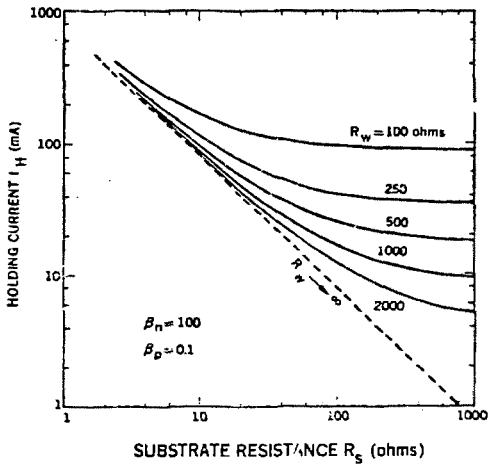


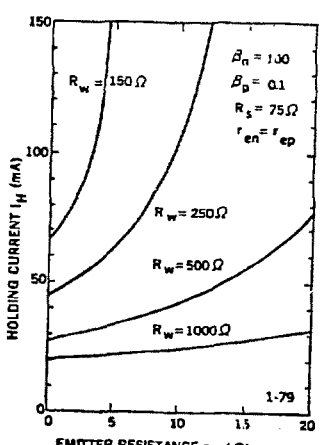
First-order equivalent circuit of the pnpn latch-up path in a bulk CMOS structure.

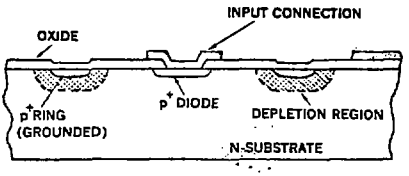

N - Epi
P-Well
Buried Layer
N - Substrate






1000
100
10
1
HOLDING CURRENT I_H (mA)
R_w = 100 ohms
250
500
1000
2000
β_n
β_p
β_n = 100
β_p = 0.1
1
10
100
1000
SUBSTRATE RESISTANCE R_S (ohms)


150
100
50
0
HOLDING CURRENT I_H (mA)
R_w = 150Ω
β_n = 100
β_p = 0.1
R_s = 75Ω
$r_{en} = r_{ep}$
R_w = 250Ω
R_w = 500Ω
R_w = 1000Ω
1-79
0
5
10
15
20
EMITTER RESISTANCE r_e (Ω)



PSUEDO COLLECTOR STRUCTURE

References

1. W. R. Dawes and G. F. Derbenwick, "Prevention of CMOS Latch-Up by Gold Doping," IEEE Trans. on Nuclear Science, Vol. NS-23, No. 6, pp. 2027-2030, December 1976.

2. J. R. Adams and R. J. Sokel, "Neutron Irradiation for Prevention of Latch-Up in MOS Integrated Circuits," IEEE Annual Conf. on Nuclear and Space Rad Effects, 1979.

3. C. E. Barnes, et al, Latch-Up Prevention in CMOS, Sandia Report SAND 76-0048, March 1976.

4. D. B. Estreich and A. Ochoa, Jr., "An Analysis of Latch-Up Prevention in CMOS ICs Using an Epitaxial-Buried Layer Process," International Electron Device Meeting, Washington, D.C., 1978.

5. S. M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, 1969.

6. D. B. Estreich, Ph.D., Dissertation, Department of Electrical Engineering, Stanford University, in progress.

7. R. H. Dennard, et al, "Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions," IEEE J. of Solid State Circuits, Vol. SC-9 No. 5, October 1974, pp. 256-260.

8. D. B. Estreich, Ph.D., Dissertation, in progress.

9. W. R. Dawes, private communication.

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