Latchup-Free ESD Protection Design With Complementary Substrate-Triggered SCR Devices

Ming-Dou Ker, *Senior Member, IEEE,* and Kuo-Chun Hsu, *Student Member, IEEE*

***Abstract*—The turn-on mechanism of silicon-controlled rectifier (SCR) devices is essentially a current triggering event. While a current is applied to the base or substrate of an SCR device, it can be quickly triggered on into its latching state. In this paper, latchup-free electrostatic discharge (ESD) protection circuits, which are combined with the substrate-triggered technique and an SCR device, are proposed. A complementary circuit style with the substrate-triggered SCR device is designed to discharge both the pad-to-V_{SS} and pad-to-V_{DD} ESD stresses. The novel complementary substrate-triggered SCR devices have the advantages of controllable switching voltage, adjustable holding voltage, faster turn-on speed, and compatible to general CMOS process without extra process modification such as the silicide-blocking mask and ESD implantation. The total holding voltage of the substrate-triggered SCR device can be linearly increased by adding the stacked diode string to avoid the transient-induced latchup issue in the ESD protection circuits. The on-chip ESD protection circuits designed with the proposed complementary substrate-triggered SCR devices and stacked diode string for the input/output pad and power pad have been successfully verified in a 0.25-μm salicided CMOS process with the human body model (machine model) ESD level of $\sim$7.25 kV (500 V) in a small layout area.**

***Index Terms*—Complementary, electrostatic discharge (ESD), ESD protection circuit, silicon-controlled rectifier (SCR), substrate-triggered technique.**

I. Introduction

ON-CHIP ESD protection circuits have to be added between the input/output (I/O) pads and V_{DD}/V_{SS} to provide the desired electrostatic discharge (ESD) robustness in CMOS integrated circuits (ICs) [1]. The ESD specifications of commercial IC products are generally required to be higher than 2 kV in human body model (HBM) [2] ESD stress and 200 V in machine model (MM) [3] ESD stress. The typical design of on-chip ESD protection circuits in CMOS ICs used to sustain the required ESD level is illustrated in Fig. 1. To avoid unexpected ESD damage in the internal circuits of CMOS ICs [4]–[9], the power-rail ESD clamp circuit must be placed between the V_{DD} and V_{SS} power lines [10]. With the highest ESD robustness in the smallest layout area, as compared with other ESD protection devices [such as the diode, MOS, bipolar junction transistor (BJT), or field oxide device] in CMOS technology, the silicon-controlled rectifier (SCR) device has been used in on-chip ESD protection circuits for a long time [11], [12]. But the SCR device often has a higher switching voltage ($\sim$20 V) in the sub-quarter-micrometer CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stages. To provide more effective on-chip ESD protection, the low-voltage-trigger SCR (LVTSCR) [13] and the complementary-LVTSCR [14] were been invented to reduce the switching voltage of the SCR devices. Moreover, some advanced circuit techniques have been also applied to enhance the turn-on efficiency of ESD protection circuits with SCR devices, such as the gate-coupled technique [15] and the GGNMOS-triggered SCR [16]. However, another issue limiting the use of SCR devices is the latchup concern [17]–[19]. Because of the low holding voltage, such SCR devices could be accidentally triggered on by noise pulses [20], when ICs are in normal circuit operating conditions.

In this paper, in combination with the substrate-triggered technique, the novel p-type substrate-triggered SCR (P_STSCR) and n-type substrate-triggered SCR (N_STSCR) devices for ESD protection are proposed. The novel complementary-STSCR devices are process compatible to general fully silicided CMOS technologies without extra process modification for ESD protection. The latchup issue among the complementary-STSCR devices can be successfully solved by increasing the total holding voltage with the stacked diode string. Such novel substrate-triggered SCR devices with stacked diode strings are designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on by the substrate-triggered technique during the ESD-zapping conditions. The on-chip ESD protection circuits designed with such complementary-STSCR devices and stacked diode strings for input pad, output pad, and power rails have been successfully verified in a 0.25-μm salicided CMOS process [21], [22].

II. Complementary Substrate-Triggered SCR Devices

A. Device Structure

The proposed device structures of P_STSCR and N_STSCR devices with stacked diode strings are shown in Fig. 2(a) and (b), respectively. As compared with the traditional lateral SCR device structure [11], an extra p^+ diffusion is inserted into the substrate of the P_STSCR device structure and connected out as the p-trigger node of the P_STSCR device. When a trigger current is applied into this trigger node, the n-p-n bipolar transistor in the SCR structure is active, and the collector current of the n-p-n is generated to bias the p-n-p bipolar transistor. When p-n-p transistor is turned on, the collector current of the p-n-p is also generated to further bias the n-p-n transistor. The positive

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The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

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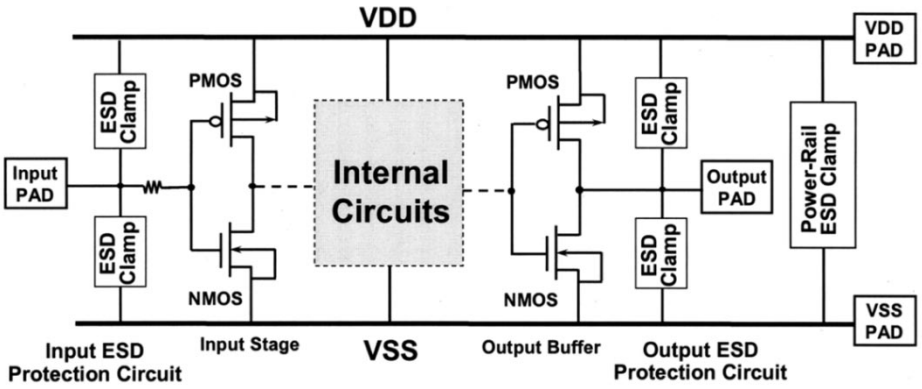


Fig. 1. Typical design of on-chip ESD protection circuits in CMOS ICs.

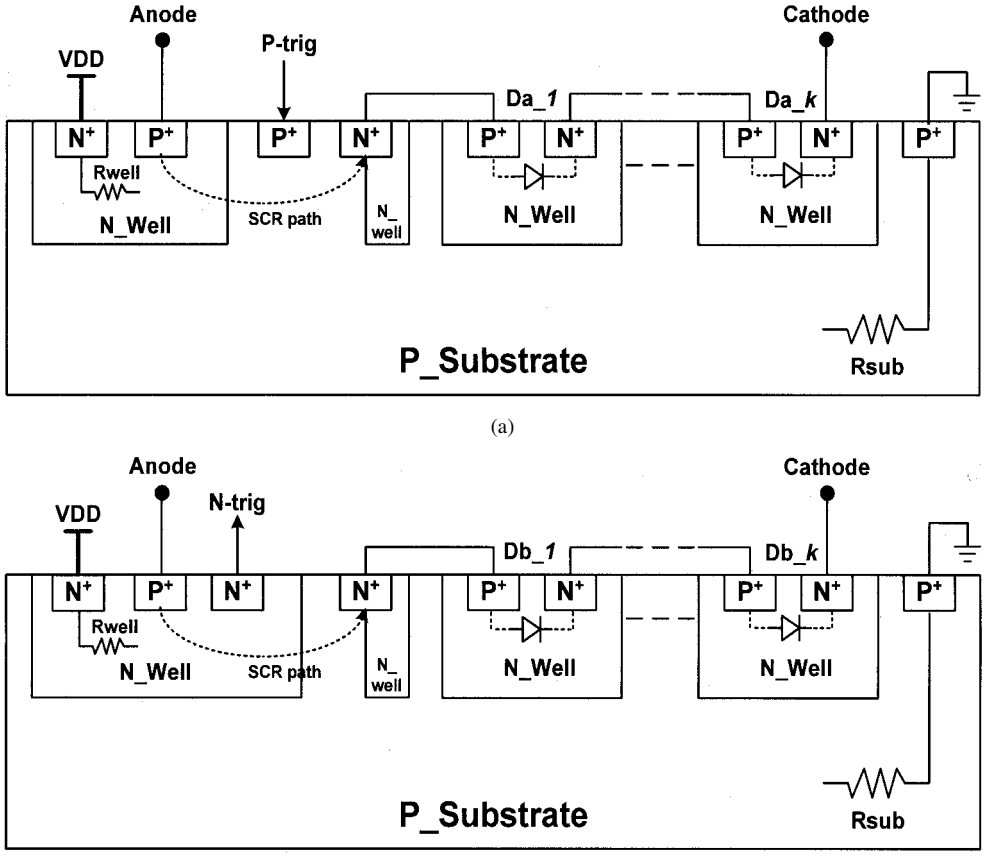


Fig. 2. Device structures of (a) the p-type substrate-triggered SCR device (P_STSCR) and (b) the n-type substrate-triggered SCR device (N_STSCR), with stacked diode string.

feedback regeneration mechanism of latchup is initiated by the substrate-triggered current in SCR structure, so the P_STSCR will be triggered into its latching state [23]. For the N_STSCR, an extra n^+ diffusion is inserted into the n-well of the N_STSCR device structure and connected out as the n-trigger node of the N_STSCR device. When a trigger current is drawn out from this trigger node, the N_STSCR will be triggered into its latching state through the positive feedback regeneration mechanism. The SCR paths in the P_STSCR and N_STSCR devices are indicated by the dashed lines shown in Fig. 2(a) and (b), respectively. The purpose of the additional n-well region under the n^+ diffusion at the end of the SCR path is used to further enhance the turn-on speed of the complementary-STSCR devices for more effective ESD protection with the substrate-triggered technique, because they increase the equivalent substrate resistance ($R_{\rm sub}$) in these device structures.

The required number of diodes in the stacked diode string is dependent on the power supply voltage level of CMOS ICs in applications. To avoid the latchup issue, the total holding voltage must be designed to be greater than the power supply voltage. The total holding voltage $V_{\rm H}$ of the P_STSCR or N_STSCR device with k stacked diodes can be written as

$$V_{\rm H} = V_{\rm H\_SCR} + (k \times V_D) \tag{1}$$

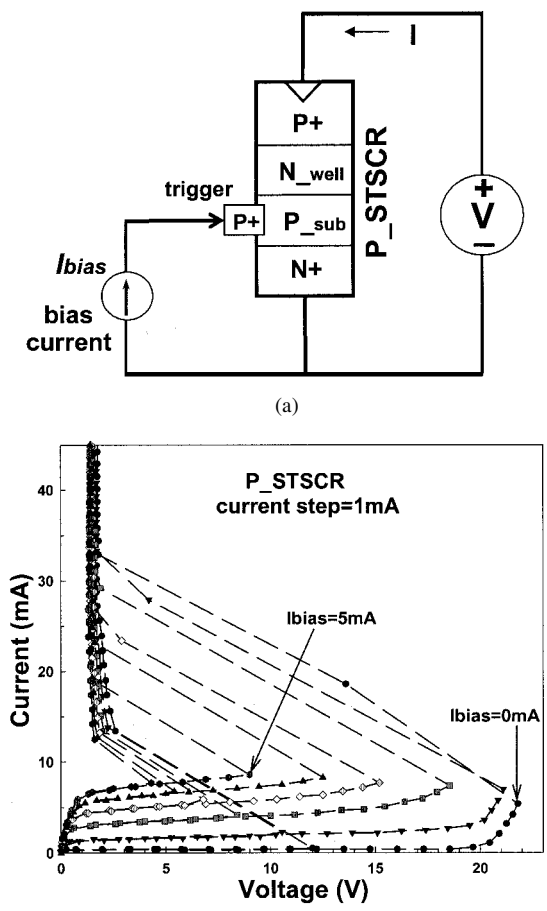


Fig. 3. (a) Experimental measurement setup to measure the I–V curves of the P_STSCR device. (b) Measured I–V curves of the P_STSCR device under different substrate-triggered currents.

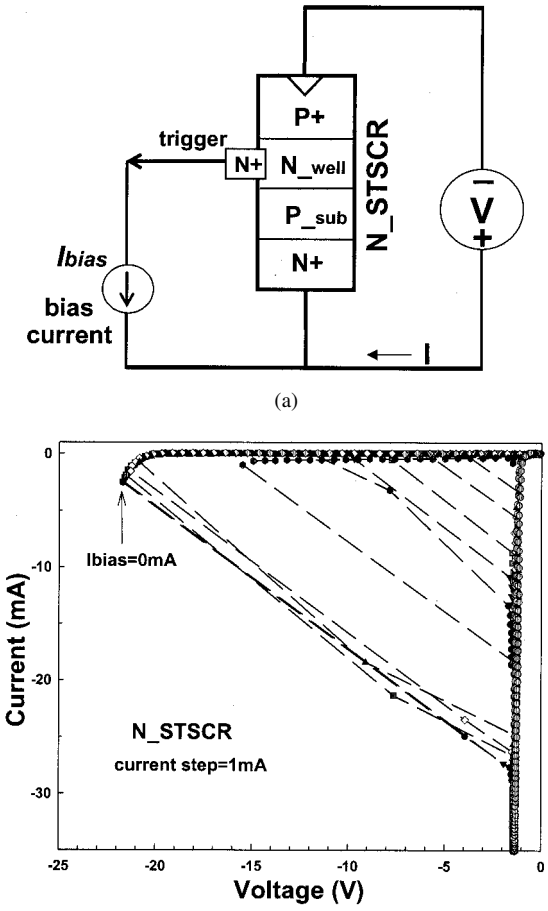


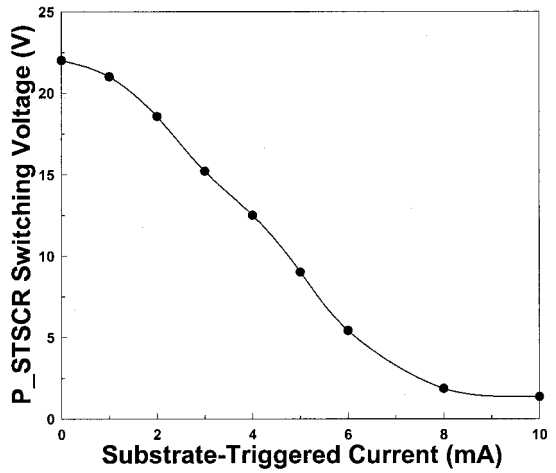
Fig. 4. (a) Experimental measurement setup to measure the I–V curves of the N_STSCR device. (b) Measured I–V curves of the N_STSCR device under different well-triggered currents.

where $V_{\mathrm{H\_SCR}}$ is the holding voltage ($\sim$1.5 V) of single P_STSCR (or N_STSCR) device and V_D is the cut-in voltage ($\sim$0.6 V) of a diode in the forward-biased condition.

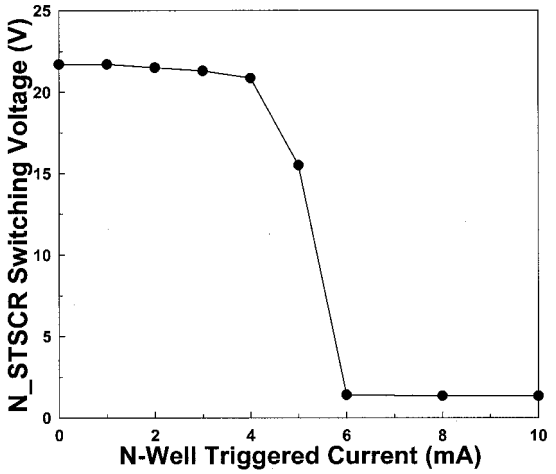
B. I–V Characteristics of the STSCR Devices

The P_STSCR and N_STSCR devices with different numbers of stacked diodes have been drawn in layout and fabricated in a 0.25-μm salicided CMOS process. The experimental setups to measure the dc I–V characteristics of the P_STSCR and N_STSCR devices are illustrated in Figs. 3(a) and 4(a), respectively. The measured dc I–V characteristics of stand-alone P_STSCR and N_STSCR devices are shown in Figs. 3(b) and 4(b), respectively. When the P_STSCR device has no substrate-triggered current ($I_{\mathrm{bias}} = 0$), the P_STSCR is turned on by its original n-well/p-substrate junction avalanche breakdown. In Fig. 3(b), the original switching voltage of the P_STSCR device is as high as 22 V when the substrate-triggered current is zero. But the switching voltage of the P_STSCR device is reduced to 9 V when the substrate-triggered current is 5 mA. Furthermore, the switching voltage of the P_STSCR device can be reduced to only 1.85 V when the substrate-triggered current is increased up to 8 mA. The characteristics of the N_STSCR device, as shown in Fig. 4(b), are similar to those of the P_STSCR device. The dependences of the switching voltage of the P_STSCR and N_STSCR devices on the substrate-triggered/well-triggered current are shown in Fig. 5(a) and (b), respectively. The higher trigger current leads to a much lower switching voltage in the complementary-STSCR devices. Without involving the avalanche breakdown mechanism, the P_STSCR and N_STSCR devices can be effectively triggered on by applying the substrate-triggered technique. With a much lower switching voltage, the turn-on speed of the P_STSCR/N_STSCR device can be further improved to quickly discharge ESD current. This is an excellent feature for the proposed complementary-STSCR devices used to protect the thinner gate oxide of input circuits in sub-quarter-micrometer CMOS processes.

Due to the parasitic SCR path, the transient-induced latchup phenomenon has been an inherent concern for bulk CMOS ICs when the IC is operating under normal circuit conditions. To avoid the latchup issue, the total holding voltage of the ESD protection device must be designed to be greater than the maximum voltage level of V_{DD} during the normal circuit operating conditions. This can be achieved by the complementary-STSCR devices with stacked diode strings in the ESD protection circuits. The dc I–V curves of the P_STSCR and N_STSCR devices with different numbers of stacked diodes are shown in Fig. 6(a) and (b), respectively. The corresponding

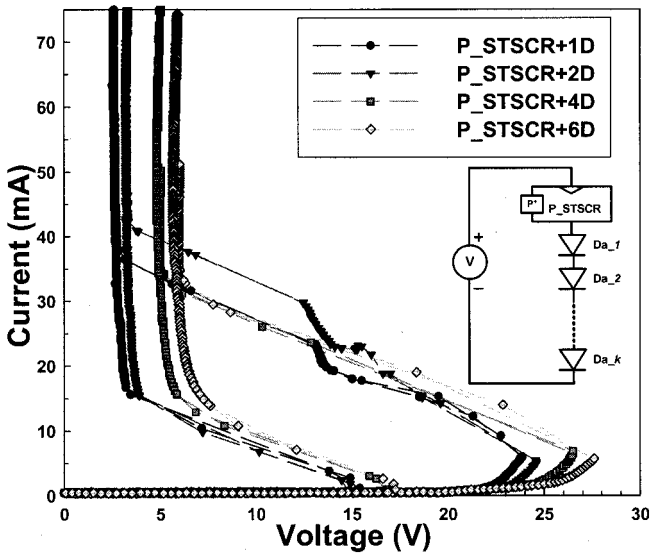


(a)

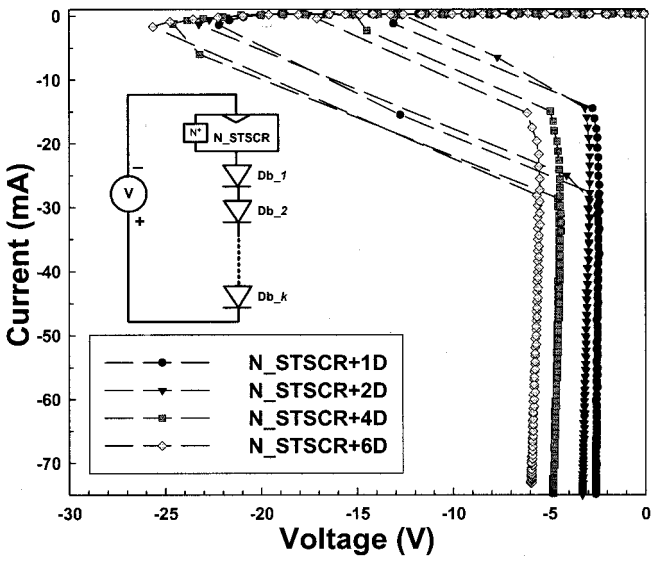


(b)

Fig. 5. Dependence of the switching voltage of (a) the P_STSCR and (b) the N_STSCR on the triggered current in p-substrate or in n-well.



(a)



(b)

Fig. 6. Measured I–V curves of (a) the P_STSCR and (b) the N_STSCR with different numbers of stacked diodes under 25 °C temperature.

measurement setups are inset into Fig. 6(a) and (b), respectively. The total holding voltages of the complementary-STSCR devices with stacked diode strings can be raised by increasing the number of stacked diodes. The holding voltages of the complementary-STSCR devices with one, two, four, and six diodes at the temperature of 25 °C are 2.6, 3.2, 4.6, and 5.8 V, respectively. The switching voltages of complementary-STSCR devices with stacked diode strings shown in Fig. 6 have a little increase when increasing the number of stacked diodes, but they can be reduced by the substrate-triggered technique to provide effective ESD protection. Fig. 7(a) and (b) shows the I–V curves of the P_STSCR and N_STSCR with six diodes under different substrate- or well-triggered currents, respectively. With the substrate-triggered technique, the switching voltages of the P_STSCR and N_STSCR with six diodes can be significantly reduced. Thus, the proposed P_STSCR/N_STSCR with stacked diode strings have the adjustable holding voltage and controllable switching voltage, so they can provide effective ESD protection for internal circuits as well as avoid the transient-induced latchup issue.

For precise design of the ESD protection circuits, the device characteristics of complementary-STSCR devices must be calibrated under different temperatures. The dc I–V curves of a P_STSCR with four diodes and an N_STSCR with six diodes under different temperatures are measured in Fig. 8(a) and (b), respectively. The insets in Fig. 8(a) and (b) are the enlarged views around the holding point for clear observation. The holding voltages of the P_STSCR with four diodes at the temperatures of 25 °C, 75 °C, and 125 °C are 4.6, 4.1, and 3.85 V, respectively. The dependences of the total holding voltage of the P_STSCR and N_STSCR with stacked diode strings on the number of stacked diodes under different temperatures are shown in Fig. 9(a) and (b), respectively. With increase of the number of stacked diodes, the holding voltages of such ESD protection devices are increased. The total holding voltages slightly reduce when the temperature is increased, because the current gain β of the parasitic bipolar transistor in the SCR device is enhanced with the increase of temperature. For safe applications in 2.5-V CMOS ICs, two diodes are suggested to

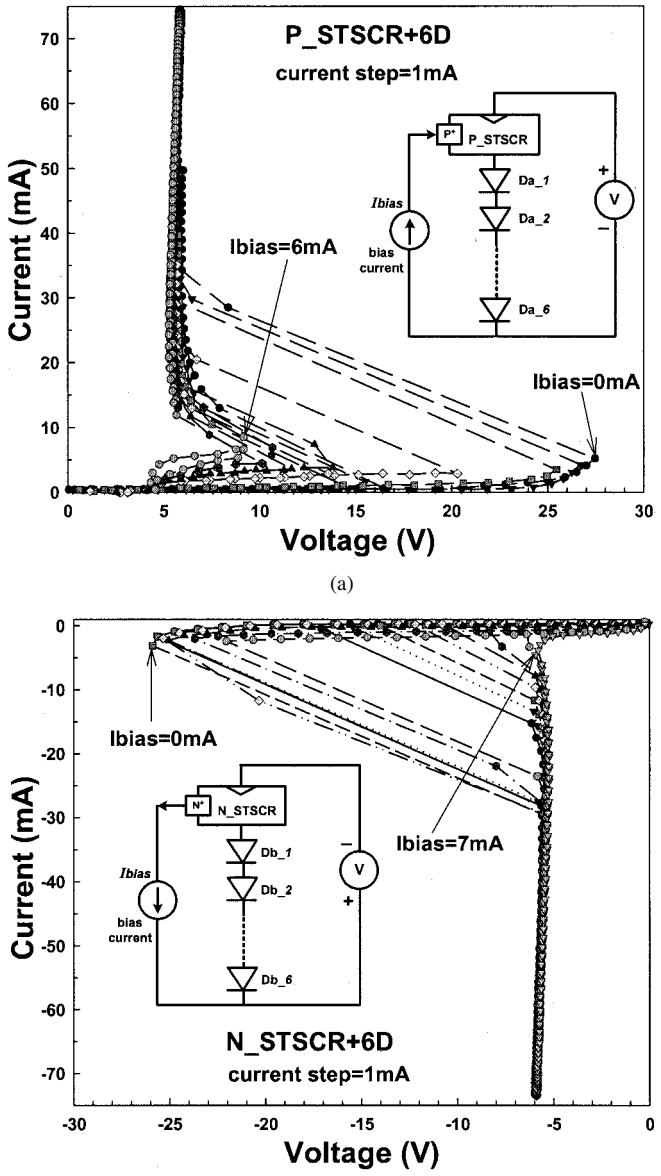


Fig. 7. Measured turn-on I–V curves of (a) the P_STSCR and (b) the N_STSCR with six stacked diodes under different triggered currents.

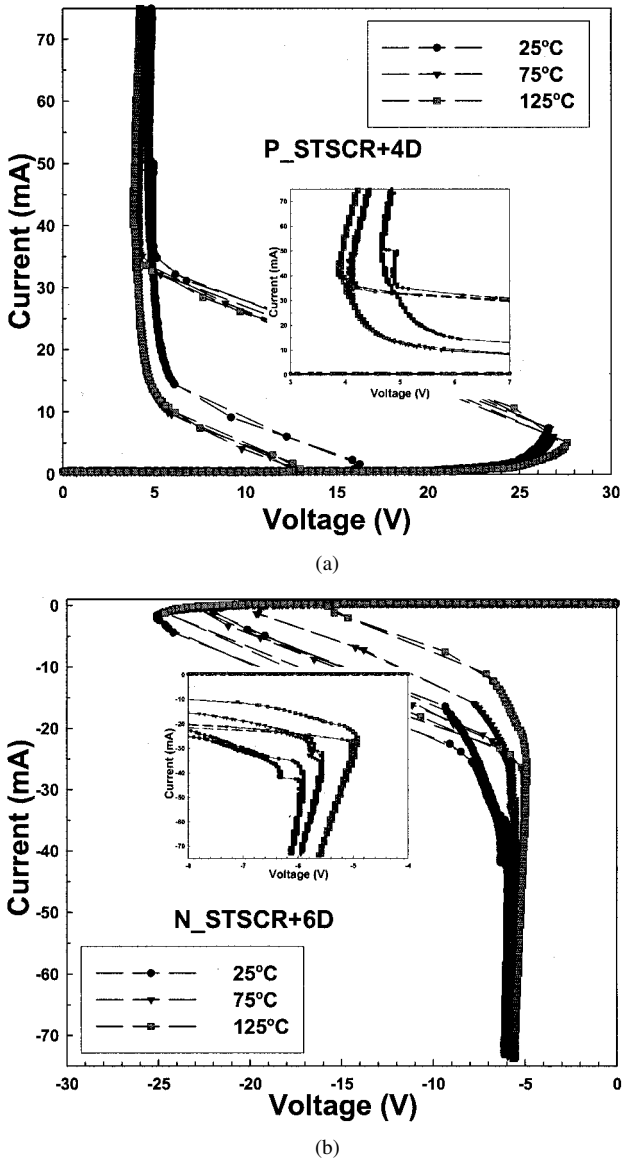


Fig. 8. Measured I–V curves of (a) the P_STSCR with four stacked diodes and (b) the N_STSCR with six stacked diodes under different temperatures.

be stacked with the P_STSCR or N_STSCR devices in the ESD protection circuits to avoid the latchup issue under normal circuit operating conditions.

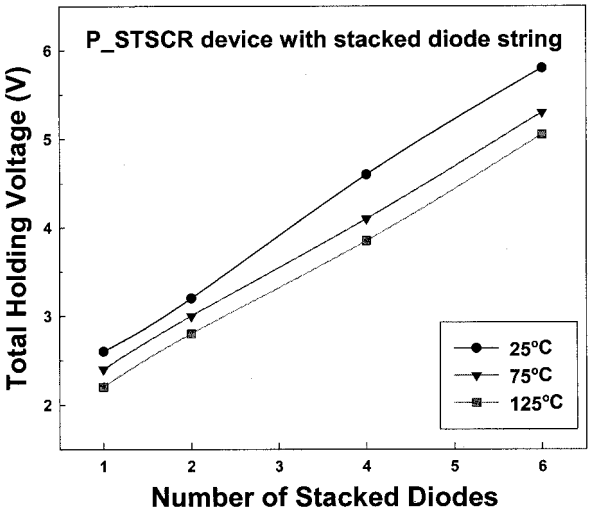
III. On-Chip ESD Protection Circuits With Complementary-STSCR Devices

A. ESD Protection Circuit for the Input/Output Pads

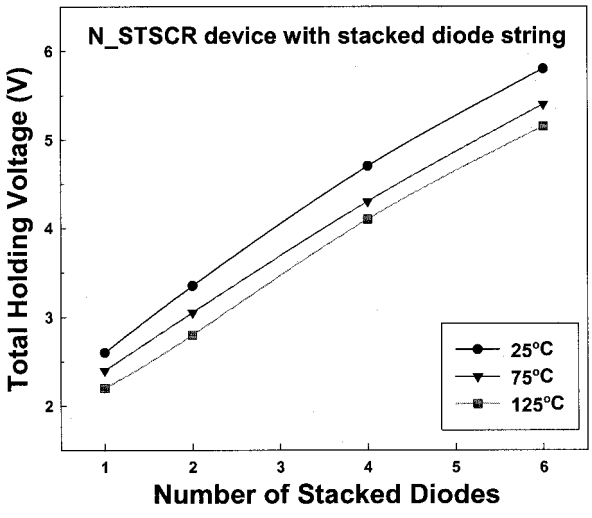
Two kinds of ESD protection designs for I/O pads, realized with the complementary substrate-triggered SCR devices with stacked diode strings, are shown in Fig. 10(a) and (b). In Fig. 10(a), the principle of *RC* delay is used to distinguish ESD-zapping events from the normal circuit operating conditions. In Fig. 10(b), the gate-coupled circuit technique is used to generate the trigger current to turn on the complementary-STSCR devices during ESD-zapping conditions.

In Fig. 10(a), the p-trigger (n-trigger) node of the P_STSCR (N_STSCR) device is connected to the output of the inv_1 (inv_2). The input of the inv_1 (inv_2) is connected to $V_{\rm DD}$ ($V_{\rm SS}$) through the resistor R1 (R2), which is better realized by the n^+ diffusion resistance for the concern of the antenna effect [24]. The resistors R1 and R2 can be shared with every I/O pad to save layout area in the CMOS IC. A capacitor C1 (C2) is placed between the input of the inv_1 (inv_2) and $V_{\rm SS}$ ($V_{\rm DD}$). These capacitors can be formed by the parasitic capacitors at the input node of the inverter. There are also two parasitic diodes (Dp_1 and Dn_1) in this ESD protection circuit. The Dp_1 is the source-to-n-well ($V_{\rm DD}$) parasitic diode of the pMOS in the inv_1. The Dn_1 is the source-to-p-substrate ($V_{\rm SS}$) parasitic diode of the nMOS in the inv_2.

In the normal circuit operating conditions with $V_{\rm DD}$ and $V_{\rm SS}$ power supplies, the input of inv_1 is biased at $V_{\rm DD}$. Therefore, the output of the inv_1 is biased at $V_{\rm SS}$ due to the turn-on of the nMOS in the inv_1, whenever the input signal is logic high

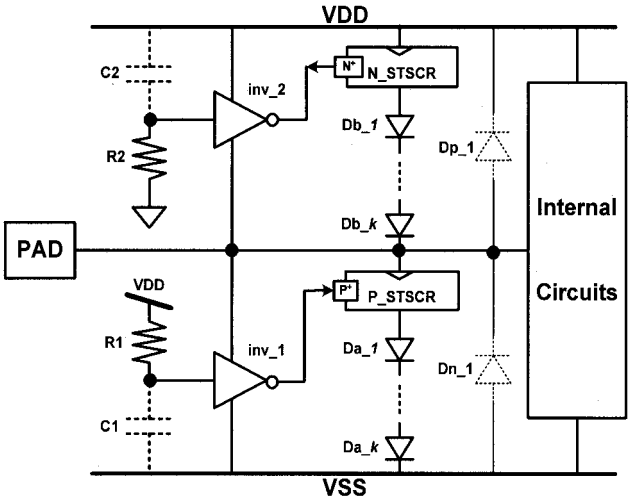


(a)

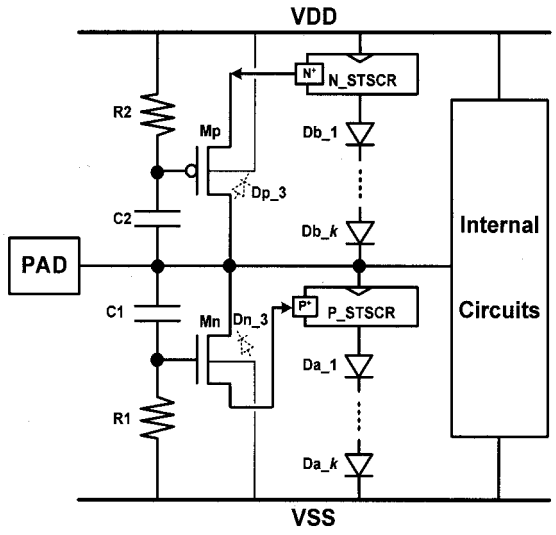


(b)

Fig. 9. Dependence of the total holding voltage of (a) the P_STSCR with stacked diode string and (b) the N_STSCR with stacked diode string on the number of stacked diodes under different temperatures.



(a)



(b)

Fig. 10. Design of ESD protection circuits for the input or output pads with the proposed complementary-STSCR devices and stacked diode strings by using (a) *RC* delay and (b) gate-coupled circuit techniques.

(V_{DD}) or logic low (V_{SS}). The p-trigger node of the P_STSCR device is kept at V_{SS} by the output of the inv_1, so the P_STSCR device is guaranteed to be kept off in the normal circuit operating conditions. The input node of inv_2 in the normal operating conditions is biased at V_{SS}. Thus, the output of the inv_2 is kept at V_{DD} due to the turn-on of the pMOS in the inv_2, whenever the input signal is high or low. The n-trigger node of the N_STSCR device is biased at V_{DD} by the output of the inv_2, so the N_STSCR is also guaranteed to be kept off in the normal circuit operating conditions. To avoid the noise transient-induced latchup issue on such P_STSCR or N_STSCR devices under normal circuit operating conditions, the total holding voltage of the ESD protection device must be designed to be greater than the power supply voltage or maximum voltage level of input signals. By changing the number of stacked diodes, the total holding voltage can be adjusted to meet different circuit applications.

An ESD energy applied on a pad may have the positive or negative voltage with reference to grounded V_{DD} or V_{SS}, so there are four modes of ESD stresses at each I/O pad of CMOS IC products. These four modes of ESD stresses are the PS, NS, PD, and ND modes [14], [15]. To clearly comprehend the ESD current paths under these ESD stresses, the equivalent circuit of the ESD protection circuit designed by complementary-STSCR devices and stacked diode strings for I/O pads is illustrated in Fig. 11. The Dn_2 is the n-well to p-substrate (V_{SS}) parasitic diode in diode Db_k structure. The Dp_2 is the p^+ to n-well parasitic diode in the P_STSCR device structure.

Under the PS-mode ESD-zapping condition (with grounded V_{SS} but floating V_{DD}), the input of the inv_1 is initially floating with a zero voltage level, thereby the pMOS of the inv_1 will be turned on due to the positive ESD voltage on the pad. So the output of the inv_1 is charged up by the ESD energy to generate the trigger current into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR device is triggered on and the ESD current is discharged from the I/O pad to the grounded V_{SS} pin through the P_STSCR device with stacked diode string. The

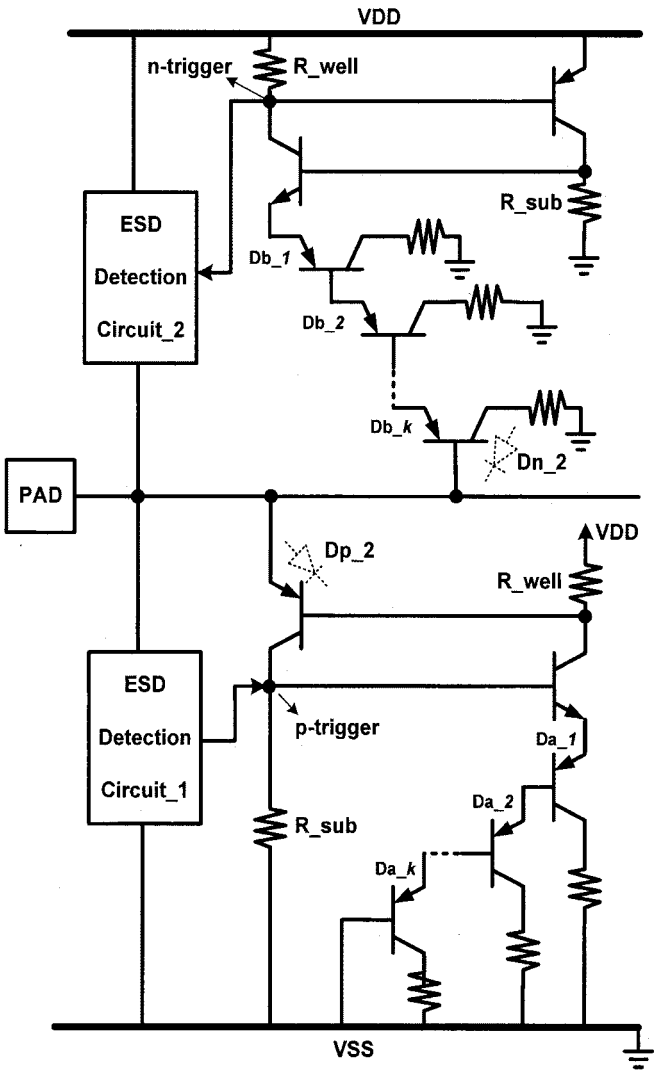


Fig. 11. Equivalent circuit of the complementary-STSCR devices with stacked diode strings for the input and output pads.

RC time constant is designed to keep the input of the inv_1 at a relatively low-voltage level during ESD stress condition, which can be finely tuned by HSPICE simulation.

Under the ND-mode ESD-zapping condition (with grounded $V_{\rm DD}$ but floating $V_{\rm SS}$), the input of the inv_2 is initially floating with a zero voltage level, thereby the nMOS of the inv_2 will be turned on due to the negative ESD voltage on the pad. So the output of the inv_2 is pulled down by the negative ESD voltage to draw the trigger current out from the n-trigger node of the N_STSCR device. Therefore, the N_STSCR device is triggered on and the negative ESD current is discharged from the I/O pad to the grounded $V_{\rm DD}$ pin through the N_STSCR device with stacked diode string.

Under the NS-mode (PD-mode) ESD-zapping condition, the parasitic diodes Dn_1 and Dn_2 (Dp_1 and Dp_2) are forward biased and turned on to discharge the ESD current from the I/O pad to the grounded $V_{\rm SS}$ ($V_{\rm DD}$). Thus, the four modes (PS, NS, PD, and ND) of ESD stresses can be clamped to a very low-voltage level by the P_STSCR with stacked diode string, Dn_1, Dn_2, Dp_1, Dp_2, and N_STSCR with stacked diode string, so the thin gate oxide in deep sub-quarter-micrometer CMOS technologies can be fully protected. In addition, the ESD level of an I/O pin is dominated by the weakest ESD current path, so the experimental measurements in the following are focused on the PS-mode and ND-mode ESD-zapping conditions.

Fig. 10(b) shows another ESD protection circuit designed with the complementary-STSCR devices with stacked diode string for the I/O pad. When a PS-mode ESD-zapping on the pad occurs, the positive transient voltage on the pad is coupled through the capacitor C1 to the gate of nMOS Mn. The Mn with a positive coupled gate bias can be turned on to conduct some ESD current from the I/O pad into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR is triggered on to discharge the ESD current from the I/O pad to the grounded $V_{\rm SS}$ pin. When an ND-mode ESD-zapping on the pad occurs, the negative transient voltage on the pad is coupled through the capacitor C2 to the gate of pMOS Mp. The Mp with a negative coupled gate bias can be turned on to draw some ESD current out from the n-trigger node of the N_STSCR device. Therefore, the N_STSCR is triggered on to discharge the negative ESD current from the I/O pad to the grounded $V_{\rm DD}$ pin. When the NS-mode (PD-mode) ESD-zapping on the pad occurs, the ESD current can be bypassed through the forward-biased parasitic diodes Dn_2 and Dn_3 (Dp_2 and Dp_3) to grounded $V_{\rm SS}$ ($V_{\rm DD}$). The Dn_3 (Dp_3) is the parasitic diode in the drain of Mn (Mp) to the p-substrate (n-well). During normal circuit operating conditions, the gate of Mn (Mp) is biased at $V_{\rm SS}$ ($V_{\rm DD}$) through the resistor R1 (R2). So the Mn (Mp) is kept off and no trigger current will be applied to the trigger node of P_STSCR (N_STSCR). The ESD protection circuits are designed to be inactive without interrupting the normal input or output signals. The capacitance values of C1 and C2 in Fig. 10(b) must be tuned at some value, where the coupled voltage under normal circuit operating conditions is smaller than the threshold voltage of Mn/Mp, but greater than the threshold voltage of Mn/Mp under ESD-zapping conditions [25].

B. ESD Clamp Circuit Between the Power Rails

The $V_{\rm DD}$-to-$V_{\rm SS}$ ESD clamp circuit realized with the P_STSCR device and the stacked diode string is shown in Fig. 12. The function of the ESD detection circuit, which is formed with resistor, capacitor, and inverter, is similar to that used in the I/O pad, but the *RC* value is designed with a time constant of about $\sim$ 1μs to distinguish the $V_{\rm DD}$ power-on event (with a rise time in milliseconds) or ESD stress events (with a rise time in nanoseconds) [10]. During the normal $V_{\rm DD}$ power-on transition (from low to high), the input of the inverter in Fig. 12 can follow up in time with the power-on $V_{\rm DD}$ voltage to keep the output of the inverter at zero. Hence, the P_STSCR device with stacked diode string is kept off, and does not interfere with the functions of the internal circuits.

When a positive ESD voltage is applied to the $V_{\rm DD}$ pin with the $V_{\rm SS}$ pin relatively grounded, the *RC* delay will keep the input of the inverter at a low-voltage level for a relatively long time. Therefore, the output of the inverter will be pulled high by the ESD energy to trigger on the P_STSCR device. While the P_STSCR device is triggered on, the ESD current is discharged from the $V_{\rm DD}$ pin to the $V_{\rm SS}$ pin through the P_STSCR device

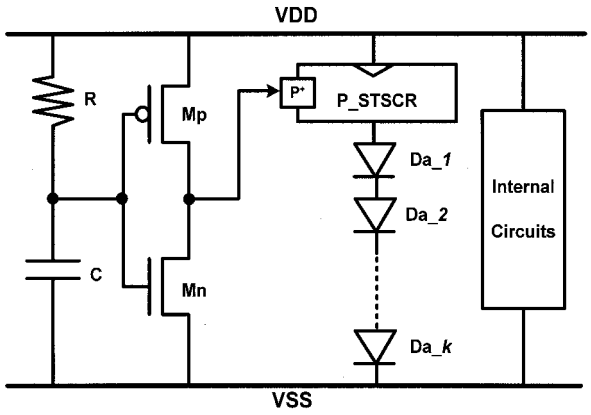


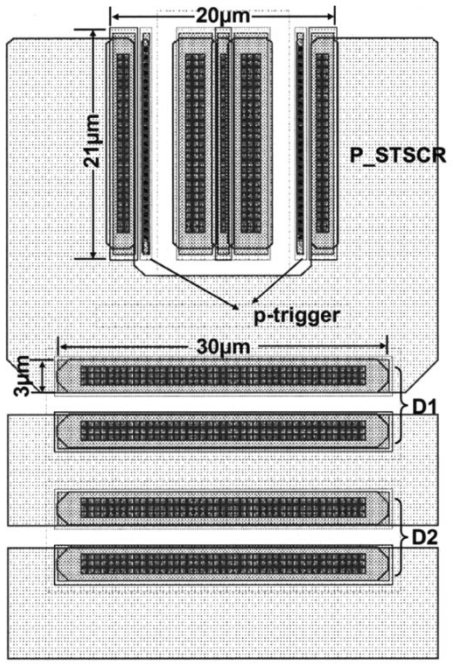
Fig. 12. $V_{\rm DD}$-to-$V_{\rm SS}$ ESD clamp circuit realized with P_STSCR and stacked diode string.

and the stacked diode string. With such a suitable ESD detection circuit, the P_STSCR device can be quickly triggered on to discharge the ESD current. When a negative ESD voltage is applied to the $V_{\rm DD}$ pin with the $V_{\rm SS}$ pin relatively grounded, the negative ESD current can be discharged from the $V_{\rm DD}$ pin to the $V_{\rm SS}$ pin through the forward-biased P-substrate ($V_{\rm SS}$)-to-n-well (which is connected to $V_{\rm DD}$) parasitic diode. In addition, by adjusting the number of stacked diodes, such power-rail ESD clamp circuits can be designed free of the latchup issue. With a suitable ESD detection circuit, the N_STSCR device can be also designed for the power-rail ESD clamp circuit.

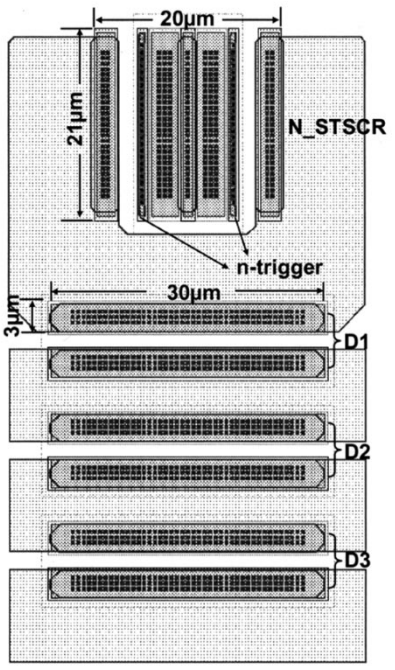
IV. Experimental Results

A. ESD Robustness

The proposed ESD protection devices and circuits for the I/O and the power pads have been fabricated in a 0.25-μm salicided CMOS process without using the additional silicide-blocking mask/process option. The layout examples of the P_STSCR device with two stacked diodes and the N_STSCR device with three stacked diodes are shown in Fig. 13(a) and (b), respectively. The device dimensions of the fully silicided P_STSCR and N_STSCR are 20 μm $\times$ 21 μm, and each diode has a 30 μm $\times$ 3 μm anode layout area. The human body model (HBM) and machine model (MM) ESD stresses are used to verify the ESD levels of the proposed ESD protection circuits designed with the complementary-STSCR devices and different numbers of the stacked diodes. The HBM and MM ESD test results of the P_STSCR/N_STSCR with stacked diode string are compared in Fig. 14(a) and (b), respectively. In this ESD verification, the failure criterion is defined as the leakage current of the device after ESD zapping is greater than 1 μA under the normal operating voltage of 2.5 V. The HBM (MM) ESD levels of the P_STSCR/N_STSCR with stacked diode string have little degradation while the number of stacked diodes is increased. The ESD-generated power across the ESD protection device can be calculated as Power $\cong I_{\rm ESD} \times V_{\rm hold}$. Thus, the HBM and MM ESD levels are decreased in principle when the total holding voltage is increased. But the stacked diode string with the parasitic vertical p-n-p BJT structures will also generate the extra current paths. These extra current paths can be also used to discharge the ESD current. So the HBM and MM ESD levels



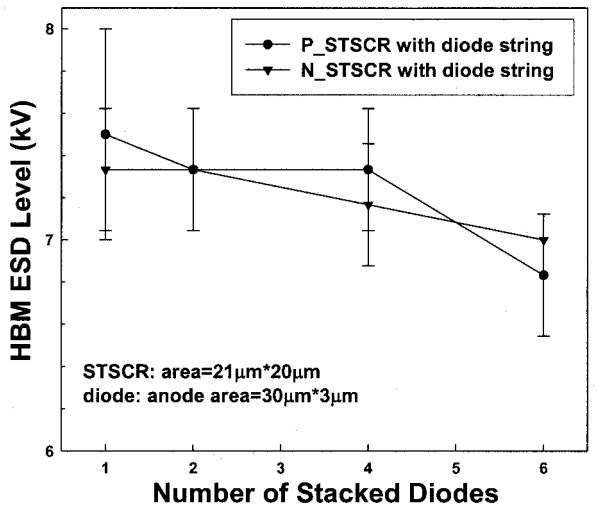
(a)



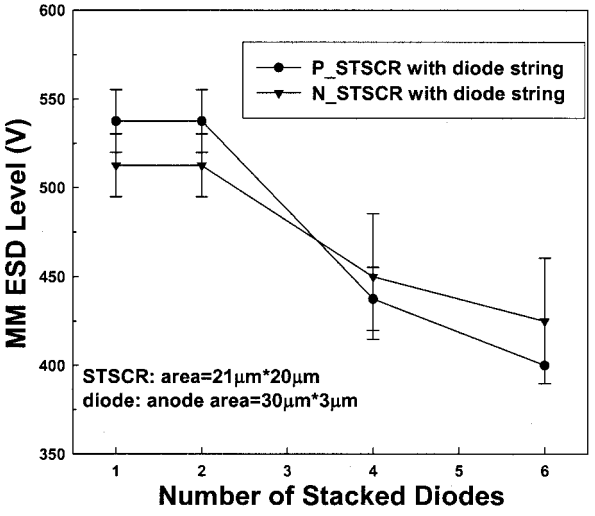
(b)

Fig. 13. Layout top views of (a) the P_STSCR with two stacked diodes and (b) the N_STSCR with three stacked diodes in a 0.25-μm salicided CMOS process.

of the P_STSCR/N_STSCR with stacked diode strings can almost be kept at the same value. For IC applications with power supply of 2.5 V, the ESD protection circuit can be free of the latchup issue even if the operating temperature is up to 125 °C, when the number of stacked diodes is two. The complementary-STSCR devices with two stacked diodes can still sustain the HBM (MM) ESD level of 7.25 kV (500 V). The ESD levels of substrate-triggered SCR devices are the same as that of the traditional SCR device under the same layout area. The aim of



(a)



(b)

Fig. 14. Dependence of the (a) HBM and (b) MM ESD levels of the complementary-STSCR devices with stacked diode strings on the number of the stacked diodes (Failure criterion: $I_{\rm Leakage} > 1\ \mu$A at 2.5-V bias).

this work is to reduce the switching voltage, to avoid the transient-induced latchup issue, and to enhance the turn-on speed of the SCR device.

By comparison, a gate-grounded NMOS (GGNMOS) device with $W/L = 200/0.5$ has been fabricated in the same CMOS process with additional silicide-blocking mask. This GGNMOS occupied a layout area of 25.8 μm $\times$ 60 μm can sustain the HBM ESD level of 3.5 kV. This has verified the excellent area efficiency of the ESD protection circuits realized with the proposed complementary-STSCR devices (8 V/μm^2 for the complementary-STSCR with two stacked diodes, as compared with 2.71 V/μm^2 for GGNMOS).

B. Turn-On Verification

The comparison of turn-on speed between P_STSCR and LVTSCR [13] under an applied 0–8-V voltage pulse is shown in Fig. 15. The device dimension W/L of the inserted nMOS in the LVTSCR structure is 40 μm/0.25 μm, and the device area of the P_STSCR is the same as that shown in Fig. 13(a).

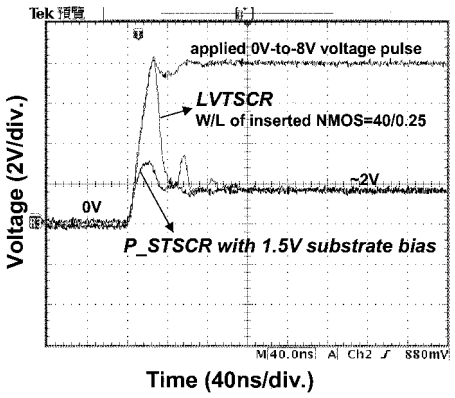


Fig. 15. Comparison of turn-on time between LVTSCR and P_STSCR under an applied 0–8-V voltage pulse.

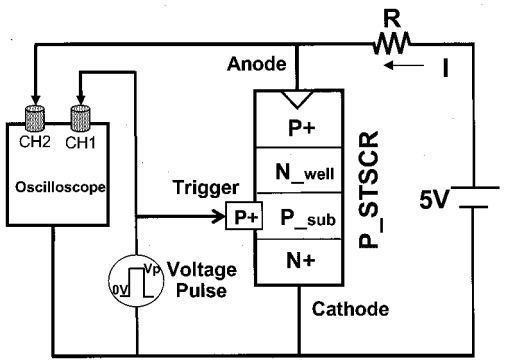


Fig. 16. Experimental setup to measure the turn-on time of the stand-alone P_STSCR device.

The 8-V voltage pulse can be more quickly clamped to a stable low-voltage level by the P_STSCR with 1.5-V substrate bias than by the LVTSCR. In order to investigate the turn-on time of the complementary-STSCR devices, the experimental setup to measure the corresponding turn-on time of the P_STSCR device is illustrated in Fig. 16. The turn-on time of the complementary-STSCR devices is defined as the corresponding time from triggering state to latching state. The measured results in the time domain are shown in Fig. 17, where the V_anode (V_trigger) is the voltage waveform on the anode (trigger) of the P_STSCR shown in Fig. 16. The anode of the P_STSCR device is biased at 5 V through the resistance R of 47 Ω, which is used to limit the sudden large transient current from power supply, when the P_STSCR is turned on. A voltage pulse with a pulsewidth of 400 ns and a rise time of $\sim$10 ns, which corresponds to the rise time of the HBM ESD event, is applied to the trigger node. While a voltage pulse of 1 V is applied to the trigger node, the V_anode has no change, as shown in Fig. 17(a). So, the P_STSCR device has at least a substrate noise margin of 1 V. The V_anode, however, is triggered into latching state while the pulse voltage is increased to 2 V, as shown in Fig. 17(b). The forward-biased p-trigger node to cathode in the P_STSCR device limited the full swing of the 2-V voltage waveform shown in Fig. 17(b). After the triggering of the 2-V voltage pulse, the V_anode is still kept at a low-voltage level of $\sim$2.5 V. The P_STSCR device has been successfully triggered on to provide a low-impedance path from

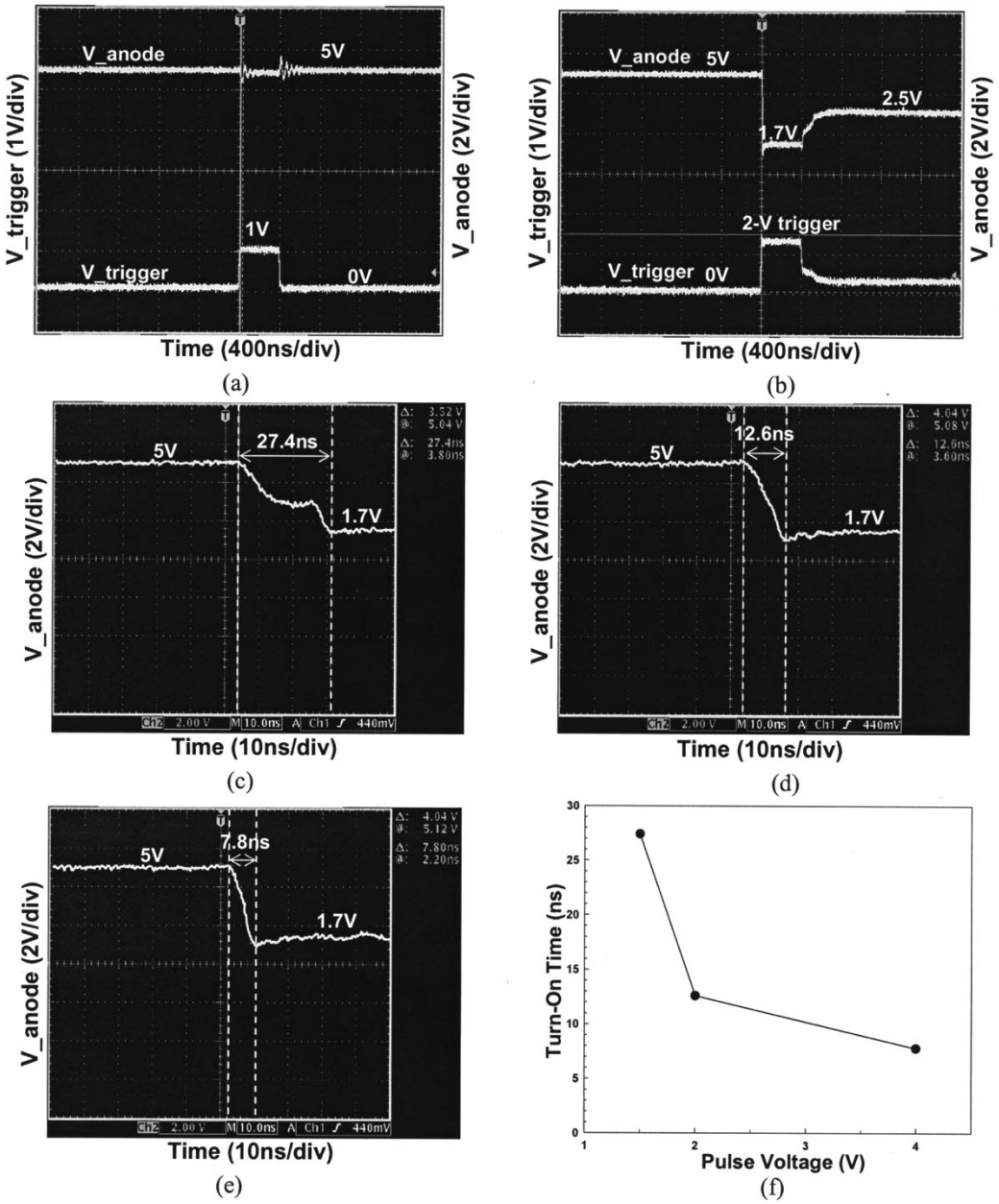


Fig. 17. Turn-on verification of the P_STSCR device under different substrate biases. The measured voltage waveforms on the anode and trigger nodes of the P_STSCR device under (a) 1-V voltage triggering and (b) 2-V voltage triggering. The close-up views of the V_anode at the falling edge while the P_STSCR is triggering by the voltage pulse of (c) 1.5 V, (d) 2 V, and (e) 4 V, into the p-trigger node. (f) The relation between the turn-on time and the triggering pulse voltage.

its anode to its cathode. The turn-on time for the P_STSCR device into its latching state is observed by the close-up views of the V_anode waveform at the falling edge, which are shown in Fig. 17(c) to (e) under different triggering voltage pulses. The dependence of the turn-on time of such P_STSCR device on the pulse height of the triggering voltage pulse is compared in Fig. 17(f). In Fig. 17(f), the turn-on time of the P_STSCR device can be reduced from 27.4 to 7.8 ns, which is faster than the rise time ($\sim$10 ns) of the HBM ESD pulse, while the pulse height of the triggering voltage pulse is increased from 1.5 to 4 V. The turn-on speed is improved by a factor of about four. The measured results have confirmed that the proposed ESD protection circuit can indeed be turned on more quickly to discharge the ESD current, which can provide more effective protection for internal circuits as long as enough substrate bias is supplied.

The ESD protection circuits are kept off under normal circuit operating conditions and triggered on under ESD-zapping conditions. In order to verify the functions of the ESD protection circuit for the I/O pad, a 2.5-V voltage pulse with a pulsewidth of 400 ns and a rise time of 10 ns is applied to the I/O pad in Fig. 10(a), where only one P_STSCR/N_STSCR device is placed between the I/O pad and $V_{\rm SS}/V_{\rm DD}$ in this verification. In this experimental measurement, the ESD detection circuit including *R*, *C*, and inverter is realized with $R = 100$ kΩ, $C = 3$ pF, pMOS dimension $W/L = 50/0.5$, and nMOS dimension $W/L = 30/0.5$. The channel length of nMOS/pMOS in the ESD detection circuit can be reduced to gain the higher triggered

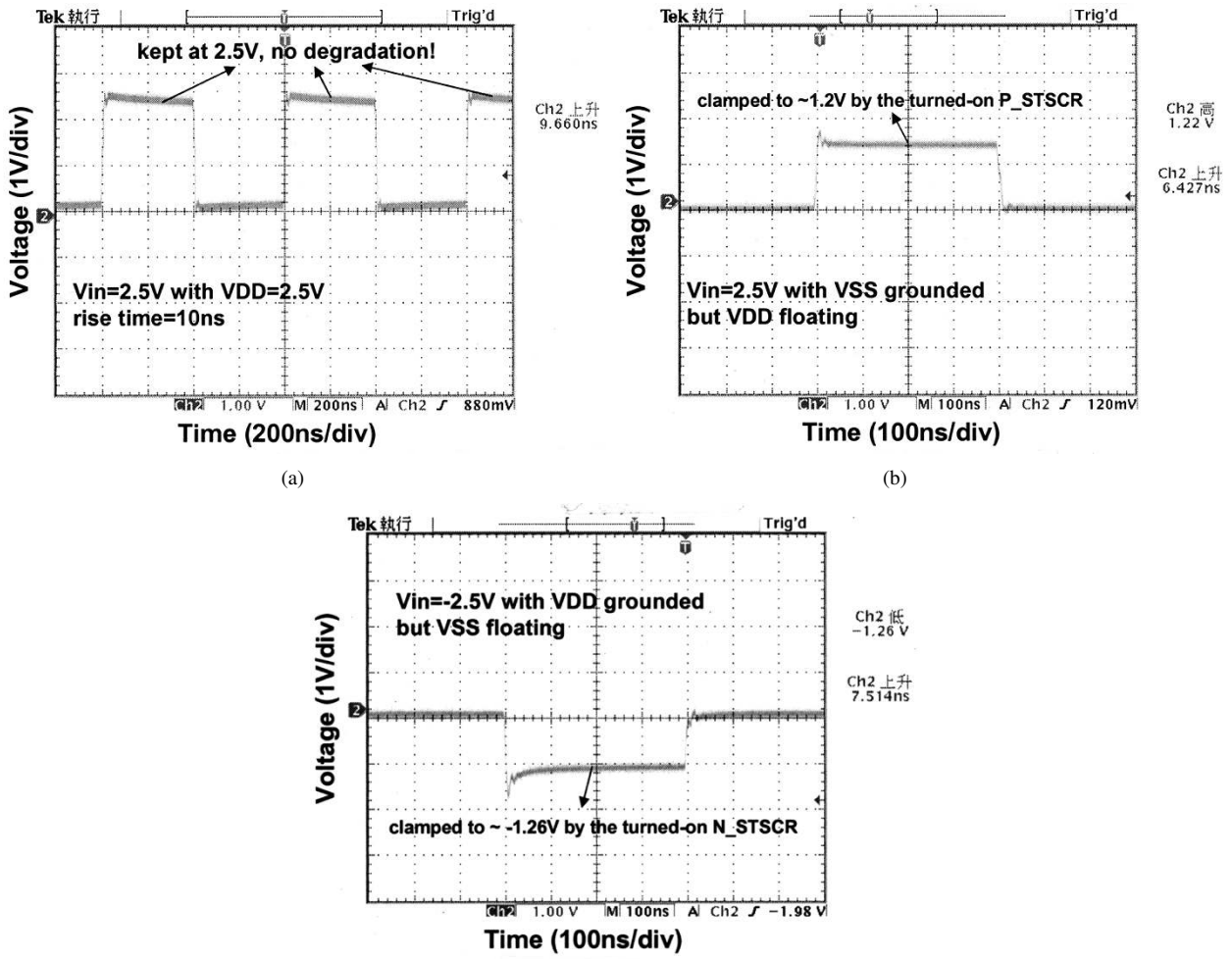
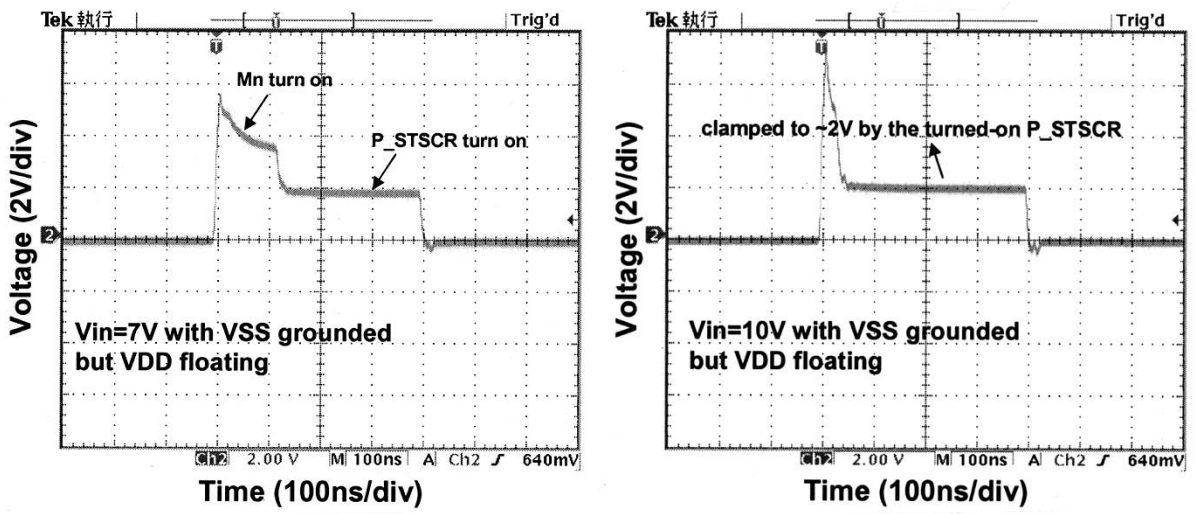


Fig. 18. Measured voltage waveforms on the I/O pad of Fig. 10(a) under (a) the normal circuit operating conditions, (b) the positive-to-V_{SS} ESD-zapping condition when a 2.5-V voltage pulse is applied to the I/O pad, and (c) the negative-to-V_{DD} ESD-zapping condition when a -2.5-V voltage pulse is applied to the I/O pad.

currents. These device dimensions can be finetuned by HSPICE simulator to fit different circuit applications. During the normal circuit operating conditions, where the V_{DD} is power-on and V_{SS} is connected to ground, the input signal of 2.5 V has no degradation, as shown in Fig. 18(a). So the ESD protection circuit does not interfere with the input signal. However, during the PS-mode ESD-zapping condition, the ESD detection circuit is active, so the applied voltage pulse of 2.5 V is clamped to $\sim$1.2 V by the turned-on P_STSCR, as shown in Fig. 18(b). During ND-mode ESD-zapping condition, a -2.5-V voltage pulse is clamped to ~ -1.26 V by the turned-on N_STSCR, as shown in Fig. 18(c). By using this method, the turn-on characteristics of the ESD protection circuit for the I/O pad shown in Fig. 10(b) can also be verified. In this measurement, the ESD detection circuit including *C*, *R*, and nMOS/pMOS is realized with $C = 96$ fF, $R = 10$ kΩ, nMOS dimension $W/L = 30/0.5$, and pMOS dimension $W/L = 50/0.5$. When a positive 0–7-V voltage pulse to simulate the PS-mode ESD-zapping condition is applied to the I/O pad of the ESD protection circuit in Fig. 10(b), the voltage waveform on the I/O pad is clamped to a low-voltage level measured in Fig. 19(a). In Fig. 19(a), the nMOS, Mn in the ESD protection circuit of Fig. 10(b), will be first turned on to conduct some ESD current to trigger on the P_STSCR device, and then the P_STSCR clamps the voltage to 1.8 V. If the pulse voltage is increased to 10 V, as shown in Fig. 19(b), the turn-on time of Mn can be shortened and the P_STSCR can be triggered into latching state more quickly. In Fig. 19(c), when a negative 0–10-V voltage pulse to simulate the ND-mode ESD-zapping condition is applied to the I/O pad of the ESD protection circuit in Fig. 10(b), the voltage waveform is clamped to a low-voltage level (~ -1.8 V) by the turned-on N_STSCR device. The measured results match the results shown in Fig. 17. The higher voltage pulse will generate the higher substrate bias through Mn or Mp. So the P_STSCR and N_STSCR can be triggered into the latching state more quickly by increasing the pulse voltage. This has verified the effectiveness of the proposed ESD protection circuits designed with the substrate-triggered technique and the SCR devices. To achieve the latchup-free condition, some diodes must be stacked with the substrate-triggered SCR devices in the ESD protection circuits.

To verify the latchup-free property, another measurement of the holding voltages of the complementary-STSCR devices with stacked diode strings is tested under transient conditions. The turn-on behavior of the power-rail ESD clamp circuit realized with the *R*, *C*, inverter, and P_STSCR with stacked diode strings is shown in Fig. 20. A 0–5-V voltage pulse with a



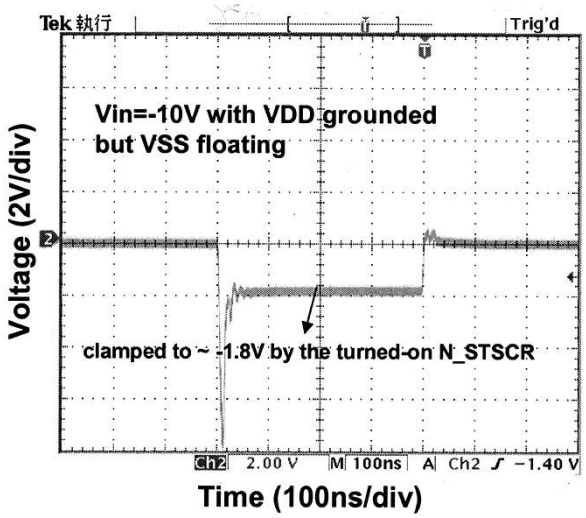


Fig. 19. Measured voltage waveforms on the I/O pad of Fig. 10(b) under (a) the 7-V positive-to-V_{SS} ESD-zapping condition, (b) the 10-V positive-to-V_{SS} ESD-zapping condition, and (c) the -10-V negative-to-V_{DD} ESD-zapping condition.

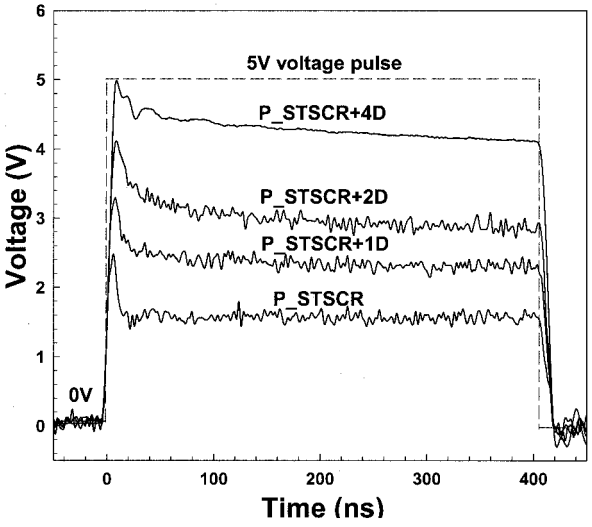


Fig. 20. Voltage waveforms clamped by the V_{DD}-to-V_{SS} ESD clamp circuit designed with the P_STSCR device and different numbers of stacked diodes, when a 0–5-V voltage pulse is applied.

pulsewidth of 400 ns and a rise time of 10 ns is applied to the V_{DD} pin of Fig. 11(a) to simulate the PS-mode ESD-zapping condition. The voltage pulse applied on the V_{DD} pin is clamped to 1.6, 2.4, 3, and 4.3 V by the ESD protection circuit realized with ESD detection circuit, P_STSCR, and zero, one, two, and four diodes, respectively. When the voltage pulse is applied to the V_{DD} pin, the voltage pulse is quickly clamped to a low-voltage level within only a few nanoseconds. The clamped voltage level of the ESD protection circuit can be linearly adjusted by changing the number of stacked diodes for practical applications in CMOS IC products with different V_{DD} voltage levels. For IC applications with V_{DD} of 2.5 V, the P_STSCR with two stacked diodes has a clamped voltage of about 3 V, so it can be free of the latchup issue.

V. Conclusion

Latchup-free on-chip ESD protection circuits realized with complementary substrate-triggered SCR devices have been successfully investigated in a 0.25-μm salicided CMOS

process. By using the substrate-triggered technique, the ESD protection circuits with complementary-STSCR devices and stacked diodes have the advantages of controllable switching voltage, adjustable holding voltage, fast turn-on speed, high ESD robustness in a smaller layout area, and freedom from latchup issue. The experimental result has shown that the turn-on time of STSCR can be reduced from 27.4 to 7.8 ns by the substrate-triggering technique. For the IC applications with $V_{\rm DD}$ of 2.5 V, the ESD protection circuits designed with complementary-STSCR devices and two stacked diodes can sustain the HBM (MM) ESD level of ~7.25 kV (500 V) in a 0.25-μm fully salicided CMOS process without using extra process modification.

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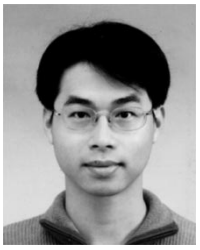
Ming-Dou Ker(S'92–M'94–SM'97) received the B.S. degree in electronics engineering and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

In 1994, he joined the VLSI Design Department of Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan, as a Circuit Design Engineer. In 1998, he became a Department Manager in the VLSI Design Division of CCL/ITRI. In 2000, he became an Associate Professor in the Department of Electronics Engineering, National Chiao-Tung University. In the field of reliability and quality design for CMOS integrated circuits, he has published over 150 technical papers in international journals and conferences. He holds 130 patents on reliability and quality design for integrated circuits, including 53 U.S. patents. His inventions in ESD protection design and latchup prevention have been widely used in modern IC products. He has been invited to teach or aid in ESD protection design and latchup prevention by more than 150 IC design houses and semiconductor companies in the Science-Based Industrial Park, Hsinchu, Taiwan, and in Silicon Valley, San Jose, CA. He has been a member of the Technical Program Committees and Session Chair of many international conferences. He was elected as the first President of Taiwan ESD Association in 2001. His research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed or mixed-voltage I/O interface circuits, especial sensor circuits and semiconductors.

Dr. Ker has received many research awards from ITRI, the National Science Council, and National Chiao-Tung University, and the Dragon Thesis Award from the Acer Foundation.



Kuo-Chun Hsu (S'01) was born in Taiwan in 1976. He received the B.S. degree from the Department of Electronics Engineering, National Chung-Hsing University, Taichung, Taiwan, R.O.C., in 1998 and the Master's degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 2000. He is currently working toward the Ph.D. degree at the Institute of Electronics, National Chiao-Tung University.

His current research interests include ESD physics, semiconductor devices, and ESD protection design in deep-submicrometer CMOS technologies.