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Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics

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ABSTRACT

We report a general approach for three-dimensional (3D) multifunctional electronics based on the layer-by-layer assembly of nanowire (NW) building blocks. Using germanium/silicon (Ge/Si) core/shell NWs as a representative example, ten vertically stacked layers of multi-NW field-effect transistors (FETs) were fabricated. Transport measurements demonstrate that the Ge/Si NW FETs have reproducible high-performance device characteristics within a given device layer, that the FET characteristics are not affected by sequential stacking, and importantly, that uniform performance is achieved in sequential layers 1 through 10 of the 3D structure. Five-layer single-NW FET structures were also prepared by printing Ge/Si NWs from lower density growth substrates, and transport measurements showed similar high-performance characteristics for the FETs in layers 1 and 5. In addition, 3D multifunctional circuitry was demonstrated on plastic substrates with sequential layers of inverter logical gates and floating gate memory elements. Notably, electrical characterization studies show stable writing and erasing of the NW floating gate memory elements and demonstrate signal inversion with larger than unity gain for frequencies up to at least 50 MHz. The ability to assemble reproducibly sequential layers of distinct types of NW-based devices coupled with the breadth of NW building blocks should enable the assembly of increasing complex multilayer and multifunctional 3D electronics in the future.

Over the past several years, semiconductor NWs[1,2] and carbon nanotubes[3] have been actively explored as the potential materials for future electronic components. These chemically derived single-crystalline nanostructures present unique advantages over conventional semiconductors, as they enable integration of high-performance device elements onto virtually any substrate[4−6] with scaled on-currents and switching speeds higher than state-of-the-art planar Si structures.[7,8] These unique electrical properties and the intrinsically miniaturized dimensions of NW and carbon nanotube building blocks may facilitate the continuation of Moore's law and the evolutionary quest for ever faster and smaller electronics well into the future. More uniquely, the capability of assembling high-performance NW building blocks with diverse functional properties could enable novel circuit concepts such as 3D integrated electronics,[9] where 3D structure arises from sequential assembly[10−12] of NWs into vertically stacked device layers.

Indeed, there has been considerable interest in multilayer electronics, as they offer a more efficient interconnection and processing of digital information.[13−15] However, materials- and fabrication-related challenges have presented major obstacles in achieving truly 3D integrated circuits based on the conventional Si CMOS technology, and the need for a new technology remains critical. Here, we report the monolithic integration of individual and parallel arrays of crystalline NWs as multifunctional and multilayer circuits, consisting of up to 10 addressable vertical layers, through a simple "bottom-up" and "top-down" hybrid methodology. A similar approach involving sequential printing of NWs and nanotubes was reported very recently by Rogers and coworkers for up to three layer structures.[16] These new assembly-based approaches overcome processing limitations of conventional planar CMOS technology and thus could make them formidable methods for the future high-performance 3D integrated circuits.

Rational integration of NWs into functional circuits requires that they be assembled with controlled orientation and density at spatially defined locations on the device

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Figure 1. Overview of 3D NW circuit integration. (a) Contact printing of NWs from growth substrate to prepatterned substrate. In general, NWs are grown with random (nonepitaxial) orientation and are well-aligned by sheer forces during the printing process. (b) Three-dimensional NW circuit is fabricated by the iteration of the contact printing, device fabrication, and separation layer deposition steps *N* times.

substrate. Previously, we have reported two solution-phase methods for assembling aligned and controlled density arrays of NWs on substrates, including flow-directed and Langmuir−Blodgett techniques.[10−12] While success has been achieved with these approaches for assembling single-layer arrays of functional NW devices using 20−40 nm diameter NWs,[17] these methods have been less successful with small ($<\sim$15 nm) diameter NWs.

To overcome this limitation, we have developed a new dry deposition strategy that enables oriented and patterned assembly of NWs with controlled density and alignment films on substrates, from Si to plastics. The overall process involves (i) optimized growth of designed NWs by nanocluster directed growth[1,2,18−20] and (ii) patterned transfer of NWs directly from a NW growth substrate to a second device substrate via contact printing, as illustrated in Figure 1a.[21] Specifically, a photolithographically patterned device substrate is first firmly attached to a benchtop, and the NW growth substrate is placed upside down on top of the patterned device substrate such that the NWs are in contact with the device substrate. A gentle manual pressure is then applied from the top followed by sliding the growth substrate 1−3 mm. Finally, the growth substrate is removed. Devices and circuits are then fabricated on the printed arrays of NWs using conventional top-down lithography and metallization processes.[6,17] To elaborate a 3D structure, the NW printing and device fabrication steps are iterated multiple times, along with the deposition of an intervening insulating SiO_2 buffer layer, in order to obtain vertically stacked electronic layers (Figure 1b). This process is general for the wide range of reported NW materials and device designs,[1,2] and moreover, the simplicity and the low processing temperature requirement of the method make it ideal for achieving high-performance 3D integrated circuitry with different functionalities in distinct layers.

Figure 2. Three-dimensional NW FETs. (a) Optical microscope image shows the array of NW FETs. (b) Dark field image demonstrates a parallel array of NWs is aligned between source (S), drain (D), and top gate (G) electrodes. (c) $I-V_{gs}$ characteristics of 40 NW FETs. (d) Transfer characteristics of the first layer NW FET before and after second layer fabrication. (e) Optical microscope image of 10 layers of Ge/Si NW FETs. Each device is offset in *x* and *y* to facilitate imaging. (f) Current vs drain-source voltage characteristics (with 1.5 V gate step) for NW FETs from layers 1, 5, and 10.

We first fabricated single-layer arrays of multi-NW FETs[6,22,23] using printed Ge/Si NW heterostructures ($\sim$10 nm thick core with $\sim$2 nm shell) as the channel material (Figure 2a,b). The Ge/Si NWs, which have higher performance than that of the state-of-the-art planar Si structures,[8] were configured as top-gated devices with channel width and length of 200 and 2 μm, respectively, and a high-κ HfO_2 gate dielectric.[8,22] Optical and scanning electron microscopy images of the Ge/Si NW FET arrays (Figure 2a,b) demonstrate several key features. First, the NWs are cleanly printed only at lithographically predefined locations on the substrates. Second, the contact printed NWs are aligned and uniform across millimeter and larger length scales. Third, the NWs are assembled with relatively high densities ($\sim$4 NW/μm). The local alignment and density is further confirmed by scanning electron microscopy images (inset, Figure 2b). These features of our methodology lead to well-defined and reproducible FET structures over large substrate areas.

The current versus gate-voltage ($I-V_{gs}$) transfer characteristics recorded from an array of 40 Ge/Si FETs fabricated on the same chip is shown in Figure 2c.[24] Notably, the FETs show minimal variation in the threshold voltage and exhibit a large average on-current of 4 mA with a 1-standard deviation variation of only 15%. We attribute this good device-to-device reproducibility to the uniformity of the contact printed Ge/Si NWs and averaging of NW-to-NW variations in the multi-NW devices. Reproducible device behavior is one of the most crucial goals for the nanomaterial building blocks for integrated circuits.[5,6] To achieve reliable 3D integration, it is also essential that the layer-by-layer assembly and fabrication process does not alter the electrical properties of previous layers. Figure 2d shows the transfer characteristics of a first-layer FET with a multi-NW channel before and after the vertical stacking of the second layer, where the $I-V_{gs}$ data show no significant change of the on-current. These results demonstrate that the assembly and fabrication steps involved in adding layers have little or no effect on the device properties, thus making our methodology highly compatible with monolithic 3D integration of various NW electronic layers on a single chip.

To explore 3D integration, we first assembled and fabricated a structure consisting of 10 layers of Ge/Si multi-NW FETs on a Si substrate, as shown in Figure 2e. The optical image shows clearly the source, drain, gate electrode structure of FETs in each of the 10 layers, which were offset in x and y from layer-to-layer for clarity. Optical interference further leads to distinct colors in the upper layers and testifies to the high quality of our structures. In addition, the current versus drain source voltage ($I-V_{ds}$) output characteristics of the NW FETs in layers 1, 5, and 10 for the assembled 3D structure were characterized as shown in Figure 2f. Notably, the 3D NW FET structure exhibits consistent layer-to-layer electrical properties with on-currents of ca. 3 mA and maximum transconductance, g_m, of ca. 1 mS. These data demonstrate the reproducibility and reliability of our assembly and fabrication process for individual device layers and the ability to vertically stack these layers without performance degradation.

Our 10-layer NW 3D electronic structure consists of the highest number of functional device layers that have been vertically stacked and reported with any single-crystalline channel material to date.[16,25−29] Recent studies using a similar transfer printing of nanomaterials has produced up to three layers with electrical measurements,[16] a factor of 3 less than in this work. In planar Si technology, it has been difficult to achieve true 3D integrated structures, due in part to materials-related challenges associated with high-temperature processing needed to produce single-crystalline silicon. This challenge has been circumvented through wafer-to-layer bonding[25−27] and incorporation of poly-Si as the active channel material,[28,29] although both approaches have limitations. Our approach represents a unique opportunity for exploring high-performance 3D integrated circuitry owing to fact that higher temperature materials growth, which enables single-crystalline functional NWs, is independent of the their low processing assembly and fabrication steps used to complete each active electronic layer.

Figure 3. Three-dimensioal integration of single-NW FETs. (a) Optical microscope images shows single NW FETs with multiple sources and a common drain with a top gate. (b) $I-V_{ds}$ (with 1 V gate step) of single-NW FETs on layers 1 and 5. (c) $I-V_{gs}$ for single-NW devices on layers 1 and 5.

A unique feature of our approach is that the on-current can be readily scaled simply by adjusting the device width and NW density in order to meet the specific circuit needs. To demonstrate this capability, we have fabricated vertically stacked layers of FETs based on only single Ge/Si NWs. Low Ge/Si NW density growth substrates were used for the contact printing step in order to reduce the density of transferred NWs, while much narrower 1 μm width S/D electrodes were used to ensure a high yield of single-NW devices. An optical microscopy image of a five-layer structure is shown in Figure 3a, together with a schematic of addressable single-NW device structure. The low-resolution image (Figure 3a, left) shows the NW FETs in successive layers, where the FET arrays in each layer are offset in x and y for clarity. In addition, high-resolution images (Figure 3a, middle) demonstrate that the desired single-NW top-gated FET devices are formed in the five-layer structure. The electrical properties of representative devices from layers 1 and 5 are shown in Figure 3b,c. Significantly, we observe good reproducibility in the FET properties from lower (layer 1) and upper (layer 5) FETs even for these single-NW devices. The Ge/Si FETs deliver on currents, I_{ON}, of $\sim$10 μA at $V_{ds} = 1$ V with g_m of 7 μS. As previously reported,[8] scaled Ge/Si NW FETs afford diameter-normalized I_{ON} and g_m values of 2.1 mA/μm and 3.3 mS/μm, respectively, both of which are better than state-of-the-art planar Si technology. Hence, coupling this new 3D methodology with Ge/Si NW building blocks and advanced lithography (to produce small channels) could lead to ultrahigh-performance 3D electronics not accessible by scaled CMOS.

Last, we have explored the assembly and fabrication of multifunctional 3D NW electronics on flexible substrates utilizing our methodology. As shown schematically in Figure

Figure 4. Three-dimensional multifunctional circuits on plastics. (a) Schematics and circuit diagrams of inverter (top) and floating gate memory (bottom) elements. (b) Optical image of inverters (layer 1) and floating gate memory (layer 2) on Kapton. (c) DC inverter characteristics. Inset shows functional devices on flexible Kapton substrate. (d) AC inverter characteristics. Gain is larger than unity (V_{in}, red; V_{out}, black) at 50 MHz and V_{DD} of 4 V. (e) Hysteresis in current−voltage characteristics of a memory layer element. (f) Switching characteristics of memory at $V_{CG} = 5$ V with −15 and +15 V pulses (pulsing time, 1 ms).

4a, our designed 3D structure consists of a lower layer of PMOS inverters[5,6] and an upper layer of floating gate memory[30] elements. The inverter-memory structures were assembled on plastic substrates, which were chosen to illustrate further the versatility of our approach, using Ge/Si NWs as the active semiconductor material.[31] An optical image of a typical 3D structure (Figure 4b) shows clearly the lower inverter logic layer and offset in the *x* upper memory layer. Each inverter logic gate consists of a load and a switching FET, and the memory devices consist of an FET with a floating gate separated from the NW channel by a thin tunnel oxide and from the control gate by a thicker oxide.[31]

The electrical characteristics of the multifunctional device structure have been characterized in several ways. First, output (V_{out}) versus input (V_{in}) behavior (Figure 4c) shows well-defined inversion with quasi-DC gain of 3.5. Second, frequency-dependent measurements[24] (Figure 4d) demonstrate that the gain is greater than unity and phase inversion is achieved when the devices are driven by up to a 50 MHz sine wave supply of 4 V. This is the highest reported operation frequency for a circuit made of any channel material on flexible substrates, outperforming amorphous Si and organic electronics by over 2 orders of magnitude.[32,33] The NW inverter structure can be further improved in the future to obtain higher frequencies by using shorter channel lengths and incorporating thinner gate dielectrics. Third, current vs voltage sweeps recorded on the memory elements (Figure 4e) exhibit large and reproducible hysteresis loops consisting of storage and removal of charge from a floating gate element. Fourth, to further elucidate the properties of the NW memory devices, we carried out writing and erasing operations by applying short, 1 ms pulses of ±15 V to the control gate. As shown in Figure 4f, these pulses result in well-defined and nonvolatile ON and OFF states transitions, while the control gate is maintained at $V_{CG} = 5$ V during the reading (Figure 4f). Further device optimization can be explored to lower the operating voltage of the NW memory devices by scaling the oxide layers and also incorporating oxide engineering.[30,34]

In conclusion, we have demonstrated a general approach for 3D multifunctional electronics based on the layer-by-layer assembly of NW building blocks. The overall approach involved a repeating sequence of (1) contact printing of NWs optimized for function and (2) PL device fabrication on substrates ranging from crystalline silicon to flexible plastics. Using germanium/silicon (Ge/Si) core/shell NWs, we have demonstrated ten vertically stacked layers of reproducible and high-performance NW FETs, which represents the highest number of functional device layers that have been vertically stacked with any single-crystalline channel material to date. We have also shown that it is straightforward to use our approach to control key FET properties by varying the density of NWs assembled during the printing step. Last, 3D multifunctional circuitry was demonstrated on plastic substrates by sequential assembly and fabrication of inverter logical gates and floating gate memory elements layers. Notably, electrical characterization studies demonstrated signal inversion with larger than unity gain for frequencies up to at least 50 MHz in the inverters and stable and rewritable on/off states in the memory devices. The ability to assemble reproducibly sequential layers of distinct types of NW-based devices coupled with the breadth of NW building blocks should enable the assembly of increasing complex multilayer and multifunctional 3D electronics in the future.

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(21) NWs were printed by sliding a growth substrate, which consists of a "lawn" of Ge/Si core/shell NWs (diameter, ~15 nm; length, ~30 μm), against a second device substrate (Si/SiO_2 or Kapton). The Ge/Si NWs are randomly oriented on the growth substrate, not epitaxial, and are well-aligned by sheer forces during the sliding process. The sliding process results in the direct and dry transfer of NWs from the growth substrate to the desired device substrate chip. Prior to transfer, the device substrate was patterned with a photoresist layer (~500 nm thickness, Shipley 1805). The patterned spacer serves as dual purpose: to prevent transfer of particles and low-quality NW material close to the surface of the growth chip, and to enable selective assembly of the NWs at defined locations. After transfer, the patterned photoresist is removed in acetone, leaving only patterned NWs, which are well-aligned along the sliding direction.
(22) The FET structures were defined by two photolithography (PL) steps. In the first PL step, the source/drain (S/D) electrodes were patterned and metallized with Ni (60 nm). A HfO_2 high-κ gate dielectric film (thickness, ~12 nm) was deposited by 100 cycles of ALD at 115 °C with each cycle consisting of 1 s water vapor pulse, 5 s N_2 purge, 3 s tetrakis(dimethylamino)hafnium [$Hf(N(CH_3)_2)_4$] pulse, and 5 s N_2 purge. In the second PL step, the top gates were patterned and metallised with Al (60 nm). For multilayer structures, a SiO_2 layer (~300 nm), which serves as a separation layer between active device layers, was deposited by plasma-enhanced CVD or e-beam evaporation. Each additional active NW layer was offset in *x* and *y* directions to facilitate imaging and electrical measurements.
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