Layout Impact of Resolution Enhancement Techniques: Impediment or Opportunity?

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ABSTRACT
This tutorial introduces the reader to the basic concepts of optical lithography, derives fundamental resolution limits, reviews the challenges facing future technology nodes, explains the principles of resolution enhancement techniques and their impact on chip layout, and discusses layout optimization considerations.

Categories & Subject Descriptors
A.1 Introductory and Survey

General Terms: Theory

Keywords: Lithography, resolution enhancement techniques, design for manufacturability, radically restricted designs.

1. INTRODUCTION
Optical lithography has long been a key enabler to the rapid pace of integration that fuels the microelectronics industry. The resolution demands of the IC industry have outpaced the introduction of more advanced lithography hardware solutions for many technology generations, making lithographic patterning increasingly difficult and requiring the use of increasingly complex resolution enhancement techniques (RET) to maintain adequate pattern fidelity. As optical lithography is being pushed even closer to its fundamental resolution limit, it is becoming increasingly difficult to implement RET without the benefit of RET-enabling layout restrictions. While this unprecedented need for communication between the design and wafer-processing communities has been a major factor in the sluggish introduction of RET, the inevitable need to address RET-enabled layouts for sub-90nm technology nodes, also provides an opportunity for broad implementation of design-for-manufacturability (DFM).

To put the discussion on RET and their impact on layout into proper context, this tutorial initially introduces the reader to some simplified concepts of optical lithography. After a review of the exposure tool options for the next two major sub-90nm technology nodes, the basic principles of RET are presented and their impact on physical design discussed. Finally, a simplified layout optimization methodology based on radical design restrictions (RDR) is introduced.

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2. FUNDAMENTALS OF OPTICAL LITHOGRAPHY
2.1 Coherent Resolution Limit

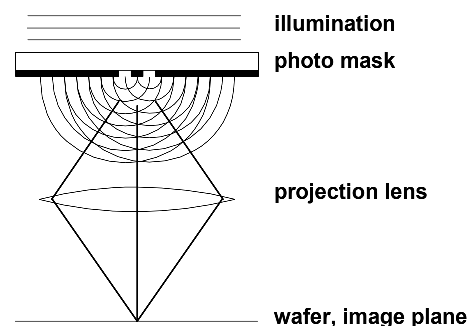

Figure 1, Schematic of an optical lithography system

For the purpose of this discussion, an optical lithography system can be represented by as drawn in Fig.1. A coherent plane of light, characterized by its wavelength, λ, illuminates a photomask, which can be seen as an opaque stencil of the desired pattern. At the dimensions in which modern IC lithography operates, the openings in the photomask can be approximated as individual light sources described by their centerline spacing or pitch, P. Since light penetrating neighboring mask openings is coherently related, constructive interference will cause diffraction nodes at any angle for which the geometric pathlength difference between the beams of light is equal to an integer multiple of the wavelength of light, or

$$\sin\theta = m\,\lambda / P \quad (1)$$

The maximum diffracted angle a projection lens can capture and use for image formation is defined as the maximum numerical aperture (NA) of the lens. Since one has to capture at least one diffracted order (the 0th order contains no spatial information), equation 1 can be rewritten as,

$$P_{min} = \lambda/NA \quad (2)$$

Or, in the more popular approximation assuming the minimum feature size, R, is simply P/2,

$$R_{min} = 0.5\,\lambda/NA \quad (3)$$

How close any given lithography process comes to this theoretical resolution limit is commonly expressed by the Rayleigh factor k_1,

$$R = k_1\,\lambda/NA \quad (4)$$

Showing that, in the coherent approximation to conventional optical lithography, resolution is proportional to λ, and inversely proportional to NA, offering two physical quantities for the reduction of printable half pitch (note: 'half pitch' is often used to bridge the gap between the 'pitch-centric' world of lithography and the 'dimension-centric' world of physical design, its accuracy is limited to equal line/space gratings found in some memory arrays, but it is commonly used for any pattern configuration).

In addition to defining the fundamental resolution limit of a patterning system, the Rayleigh factor is also used as a unit less measure of lithographic challenge, i.e.

$$k_1 = \text{Dimension}\ (NA/\lambda)\ (5)$$

expresses how difficult it is to resolve a certain dimension with a given lithography tool and is often used in lieu of feature size.

2.2 Depth of Focus

As illustrated in Fig.1, the image on the wafer, at the resolution limit, is formed by the interference of the 0th and 1st diffracted orders. Since the 0th diffracted order traverses the optical system perpendicular, i.e. along the center axis of the optical system, a pathlength difference is introduced relative to the higher diffracted orders. This pathlength difference changes as a function of the vertical image plane displacement, z

$$z\text{-}z\cos\theta\ \ (6)$$

The change in pathlength difference causes the phase relationship between the beams to vary. Rayleigh defines the depth of focus (DOF) as the vertical displacement for which the pathlength difference between the two beams is $\lambda/4$, leading to,

$$DOF = (\lambda/4)\ (1/(1-\cos\theta))\ \ (7)$$

…which after some trigonometric contortions and substitution of NA for $\sin\theta$ reduces to the commonly quoted DOF equation,

$$DOF = \lambda/(2NA^2)\ \ (8)$$

…highlighting the inverse square dependence of DOF and NA. This rapid loss of DOF is one of the fundamental limitations of high-NA lithography.

2.3 Complicating Details

2.3.1 Partial Coherence

Fig. 2 illustrates one refinement to the simplistic ray-tracing model of Fig.1. The illuminating light does not impact the photomask as a perfect plane wave, but rather spreads the illumination over and angle, $\sin\theta_c$ which is described relative to the NA in terms of the coherence factor σ,

$$\sigma = \sin\theta_i/\sin\theta_c\ \ (9)$$

This additional angle in the ray diagrams allows the theoretical resolution to be pushed beyond the limit identified in eq'n 4 to,

$$R = k_1\ \lambda/(NA(1+\sigma))\ (10)$$

…the outer limit at which a sliver of the diffracted cone of light is captured by the lens. While this has to be mentioned for completeness sake, the coherent approximation of eq'n 4 is most commonly used to qualitatively describe resolution.

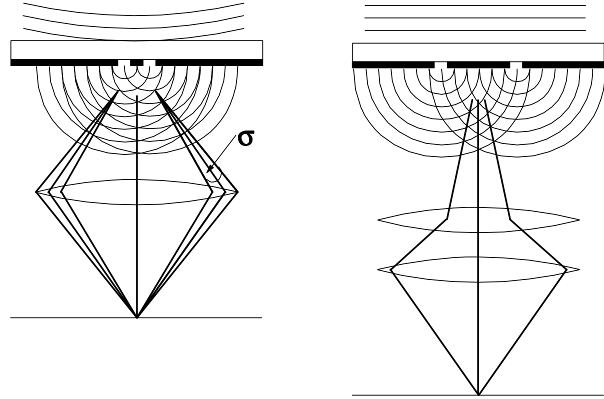

Figure 2, partially coherent imaging **Figure 3**, reduction stepper

2.3.2 Reduction steppers

A further complication to the convenient model of Fig.1 is the fact that lithography systems are no longer 1x projection systems. The mask patterns are typically magnified to 4 or 5x the dimension that is desired on the wafer. As illustrated in Fig.3, this mask magnification causes the diffracted angle on the mask side of the projection lens to be significantly smaller than in the 1x illustration of Fig.1. However, since the wafer side of the projection lens has to operate at 1x, the resolution and DOF eqn's 4 and 7 are unaffected by this detail. The main impact of the introduction of reduction steppers over a decade ago, has been what some refer to as 'the mask maker's vacation', i.e. mask manufacturing has benefited significantly from being able to manufacture magnified masks.

2.4 Wavelength

The direct correlation of lithographic resolution and illumination wavelength, eq'n 4, has traditionally been the main resolution reduction enabler.

Source	λ (nm)	λ ratio	Intended Resolution	Year of Introduction
G-line	436		Micron	
I-line	365	.83	half-micron	1984
KrF	248	.68	quarter-micron	1989
ArF	193	.78	100nm-node	2001
F_2	157	.81	65nm-node	?2004?
Ar_2	126	.80	45nm-node	*

Table 1, Lithography wavelengths and their applicability, * 126nm lithography is no longer considered a viable option.

Table 1 lists past, present, and future lithography wavelengths, their practical applicable range in terms of resolution, and their year of introduction. This short list makes a few important points:

- there are only a few distinct wavelengths that can be used for lithography
- we are quickly approaching the end of available light sources

- the ratio of wavelength reduction is, in most cases, not even enough to support one linear shrink of 70%.

Not captured in Table 1 is the immense financial- and time-investment in introducing not only an exposure tool at a new wavelength but a full patterning solution including resist and etch processes. As the drive to shorter wavelengths continues, severe physical barriers arise in: insufficient light intensity requiring super-sensitive chemically amplified resist systems, increased light absorption forcing more exotic optical materials and tighter cleanliness specifications on all optical components including the photomask, and ultimately, the need to operate in vacuum with reflective optics.

2.5 Numerical Aperture

Being defined as the sine of an angle, the mathematical limit of the NA is 1. Controlling critical parameters such as aberrations and focal plane flatness over large areas during lens manufacturing has made the introduction of NAs larger than 0.7 very difficult. Finally, the inverse quadratic relationship between DOF and NA (eq'n 8) make it challenging to manufacture with NAs much above 0.7 (for a NA of 0.7 the DOF is roughly 2 λ, requiring extreme control of wafer flatness, reduction of process induced topography, and very tight focus control in the exposure). Nonetheless, state of the art exposure tools use NAs of 0.75 in wafer production and 0.85 NA tools are soon to be introduced.

3. Manufacturing Trends

3.1 Past to Present

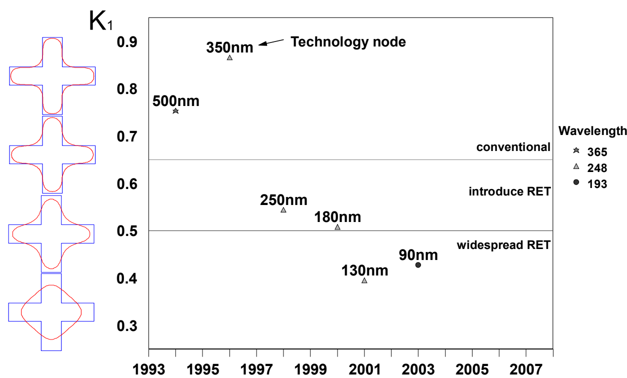

Figure 4, Erosion of the k_1 factor over time

Fig.4 illustrates how, in spite of continuous reduction in λ and increase in NA, lithography has been getting more difficult over time. For technology nodes ranging from 500nm through 90nm, the k_1 factor, as defined in eq'n 5, is plotted against the year of first manufacturing introduction. To the left of the graph is a series of simulations that illustrate how patterning fidelity decreases with k_1. Three distinct k_1 zones can be identified in Fig.4, the 500nm and 350nm technology nodes were imaged with a comfortable k_1>.65 using conventional lithography, the 250nm and 180nm technology nodes were approaching a k_1 of 0.5 and required more optimization effort and the introduction of RET such as attenuated phase shifted mask lithography (attPSM) and optical proximity correction (OPC), discussed in more detail below. The use of these RET was solidified with the 130nm and 90nm technology nodes which operate well below the k_1=0.5 resolution limit approximated in eq'n 3.

3.1.1 Attenuated Phase Shifted Mask Lithography

AttPSM lithography improves pattern fidelity by 'darkening' the edges of shapes through destructive interference of light using a mildly translucent photomask. Now commonly called 'embedded attenuated phase masks', these attPSM use mask substrates that allow a small amount of light (6-10%) to penetrate the normally opaque regions of the mask. Through careful material optimization, the background light penetrates the mask exactly 180° out-of-phase with the light penetrating the clear regions of the mask. As illustrated in Fig. 5, this phase shifted background light improves feature contrast at the edges of the printed image. Forcing the electric field vector of the background light to be negative by shifting it 180° relative to the foreground light causes a dark rim in the intensity profile. This 'crisping up' of the printed images helps to recover some patterning fidelity, but it does not fundamentally improve the resolution or DOF as outlined in eqn's 3 and 8. It is important to note that the self-consistency of the phase shifting effect in attPSM (i.e. no inter-shape phase interference), allows this technique to be applied to arbitrary layout configurations with no design restrictions.

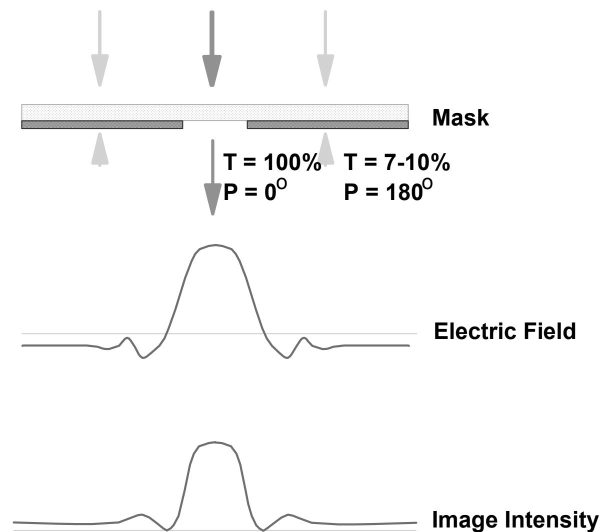

Figure 5, Principle of attenuated phase shifted mask (attPSM)

3.1.2 Optical Proximity Correction

A second example of RET that enabled volume manufacturing at vanishing patterning resolution, is OPC. Schematically outlined in Fig. 6, OPC begins by characterizing the patterning operation and all its inaccuracies from various sources such as the mask build, wafer exposure, etch, etc. In the now commonplace 'model-based OPC' this mathematical description of the process is used in iterative optimization routines to pre-distort the mask shapes to compensate for known, systematic, and modeled patterning inaccuracies. OPC improves the 'effective resolution' of a patterning process by overlapping the conditions with which different feature types can be imaged accurately, i.e. nested features typically image on-size and with the best image quality at a different exposure dose than isolated features. Biasing the mask patterns appropriately will allow both feature types to be imaged adequately in a single

exposure. However, OPC does not change the fundamental resolution limits of a lithography system and, though common practice, calling OPC a RET is a misnomer.

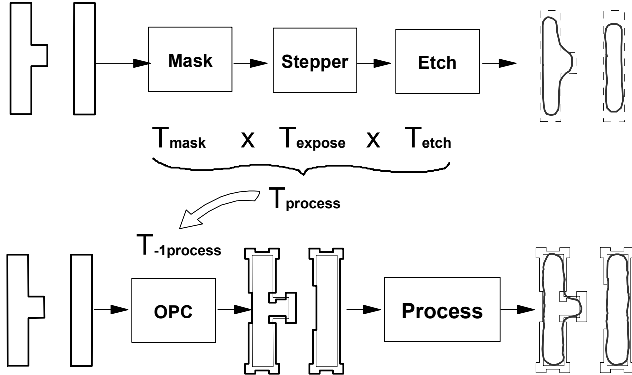

Figure 6, Optical proximity correction

3.2 Future Challenges

3.2.1 The Map That Guides Us

An excerpt of the international roadmap for semiconductors [1], shown in table 2, highlights the patterning challenges facing future technology nodes, often referred to as 'the sub-100nm nodes'.

The International Technology Roadmap For Semiconductors: 2002 Update

Year of Production	2001	2002	2003	2004	2005	2006	2007
MPU 1/2Pitch (nm)	150	130	107	90	80	70	65
MPU gate in resist (nm)	90	70	65	53	45	40	35
MPU gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
Gate CD control (3 sigma) (nm)	5.3	4.3	3.7	3	2.6	2.4	2
ASIC/LP 1/2 Pitch (nm)	150	130	107	90	80	70	65
ASIC gate in resist (nm)	130	107	90	75	65	53	45
ASIC/LP gate length after etch (nm)	90	80	65	53	45	37	32
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
CD control (3 sigma) (nm)	7.3	6.5	5.3	4.3	3.7	3	2.6

Table 2, Patterning challenges as spelled out in the ITRS

Patterning 160nm pitches with 2.6-3.7nm linewidth control would be exceedingly difficult in any kind of environment, but becomes daunting in light of the lithography tooling challenges discussed below.

3.2.2 Hardware Options

3.2.2.1 157nm Lithography

The upfront choice of manufacturing lithography for the 2005 technology node has long been 157nm λ, ultra-high NA lithography. Technical challenges, predominately related to unanticipated optical material challenges related to unique characteristics of CaF_2, coupled with significant economic challenges, have caused the 157nm lithography program to slip behind schedule [2]. The most optimistic estimate on having a fully integrated 157nm exposure process ready for manufacturing is mid-2005. Even with this somewhat unrealistic optimism, 157nm lithography will be late for all of the 65nm technology node (2005 manufacturing) process development and its soft ETA makes manufacturing strategies that rely on the availability of 157nm lithography very risky.

3.2.2.2 Extreme Ultra Violet Lithography

The prospect of lowering the illumination wavelength all the way to 13.5nm make Extreme Ultra Violet (EUV) lithography a very attractive proposal. The idea of illuminating a reflective reticle, manufactured by stacking 40-50 Mo/Si bilayers at atomic-scale accuracy, with light emitted by a laser produced plasma which is formed by zapping a Xenon medium with a high power laser in vacuum at very low power conversion efficiency, puts EUV in the technical challenge ballpark of the ICBM defense star-wars initiative. In spite of its mind-boggling technical complexity, EUV is currently moving out of the national laboratories into early commercialization [3]. However, it is unrealistic to assume that EUV will have any impact on either the 65nm or 45nm (2005 and 2007 manufacturing) nodes.

3.2.2.3 Immersion Lithography

With no hopes of having a shorter illumination wavelength available, immersion lithography uses a well-known microscopy trick to improve resolution. Since, as Fig. 3 illustrates, the diffraction limited resolution of the lithography system is defined on the wafer side of the projection lens and since the resolution and DOF, eqn's 4 and 8, should more correctly refer to the wavelength of the exposure light in the medium filling the gap between the exit pupil and the wafer, adding a higher index of refraction material in this gap, can, in theory, improve lithographic resolution. As challenging as the proposal of introducing wafers in a cleanroom environment into a watery or oily substance, scanning a precision lens in close proximity at very high speeds, and finally removing the wafers from the immersion bath for further processing sounds; it is being discussed as a possible manufacturing solution [4]. Since immersion lithography was only recently accepted as a potential concept, it is hard to even estimate possible availability dates.

3.2.3 The New k_1 Landscape

Based on the delay in 157nm lithography and the distinct lack of other alternatives, Fig. 7 shows the k_1 estimates for the upcoming technology nodes.

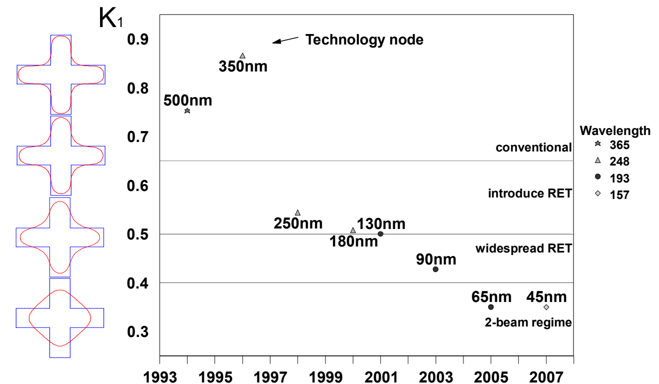

Figure 7, extending k_1 estimates into the future

Against the realization that even 130nm technology nodes are best manufactured with the k_1 relief provided by 193nm lithography, the 65nm and 45nm technology nodes are dangerously far below the k_1=0.5 resolution cutoff for conventional lithography. Fig. 7 introduces a new k_1 zone: the '2-beam imaging regime' in which highly optimized strong-RET facilitate volume manufacturing. How these strong-RET work, how they impact chip design, and what opportunities this impact enables, are the topics for the remainder of this tutorial.

4. The 2-Beam Imaging Regime

4.1 Principle of Strong-RET

If, as illustrated in Fig. 8, one were able to 'push back' one of light sources approximating the mask openings, by ½ λ, one would obtain a very different diffraction pattern.

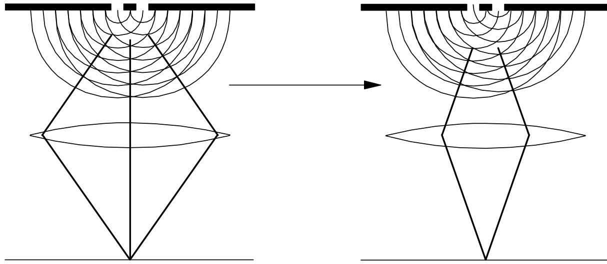

Figure 8, Advantages of 2-beam imaging

Since the first interference now occurs at an angle that adds ½ λ pathlength difference (rather than 1 λ for conventional lithography) the minimum set of diffracted orders required to form an image for a given pitch are much closer to the center of the imaging lens. For a given NA, the ultimate resolution, in terms of half-pitch, is now described by

$$R_{min} = 0.25\ \lambda/NA \quad (11)$$

…or a $k_1 = 0.25$. In addition, no constructive interference occurs at the 0° angle (the light sources are ½ λ out of phase), so the perpendicular beam is eliminated and with it the DOF limitations of eq'n 9. Therefore, 2-beam imaging provides 50% resolution improvement and significantly enhanced DOF.

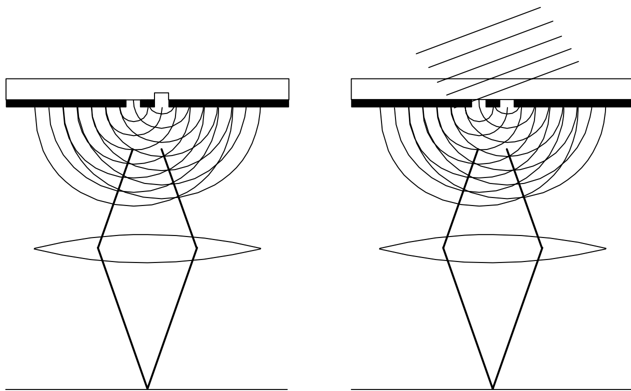

Figure 9, altPSM (left) and OAI (right) produce 2-beam imaging

Two means of achieving 2-beam imaging are shown in Fig. 9. To obtain the ½λ phase offset, alternating phase shifted mask lithography (altPSM) manipulates the mask topography to recess juxtaposed mask openings by

$$\text{Etch Depth} = 0.5\ \lambda / (n-1) \quad (12)$$

…where n is the refractive index of the mask substrate, typically around 1.4. Off-axis illumination (OAI) achieves the same effect by illuminating the mask at the appropriate angle

$$\sin \theta = 0.5\ \lambda / \text{Pitch} \quad (13)$$

More details on these two strong-RET, i.e. RET that aim to achieve 2-beam imaging and all its inherent benefits, are provided in the following.

4.2 AltPSM

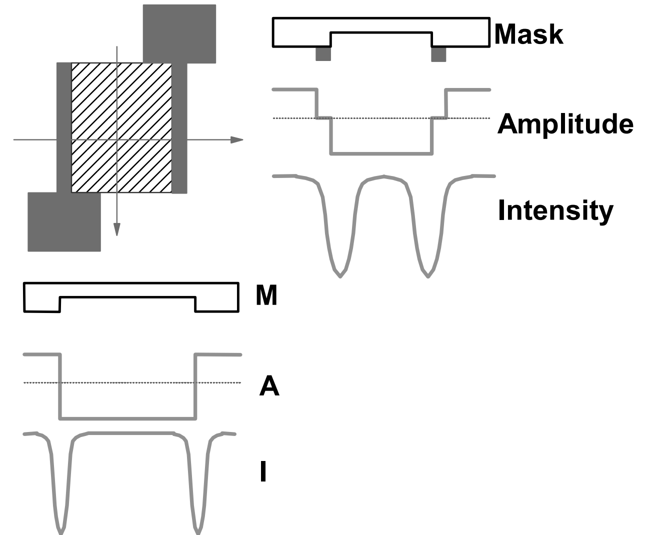

Figure 10, principle of altPSM

Two major challenges with altPSM are illustrated in Fig.10 on the example of a pair of transistor-like structures. In this case, the resolution enhancing phase shift is create across the narrow portion of the opaque mask structure. To facilitate this phase shift, juxtaposed mask regions have to exhibit the step height difference outlined in eq'n 12. As shown in the cross-sectional view to the right of the layout, this is achieved by recessing the appropriate mask region. This causes the electric field amplitude of the imaging light to reverse sign and yields high contrast shadows for the narrow images. Unfortunately, the recessed region of the mask can not always be forced to terminate on opaque features, causing the printing of unwanted residual images along the phase step as shown in the cross-section below the layout. Many creative ideas have been experimented with to eliminate the residual phase image, but ultimately the lithography community is conceding to the need for a double exposure process, as shown in Fig. 11. In this dark field alternating process the narrow layout segments are imaged by the phase shifted mask (left, layout and image) and a second exposure is used to remove residual images and fill-in the wider portions of the layout (right). The two images add in the photo resist to reasonably reconstruct the original pattern (bottom). While this double exposure process adds manufacturing cost, it does not change the design impact of altPSM over other approaches.

The fundamental need to identify regions on the mask that are to be recessed requires the addition of phase shapes to the chip layout. Lithography and mask manufacturability dictate certain dimensional constraints for the phase shapes which in turn prohibits the addition of legal phase shapes to arbitrary layout configurations, driving the need for altPSM-enabling layout restrictions.

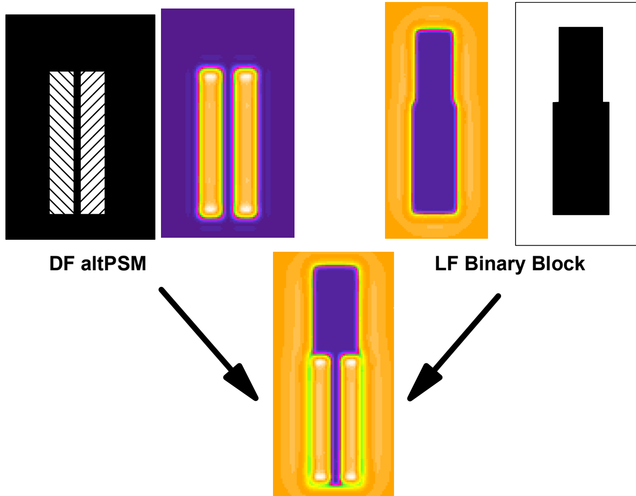

Figure 11, double exposure altPSM

Layout configurations that are otherwise design rule clean can lead to 'uncolorable' phase errors. A small hypothetical layout (original pattern in solid black, regions of opposite phase in diagonal-hatch) that violates no intra- or inter-shape design rules, yet causes an un-resolvable phase conflict, is shown at the top of Fig. 12. Multiple solutions to the phase conflict are also shown in Fig. 12, the optimum layout solution will depend on the specific layout objectives. Key challenges in the implementation of altPSM are the lack of reliable design rule checking to guarantee phase-compliant layouts [5] and the difficulty in converting abstract colorability feedback into required layout modifications.

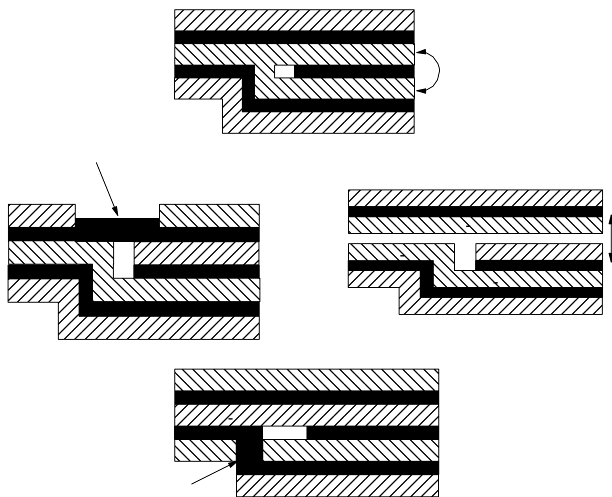

Figure 12, sample layout conflict (top) and possible solutions

4.3 OAI, attPSM, and SRAF

One problem associated with OAI is that the image is formed by interference between a beam of light that is transmitted perpendicular through the mask (0th –order) and a beam of light that is diffracted by the mask pattern (1st –order). While the illumination angle is chosen to perfectly balance the pathlength of these two beams, their light intensities are not balanced and exposure latitude (i.e. the insensitivity to dose variations) is reduced. AttPSM with the correct transmission value can be used to rebalance the intensities of the 0th and 1st diffracted orders and are used in this strong-RET to restore exposure latitude.

The other problem with OAI is that the illumination angle is optimized for a given mask feature pitch (eq'n 13), feature pitches that are significantly different than the pitch for which the illumination was optimized, will see much less resolution enhancement.

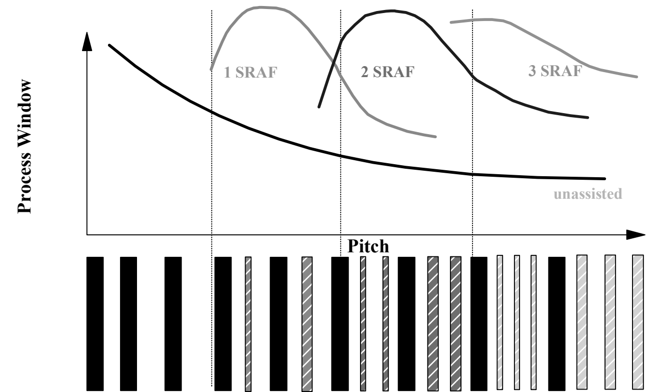

Figure 13, Sub-resolution assist features

To overcome the limitation of pitch-specific resolution enhancement, sub-resolution assist features (SRAF) are added to the layout [6]. These SRAF are dummy features that are drawn into the layout at a dimension where they optically mimic the diffraction angle of the pitch for which the illumination was chosen, but they are below the dimensional resolution of the lithography system so as to not leave an image in the photoresist. Fig 13 shows the gradual decrease in lithographic process window (i.e. the measure of how well pattern fidelity can be controlled over a range of exposure dose and defocus) as a function of increasing pitch ('unassisted' curve). The other curves in Fig. 13 show the discontinuous benefit afforded by one, two, or more SRAF.

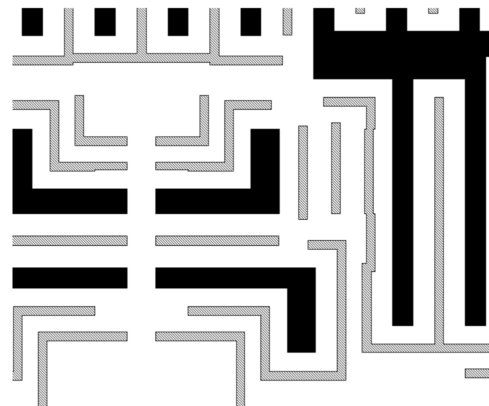

Figure 14, sraf-enhanced layout showing local sraf conflicts

While OAI and attPSM by themselves impose no layout restrictions, the need to add SRAF to the layout increasingly drives the need for SRAF-enabling design rules. The layout shown in Fig.14 presented an acceptable SRAF solution for the 130nm technology node [7], however, the hole in the SRAF coverage just right of center in the layout and the general inability to reconstruct an orderly diffraction grating, will cause significant loss of resolution enhancement for more aggressive applications like the 65nm technology node. In

one-dimension, the most commonly accepted layout restriction for SRAF is the 'forbidden pitch', i.e. pitches that fall in the transition regions between adequate SRAF coverage and cause the process window 'dips' shown in Fig. 13. Several variations on the OAI-attPSM-SRAF theme have recently been publicized. Double dipole lithography (DDL) [8] removes some of the 2-d SRAF challenges and allows for more aggressive illumination optimization by decomposing the layout into an entirely horizontal mask and its vertical counterpart. These two complementary masks are then superimposed in two separate exposures to reconstruct the original layout. Chromeless phase lithography (CPL) [9] uses mask topography manipulation, similar to altPSM to create what amounts to an extremely transparent attPSM to replace the embedded attenuated PSM. Ultimately, both DDL and CPL derive their resolution enhancement from OAI and require the same layout considerations that arise from adding SRAF to a variable-pitch layout.

4.4 RET are Key, Layout Restrictions are Inevitable

The intent of the preceding discussion was to convince the reader that the microelectronics industry has no option but to adopt strong, highly optimized RET as the only viable lithography solution for all future optical technology nodes. Further, it is important to realize that there are no 'miracle RET cures' that avoid layout restrictions. RET-enabling design constraints are the result of tradeoffs between lithographic process window, mask manufacturability, and layout impact. The extremely tight tolerances called for by the 65nm and 45nm nodes leave very little room for lithography tradeoffs.

If strong-RET are carefully optimized they will accurately approximate 2-beam imaging which will provide adequate resolution to pattern the tight pitches of sub-100nm nodes and will afford sufficient process window to meet the tight linewidth control targets spelled out in Table 1. However, chip designs for future technology nodes have to take into account the extremely limited two-dimensional information that can be transferred with a single diffracted order of light.

5. Design for Manufacturability

5.1 RET-embedded Design Flow

RET-enabling layout constraints, while unavoidable, cannot be described or enforced through conventional design rules without being unduly conservative [10]. 2-d SRAF layout violations are most commonly caused by proximity environments that are shared by multiple non-projecting feature edges at distances that cause un-manufacturable layout configurations. The most complicated altPSM layout violations involve odd cycles of phase transitions that can stretch over many adjoining features. Since a major goal in previous attempts to implement strong-RET such as altPSM was to minimize the impact on layout density and design complexity, design flows that embed the actual RET tool, as shown in Fig. 15, were developed. In the RET-embedded methodology, layouts are optimized directly against conflicts highlighted by the RET tool.

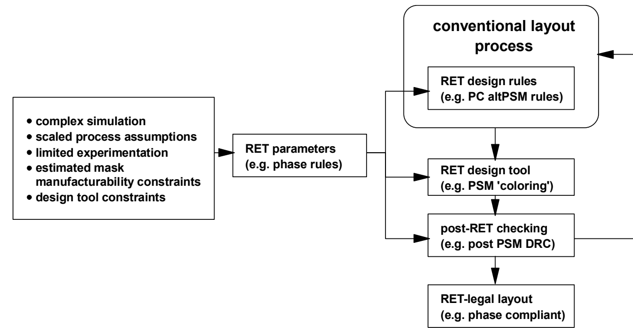

Figure 15, RET-embedded layout methodology

Several shortcomings of this RET-embedded approach can be identified:

- committing to a set of RET-parameters, in form of design rules or through iterative legalization using the RET design tool, long before mask and wafer processes are established (designs typically start 2-2.5yrs prior to manufacturing ramp-up), bears the risk of optimizing to a changing specification.
- the process-specific nature of the RET-specific optimization does not offer any insight into layout compatibility with future lithography solutions and inherently limits the layout to a single technology node.
- while significant layout effort is required to make designs RET-compliant (feed-back from the RET tools is much more abstract than from conventional DRC tools), general manufacturability [11] is not directly addressed.

5.2 Radically Restricted Rules

5.2.1 The Design for Manufacturability Mantra

To avoid the above-mentioned shortcomings and risks, design-rules, -tools, and -methodologies aimed at optimizing layouts for all future technology generations should:

- **Generically enable lithographic resolution enhancement techniques**

a layout that is optimized for many or all strong-RET avoids the problems associated with early commitment to a specific high-risk lithography process

- **improve manufacturability at extremely aggressive patterning resolution**

a layout that does not rely on tight control of 2-d detail will function even within the limitations of two-beam imaging lithography

- **ensure migrateablility of designs into future technology nodes**

the resource and time investment in a new layout make it necessary to use a given chip design for multiple technology generations with minimal redesign effort

- **allow for density- and performance-competitive chip designs**

constraints that optimize lithography but erase any benefit of moving to the next technology node do not make sense

- **address a broad spectrum of customer objectives with a single design and process solution**

to leverage the cost of mask and wafer manufacturing, different customer's needs have to be addressed with a common process solution.

These layout objectives can be met by changing from a 'minimum perturbation' approach to an approach based on 'radical design restrictions' (RDR) [12]. By clearly communicating fundamental aspects of the patterning process (e.g. resolution is driven by feature pitch) and fundamental goals of the chip design (contacted device pitch is the main driver of chip density in the front end of the layout), compromised rules can be derived that fundamentally improve manufacturability.

5.2.2 Feasibility Study

One example of RDR is investigated here. Rather than specifying forbidden pitches and ruling-out specific complex 2-d constructs, the designs are restricted to allow critical dimension features only in one orientation at integer multiples of the contacted device pitch. Fig.16 illustrates how a fundamental redesign, involving re-routing the power supplies, can achieve equivalent, even better, layout density (right) compared to the much less manufacturable, unconstrained layout. The original layout (left) poses many challenges (tight corners, 2-d environments, multiple pitches…). Addressing these issues at the layout level, i.e. by manipulating the CAD polygons, causes significant density impact (center). But a more rigorous redesign achieves all DFM objectives at high layout density (right).

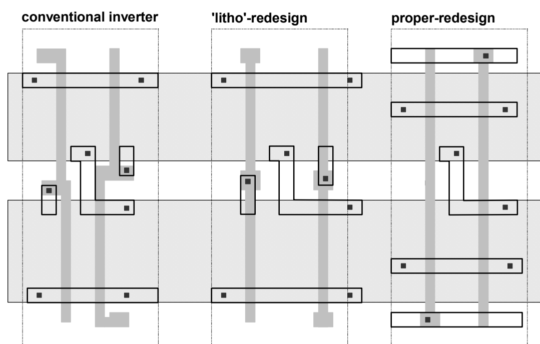

Figure 16, Layout optimization has to be done at design level (right) not at the layout level (center)

Generic RET-compliance is important for migrateability of the design as well as to mitigate lithography risk and is illustrated in Fig.17 on a high-performance, high-density latch design.

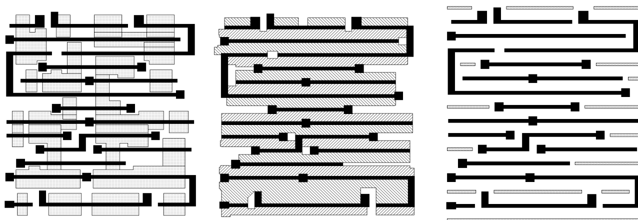

Figure 17, Latch cell designed with RDR (left) is altPSM optimized (center) as well as OAI-attPSM-SRAF optimized (right)

The radically restricted layout is inherently optimized for all strong-RET, greatly simplifying the logistics involved in RET-legalization. While not illustrated here, these same principles apply equally to dense memory arrays such as sram.

5.2.3 Challenges

While the basic DFM concept is almost intuitive and provides many benefits that could turn out to be of strategic importance to future technology nodes, much more work needs to be done in solving:

- multi-level optimization tradeoffs, e.g. avoiding wrong way poly-conductor shapes moves more local interconnect to the first metal level and may increase its complexity
- multi-parameter layout optimization, balancing the needs of RET-enabled lithography, random defect yield, layout density, and chip reliability is not trivial. Even if each category of concern is reduced to first principle 'rules of thumb' many oppose each other, e.g. lithography would like to keep the diffusion level largely rectangular with no small jogs near critical gates, electro-migration concerns dictate the addition of multiple redundant contacts that often require extensions and outcroppings on the diffusion shapes.

In addition to the technical challenges, there is the business challenge of 'selling' the DFM mantra to fabless design shops that often judge foundries by the aggressiveness of their design rules.

6. Conclusion

Future technology nodes are critically dependent on flawless implementation of strong-RET.

All strong-RET require layout restrictions, prohibiting the reuse of existing layouts in these technology nodes.

The need to generate RET-compliant designs offers the opportunity to fundamentally improve chip layouts by adopting the DFM mantra and implementing radical design restrictions.

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