Layout of Decoupling Capacitors in IP Blocks for 90-nm CMOS

Xiongfei Meng, *Student Member, IEEE*, Resve Saleh, *Fellow, IEEE*, and Karim Arabi, *Member, IEEE*

***Abstract*—On-chip decoupling capacitors (decaps) in the form of MOS transistors are widely used to reduce power supply noise. This paper provides guidelines for standard cell layouts of decaps for use within Intellectual Property (IP) blocks in application-specific integrated circuit (ASIC) designs. At 90-nm CMOS technology and below, a tradeoff exists between high-frequency effects and electrostatic discharge (ESD) reliability when designing the layout of such decaps. In this paper, the high-frequency effects are modeled using simple equations. A metric is developed to determine the optimal number of fingers based on the frequency response. Then, a cross-coupled design is described that has been recently introduced by cell library developers to handle ESD problems. Unfortunately, it suffers from poor response times due the large resistance inherent in its design. Improved cross-coupled designs are presented that properly balance issues of frequency response with ESD performance, while greatly reducing thin-oxide gate leakage.**

***Index Terms*—Electrostatic discharges, integrated circuit layout, leakage currents, MOS capacitors.**

I. Introduction

With increasing clock frequency and decreasing supply voltage as CMOS technology scales, maintaining the quality of the power supply has become a primary issue. Voltage variations in the power supply arise due to IR drop and Ldi/dt [1]. The IR drop has been increasing over time due to increased resistances in the power grid as the metal widths continue to shrink with each successive technology generation. The inductive Ldi/dt effects are also increasing due to the high current demands of application-specific integrated circuit (ASIC) designs in 90-nm CMOS technology. However, the pin and package inductance overwhelms the inductance of the on-chip power distribution network, and therefore, the on-chip inductance is usually neglected [1].

There are a variety of different methods that can be used to manage voltage drops. Among them, the most popular is to use on-chip decoupling capacitors (decaps) to maintain the power supply within a certain percentage (e.g., 10%) of the nominal supply voltage [2], [3]. Decaps are typically placed in regions between areas of high current demands and the power pads and input/output (I/O) pins [4]–[6]. This paper addresses standard-cell decap layout [7], [8], [15] at the 90-nm technology node and below.

A number of relatively new issues for standard cell decaps must be addressed that impact the design and layout of these cells at scaled technology nodes. We address two important problems of decap frequency response and electrostatic discharge (ESD) protection [11]. Since decaps are required to perform at increasingly higher operating frequencies, we first investigate the frequency response [6], [9], [10] and propose improvements to optimize decap layouts. Next, we investigate the problems of reduced oxide thickness of a transistor, namely, ESD [11] and thin-oxide gate leakage [3], [4], in the context of decap design. A potential ESD event across a thin gate oxide increases the likelihood that a chip will be permanently damaged due to a short circuit in the decap itself. Higher gate leakage increases the total static power consumption of the chip.

A cross-coupled standard-cell design was proposed [12] to address the issue of ESD performance. The design provides sufficient ESD protection, but does not offer any savings in gate leakage and it may compromise the frequency response. This paper suggests improved layouts of the cross-coupled design that properly tradeoff frequency response and ESD performance, while greatly reducing gate leakage current.

The rest of this paper is organized as follows. In Section II, layout design based on the frequency response of decaps is addressed. The two new design issues, ESD reliability and gate tunneling leakage, are briefly discussed in Section III, followed by the cross-coupled design and its layout modifications. Conclusions are provided in Section IV.

II. High-Frequency Response of Decoupling Capacitors

Standard cell layouts of an Intellectual Property (IP) block consist of rows of fixed-height cells in the ASIC design flow. After cell placement is completed, there are a number of empty cells that can be filled with decaps of various sizes depending on the space available. Previous work has addressed the automatic placement and sizing of decap cells [8]. Our focus is on optimal layout of each decap filler cell. Typically, these standard cells have both nMOS and pMOS devices as shown in Fig. 1(a), with a corresponding layout in Fig. 1(b). Thin-oxide MOS devices are generally used for standard-cell decap implementation.

As the frequency of operation increases, a fingering approach is required to implement the layout. That is, a single transistor is split into a number of parallel transistors with the same width, but smaller channel lengths. The overhead of this approach is additional spacing for source/drain contacts and an overall reduction in the low-frequency capacitance. However, the average capacitance of the decap over a given frequency range improves

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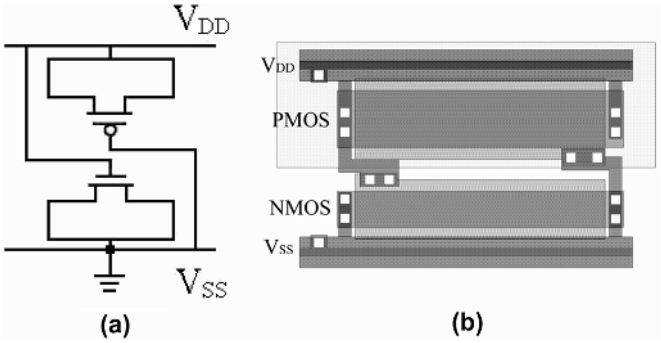

Fig. 1. (a) Standard cell decap can be implemented as an nMOS in parallel with a pMOS device. The corresponding layout is shown in (b).

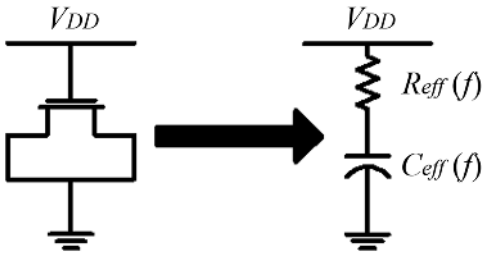

Fig. 2. Decap can be implemented as an nMOS device and modeled as a lumped-*RC* circuit with effective resistance and effective capacitance as functions of frequency f.

as we increase the number of fingers. Therefore, we address the problem of how many fingers to use, given a fixed area of a filler cell and fixed gate-oxide thickness, and develop a useful metric to capture the frequency response characteristics in order to choose the optimal number of fingers.

To derive the needed equations, we begin with an nMOS decoupling capacitance as shown in Fig. 2. Non-idealities associated with MOS devices are modeled as a lumped-resistance–capacitance (*RC*) circuit [10] where both the effective resistance R_{eff}, and effective capacitance C_{eff}, are functions of frequency f, as shown in Fig. 2.

The dc capacitance $C_{\text{eff},0}$ and resistance $R_{\text{eff},0}$ are given by [7], [10], [13]

$$C_{\text{eff},0} = C_{\text{OX}}WL + 2C_{\text{OL}}W \tag{1a}$$

$$R_{\text{eff},0} = \frac{1}{12}\frac{L}{\mu C_{\text{OX}}W(V_{\text{GS}} - V_T)} \tag{1b}$$

where C_{OX} is the oxide capacitance per unit area, C_{OL} is the overlap and fringing capacitances per unit width of the device, μ is the mobility, V_{GS} is the voltage across the oxide, V_T is the threshold voltage, and W and L are the width and length of the transistor, respectively.

Assuming that a given filler cell has a horizontal dimension X and vertical dimension Y, the channel length of each device in a fingered layout is

$$L_n = [X - (n-1)x_{\text{contact}}]/n \tag{2}$$

where n is the number of fingers and x_{contact} is the distance between fingers required by contact spacing rules. Modified expressions for $C_{\text{eff},0}$ *and* $R_{\text{eff},0}$ can be derived as a function of the number of fingers. Thus, the effective capacitance at dc is given by

$$C_{\text{eff},0(n)} = n \times (C_{\text{OX}}YL_n + 2 \cdot C_{\text{OL}}Y). \tag{3}$$

For capacitance, each additional finger adds extra overlap and fringing capacitances but loses area due to the contact spacing. Therefore, the capacitance actually decreases linearly as we increase the number of fingers. The corresponding equation for $R_{\text{eff},0}$ with n fingers in a parallel combination is

$$R_{\text{eff},0(n)} = \frac{1}{12}\frac{L_n}{\mu C_{\text{OX}}W(V_{\text{GS}} - V_T)} \times \frac{1}{n} \approx \frac{R_{\text{eff},0}}{n^2}. \tag{4}$$

In previous work [10], the resistance was used to select the channel length and there were no area constraints involved. However, since the resistance drops off as n^2, it is not as important in the selection of a suitable n. In fact, the goal of an optimal layout should be to provide the highest capacitance value in the given area over a desired operating frequency, 0 to f_{o}, while delivering a low resistance. A simple metric is needed to evaluate layouts with differing number of fingers. The logical choice for a metric is to use the average capacitance over this frequency response up to f_o, as follows:

$$C_{\text{avg}(n)} = \frac{C_{\text{eff},0(n)} + C_{\text{eff}(n)}(f_o)}{2} \tag{5}$$

where $C_{\text{eff},0(n)}$ is obtained from (3) and $C_{\text{eff}(n)}(f_o)$ is the effective capacitance with n fingers at frequency f_o. A weighted average is also feasible, but we find that the simple average works well in practice.

The main issue with the metric is that $C_{\text{eff}(n)}(f_o)$ is difficult to compute without the aid of HSPICE or an equivalent simulation tool. To facilitate the process, we developed simple frequency-dependent models for both C_{eff} and R_{eff}. We also wanted the characteristics of both functions to be accurate as technology scales. First, we performed a number of ac simulations in HSPICE for a 90-nm CMOS technology using *nonquasi-static* (NQS) models, which are essential when simulating decaps in the gigahertz frequency range of operation. Two parameters, ACNQSMOD and TRNQSMOD, were set to "1" in BSIM4 [13]. The circuit in Fig. 3 was used to extract the effective resistance and capacitance from HSPICE results as follows:

$$R_{\text{eff}}(f) = \frac{\text{Re}(I_{\text{RC}})}{\text{Mag}^2(I_{\text{RC}})} \quad C_{\text{eff}}(f) = \frac{\text{Mag}^2(I_{\text{RC}})}{2\pi f \text{Im}(I_{\text{RC}})}$$

where $\text{Re}(I_{\text{RC}}), \text{Im}(I_{\text{RC}})$, and $\text{Mag}(I_{\text{RC}})$ are the real, imaginary, and magnitude components of I_{RC}, respectively.

Both nMOS and pMOS decaps were simulated with W × L sizes as follows: 15 μm × 5 μm, 10 μm × 10 μm,

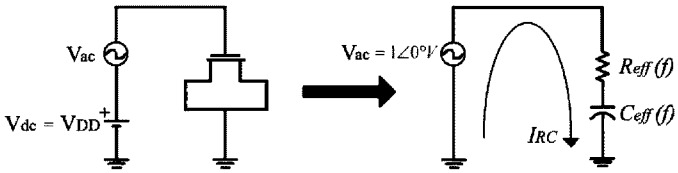

Fig. 3. Circuit setup to extract the effective resistance and the effective capacitance values from an ac analysis.

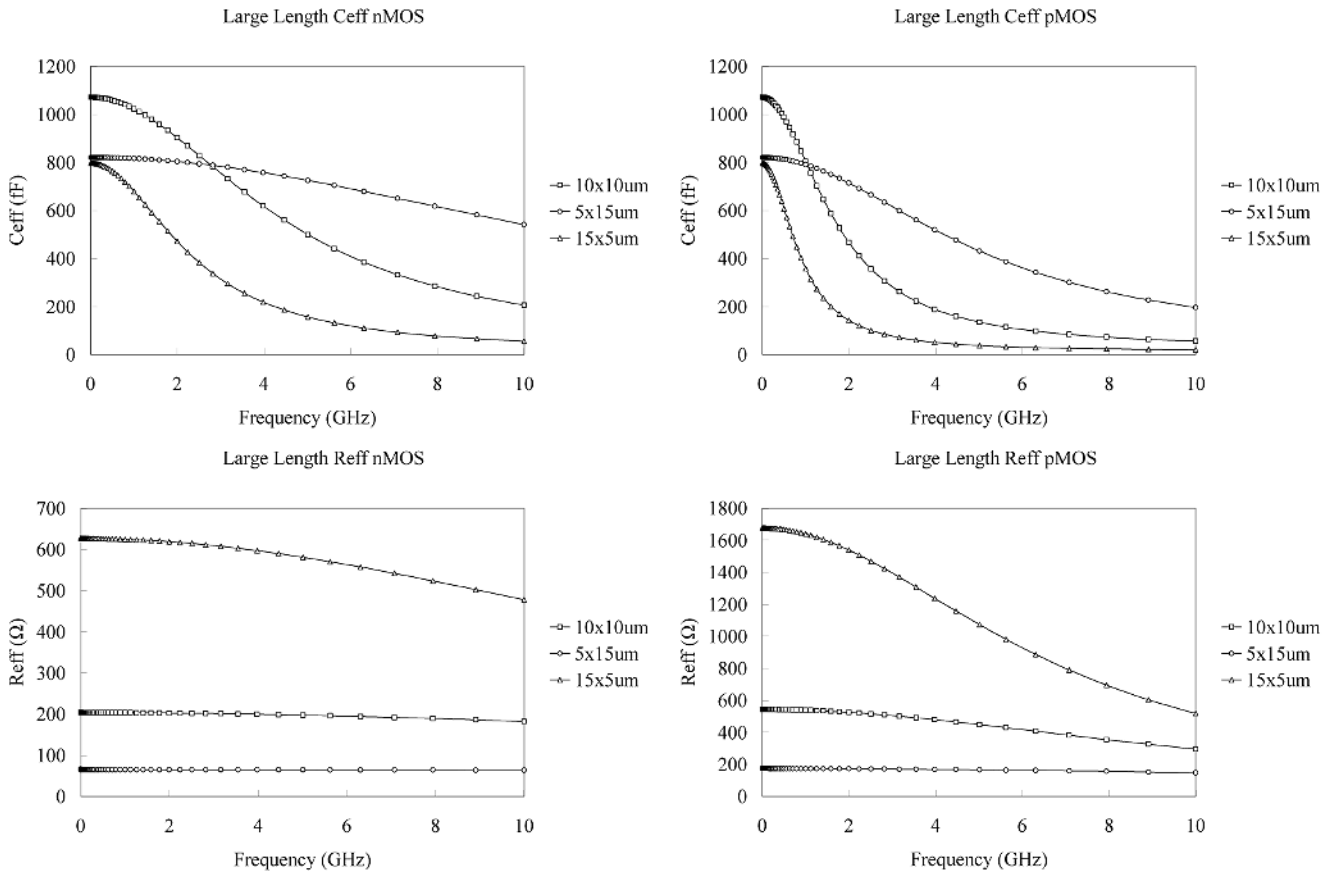

Fig. 4. Circuit setup to extract the effective resistance and the effective capacitance values from an ac analysis.

and 5 μm × 15 μm. The simulation frequency ranged from 0 to 10 GHz. Typical ASIC clock rates today are in the range of 500 MHz to 1 GHz, but it is important to study frequency response well beyond the clock frequency. Most of the spectral power density of digital signals lies within frequencies of up to $f_{\text{knee}} = 1/(2t_{\text{rise}})$, where t_{rise} is a signal's rise time (which can be on the order of 50 ps or less), and f_{knee} is the 3-dB cutoff frequency of the spectral power density [14]. We assume conservatively that $t_{\text{rise}} = 50$ ps, and carry out the analysis up to 10 GHz.

The results of the simulations are shown in Fig. 4. As f increases, there is a noticeable rolloff in the curves due to finite transit time effects. Devices with large L's have a more pronounced effect. In fact, the C_{eff} curve for 5 μm × 15 um quickly decays in value relative to 15 μm × 5 μm. A general observation on nMOS and pMOS decaps can also be made: nMOS is superior to pMOS in its high-frequency behavior since it has a larger C_{eff} and a smaller R_{eff} at high frequencies, assuming the area is fixed. Although standard cells employ both nMOS and pMOS devices for decaps, these results show that nMOS decaps would provide better frequency response characteristics.

Based on the frequency responses of C_{eff} and R_{eff}, we postulated functions for modeling purposes of the form

$$C_{\text{eff}}(f) = \frac{C_{\text{eff},0}}{1 + (f/f_T)^2\tau_1^2} \tag{6a}$$

$$R_{\text{eff}}(f) = \frac{R_{\text{eff},0}}{1 + (f/f_T)^2\tau_1^3} \tag{6b}$$

where $\tau_1 = 1/12$ [13] and $f_T = (\mu(V_{\text{GS}} - V_T))/(2\pi L^2)$. Shown in Fig. 5 are the results of curve-fitting using (6a) and (6b) against HSPICE for the nMOS device. The results are very close. A factor of 1/2 was applied to f_T in order to produce results shown in Fig. 5. That is, the equation for f_T must be adjusted by a fitting factor of 0.5 in order to obtain good results. Similar results were obtained for pMOS devices. This demonstrates that the first-order equations for $C_{\text{eff}}(f)$ and $R_{\text{eff}}(f)$ are reasonably accurate and, perhaps more importantly, that $C_{\text{eff}(n)}(f_{\text{o}})$ can be easily computed for the metric without running HSPICE.

We now have all the necessary information to determine the number of fingers based on the frequency response. From (6a), the effective capacitance in (5) at f_o with n fingers is

$$C_{\text{eff}(n)}(f_o) = \frac{C_{\text{eff},0(n)}}{1 + (f_o/f_{T(n)})^2\tau_1^2}$$

where

$$f_{T(n)} = \frac{\mu(V_{\text{GS}} - V_T)}{2\pi L_n^2}.$$

To demonstrate the efficacy of the metric, we apply it to the layout of a standard-cell decap in an available area of 2 μm × 9 μm. Using (5), Table I lists the $C_{\text{avg}(n)}$ metric values for the nMOS or pMOS devices for different frequency ranges. The optimal number of fingers corresponds to the largest entries in bold. For example, if the frequency range of interest is 0 to

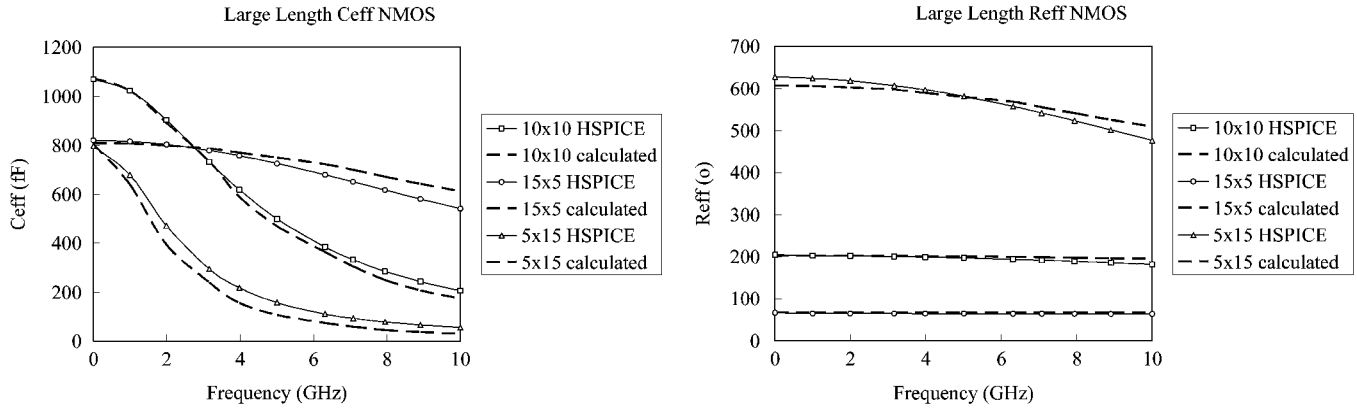

Fig. 5. Plots of C_{eff} and R_{eff} for three nMOS devices (HSPICE versus model).

TABLE I
OPTIMAL NUMBER OF FINGERS FOR DIFFERENT FREQUENCY RANGES

Freq range $0 - f_0$		C_{avg} Metric vs. Number of Fingers				
		n = 1	n = 2	n = 3	n = 4	n = 5
0 – 2GHz	N	180fF	**187fF**	182fF	177fF	171fF
	P	150fF	**183fF**	182fF	177fF	171fF
0 – 5GHz	N	150fF	**184fF**	182fF	177fF	171fF
	P	110fF	165fF	**178fF**	176fF	171fF
0 – 10GHz	N	120fF	173fF	**180fF**	176fF	171fF
	P	100fF	135fF	166fF	**172fF**	169fF

10 GHz, then 3 nMOS fingers and 4 pMOS fingers are optimal relative to our metric. Of course, if the range is 0 to 2 GHz, two fingers are sufficient for both N or P devices. Note that pMOS devices typically require one more finger than nMOS devices at higher frequencies of operation.

Table I was shown to illustrate the use of the metric in determining the optimal number of fingers. In practice, the design process would be as follows. First, the area of a filler cell (in particular, the X-dimension of the cell) and frequency range of operation are used as input parameters. Then, the capacitance value as a function of n is computed using (5). Finally, the value of n producing the highest capacitance is used to implement the layout.

The results in Table I can be validated by using (3) and (6a) to generate $C_{\text{eff}(n)}$ plots for both nMOS and pMOS devices, as shown in Fig. 6. The results in the plot were verified with HSPICE to ensure consistency. As an example, consider the cases with 1 finger and $f_o = 10$ GHz. For the nMOS case in Fig. 6 $C_{\text{avg}(1)n} = (C_{\text{eff},0} + C_{\text{eff}(1)}(f_o))/2 = (190\text{ fF} + 50\text{ fF})/2 = 120$ fF, whereas for pMOS, $C_{\text{avg}(1)\,p} = (C_{\text{eff},0} + C_{\text{eff}(1)}(f_o))/2 = (190\text{ fF} + 10\text{ fF})/2 = 100$ fF. These are the same values that are found in the last row of the table with $n = 1$. The rest of the table is produced in the same manner for different values of n and frequency range $0 - f_o$.

By inspection, the plots indicate that three fingers would be optimal for nMOS decaps and four fingers would be optimal for pMOS decaps, based on the flatness of the lines and the initial value of the capacitance. This conclusion is consistent with Table I. However, by using the metric, designers can quickly obtain the optimal number of fingers for a target operating frequency, without the need for such plots or SPICE simulations.

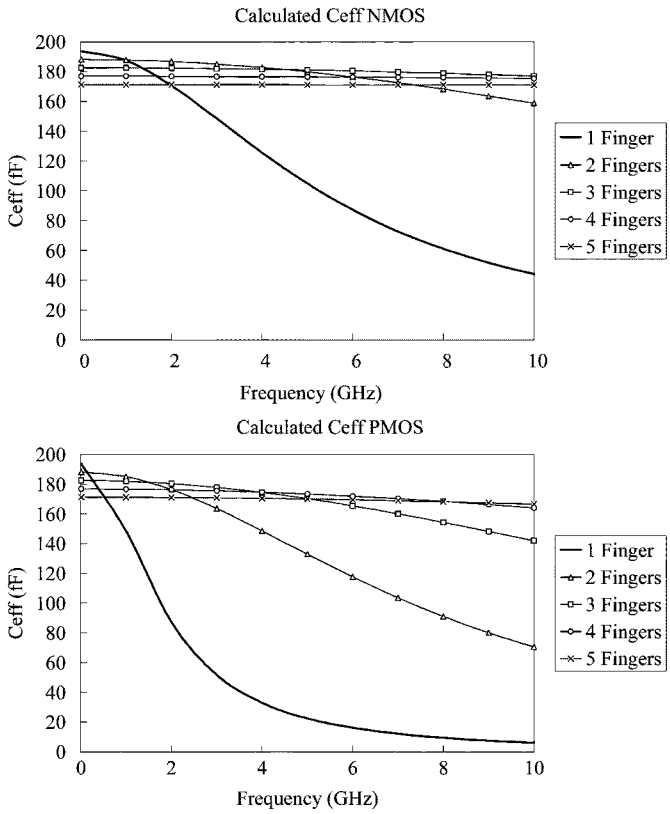

Fig. 6. Effective capacitance $C_{\text{eff}}(f)$ of nMOS and pMOS decaps in 90 nm for different numbers of fingers in a fixed area of $Y = 2\ \mu$m and $X = 9\ \mu$m.

Fig. 7 illustrates how standard cell layouts would be implemented using the previous results, assuming a 10-GHz operating range. These layouts would be automatically created by a decap filler cell generator. Two possible layouts are shown: (a) uses the N and P devices and (b) is nMOS only. Fig. 9(a) uses three fingers for the nMOS device and four fingers for the pMOS device. From an average capacitance perspective, the nMOS-only layout style of Fig. 9(b) is better, and this is also reflected in Table I. To implement this type of layout in a standard cell, the p-well region must be extended to cover the entire area, which is not typical of standard cell design. This approach can be used

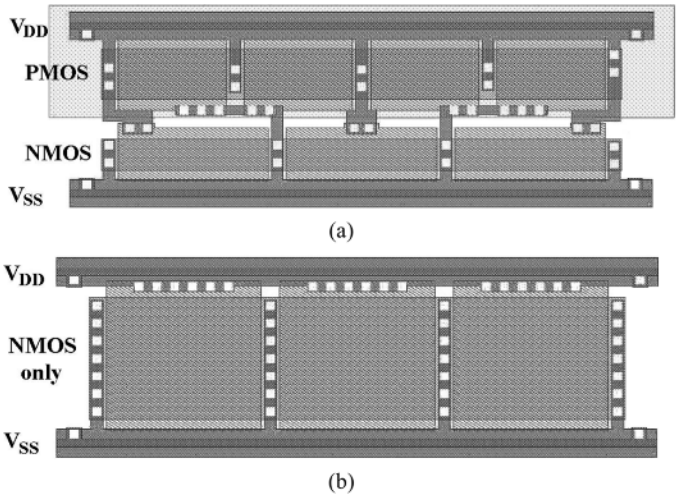

Fig. 7. Two sample layouts showing (a) N and P decap with four pMOS and three nMOS fingers and (b) nMOS-only with three fingers in a 90-nm technology.

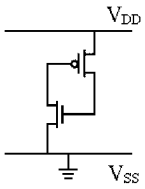

Fig. 8. Cross-coupled decap schematic [12].

as long as the design rules at the boundaries of adjacent standard cells are satisfied.

III. Cross-Coupled Decoupling Capacitor Designs

At the 90-nm technology node, there is the possibility of oxide breakdown during an ESD event. A simple ESD protection scheme for decaps is to insert a relatively large resistance in series to limit the maximum voltage seen at the gate of the decap [11]. A minimum $R_{\text{eff},0}$ is needed to ensure ESD reliability for decap cells. A cross-coupled decap design has been proposed by cell library developers [12] to address the issue of ESD reliability. Fig. 8 illustrates the new decap wherein the drain of the pMOS device is connected to the gate of the nMOS, and vice versa [12]. The cross-coupled design provides additional series resistance to the inherent decap resistance to increase $R_{\text{eff},0}$.

The frequency response characteristics of this new configuration can be evaluated to determine if the results obtained in the last section can be applied directly to the new circuit. We first compared a standard 3N-4P decap of Fig. 7(a) to a same-area cross-coupled decap using HSPICE ac analysis in Fig. 9.

The standard 3N-4P decap has a very low resistance (around 30 Ω), which makes it prone to ESD failure. The cross-coupled 3N-4P design has a much higher dc $R_{\text{eff},0}$ (around 3500 Ω) but a poorer frequency response for C_{eff}. Consequently, the tradeoff between ESD reliability and frequency response must be considered in the design process and decap layout. To improve the frequency response, additional fingers must be used. The target

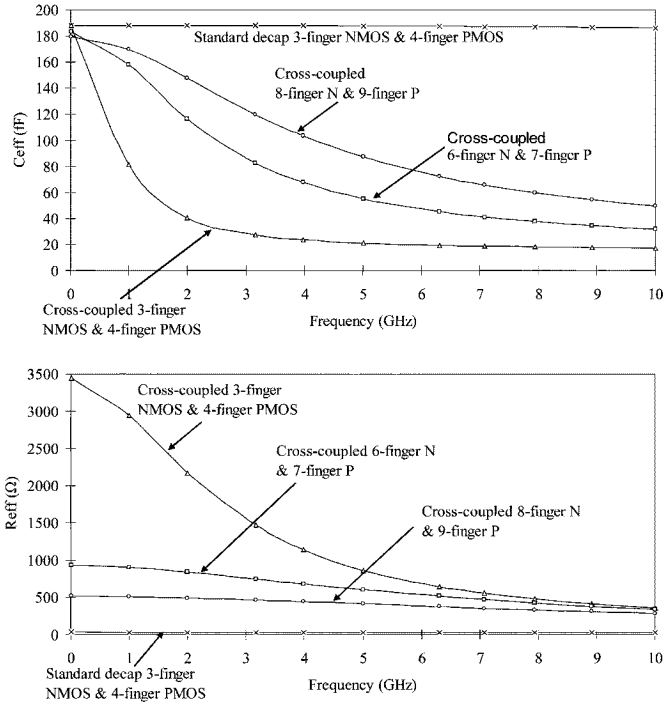

Fig. 9. $C_{\text{eff}}(f)$ and $R_{\text{eff}}(f)$ comparison of fixed-area standard decap and cross-coupled decap: same MOS device sizes but different poly connections.

resistance $R_{\text{eff},0\_\text{target}}$ for ESD protection in our case is a minimum of 500 Ω. We increased the number of fingers to reduce the resistance from 3500 Ω down to that required by ESD. According to (4), the scale factor on the 3N-4P design can be found as follows:

$$R_{\text{eff},0\_\text{target}} = \frac{3500}{n^2} = 500 \therefore n = \sqrt{3500/500} = 2.6.$$

Scaling the 3N-4P by approximately this amount, we produced a cross-coupled 8N-9P decap. Similarly, for an ESD target $R_{\text{eff},0\_\text{target}} = 1000\ \Omega$, we find that $n = 1.9$, so we chose 6N-7P. The plots for 6N-7P and 8N-9P fingers are also illustrated in Fig. 9. The results show that the 8N-9P cross-coupled version is the best configuration to address both frequency response and ESD protection.

From a layout perspective, the cross-coupled decaps can be realized by simply rerouting the poly connections of the standard decaps, while keeping the MOS devices the same. The layouts of two cases, 3N-4P and 8N-9P, are shown in Fig. 10.

We addressed one other issue of thin-oxide gate leakage current [16] of the decap, which contributes to the chip's total static power. Using HSPICE, the standard and cross-coupled decap circuits were found to have almost identical gate leakage. That is, since the cell area is fixed and only the poly terminal connections are swapped, the cross-coupled design provides no inherent savings in gate leakage as compared to the standard design. There exists a simple design approach to save gate leakage. Simulations using BSIM4 SPICE models [17] indicated that pMOS gate leakage is roughly 3 times smaller than nMOS gate leakage for same size transistors [18], [19].

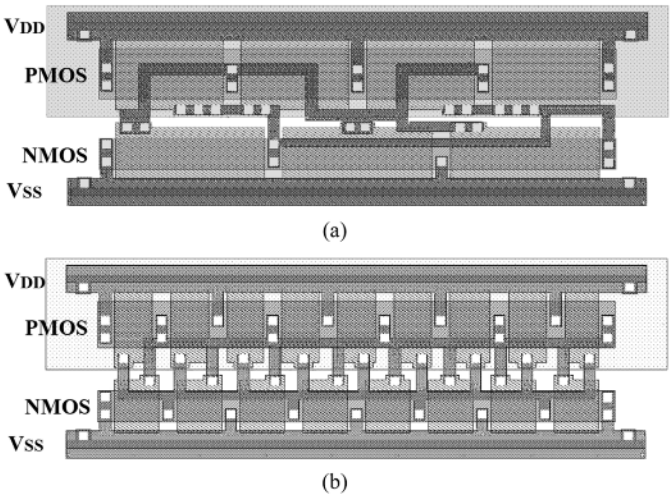

Fig. 10. Sample layouts of cross-coupled decap cells for (a) 3N-4P (b) 8N-9P.

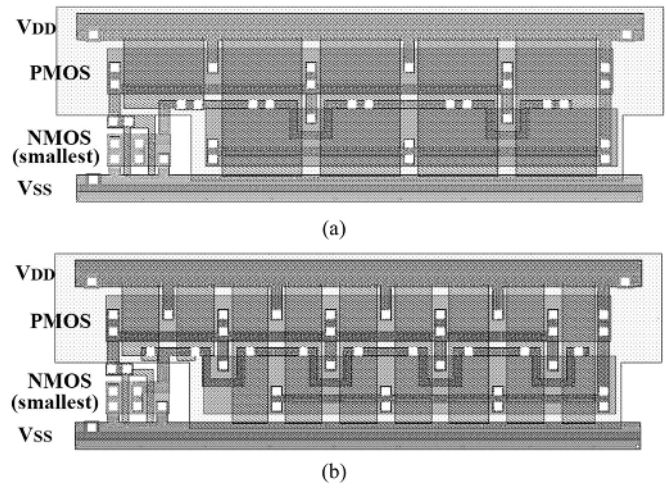

Fig. 11. Sample layouts of improved decap cells for (a) 1N-9P (b) 1N-16P.

Therefore, pMOS devices are preferred from a leakage perspective. Since pMOS devices have a poor frequency response, more fingers can be used to obtain the desired result. But this must be carried out in the context of the cross-coupled design to preserve ESD protection.

The basic idea to control leakage is to have the smallest possible nMOS device cross-coupled with the largest possible multi-fingered pMOS device. This way, the advantages of pMOS leakage and cross-coupling ESD protection are preserved. The layouts of two configurations are illustrated in Fig. 11. A small nMOS device is used in both cases. Note the n-well regions have been expanded in both layouts to accommodate the larger pMOS device. Fig. 11(a) uses 9 pMOS fingers while Fig. 11(b) has a total of 16 fingers. The same cell area as before (2 μm $\times$ 9 μm) was used for the two designs.

Table II summarizes the leakage values for the different cases. The standard and cross-coupled 3N-4P decaps have roughly the same leakage. It is somewhat reduced for the 8N-9P case since there is less area for leakage. However, for the two layouts with

TABLE II
COMPARISON OF THE NEW DESIGNS AND THEIR GATE LEAKAGE CURRENT

Decap cell layout		Description	Gate Leakage (nA)
Std. 3N+4P		Standard decap with 3 fingers for NMOS and 4 fingers for PMOS	262.4
Cross-coupled 3N+4P		Cross coupled with 3 fingers for NMOS and 4 fingers for PMOS	260.8
Cross-coupled 8N+9P		Cross coupled with 8 fingers for NMOS and 9 fingers for PMOS	206.8
Modified	9P	Cross coupled with smallest NMOS and 9 fingers for PMOS	**119.1**
	16P	Cross coupled with smallest NMOS and 16 fingers for PMOS	**99.7**

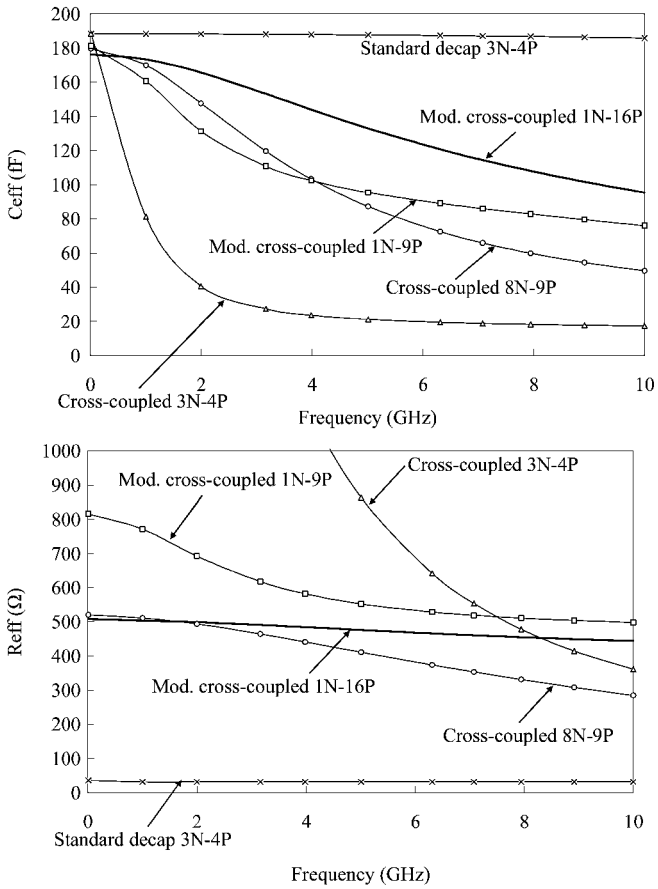

Fig. 12. Frequency response of various cross-coupled designs.

the small nMOS devices, the leakage is cut in half. In fact, the case with 1N-16P, the leakage is 62% less than the standard decap 3N-4P.

The $R_{\text{eff},0\_\text{target}}$ of the cross-coupled design must be set based on ESD considerations, but that also controls the maximum number of fingers permitted $n_{\max}$. Since the nMOS device is fixed while the pMOS device is multi-fingered, we use the following equation to determine the resistance:

$$R_{\text{eff},0\_\text{target}} = R_N // \frac{R_P}{n_{\max}^2}$$

where R_N and R_P are the resistance of the decaps without fingers. This target $R_{\text{eff},0}$ sets up the equation for a maximum number of fingers, $n_{\max}$. That is

$$n_{\max} = \sqrt{\left(\frac{1}{R_{\text{eff},0\_\text{target}}} - \frac{1}{R_N}\right) R_P}. \tag{7}$$

As described in Section II, the optimal n depends on the frequency response (i.e., $C_{\text{avg}(n)}$), but the number of fingers selected should not exceed $n_{\max}$ to satisfy ESD requirements.

Fig. 12 illustrates the frequency response of the various designs from 0–10 GHz. All of the configurations provide similar $C_{\text{eff},0}$ values but are dramatically different in the frequency response characteristics. The standard 3N-4P case is the best, followed by the modified cross-coupled 1N-16P. The $R_{\text{eff},0}$ are different in all cases but only the standard 3N-4P case is unsuitable for ESD protection. However, it is desirable to select the configuration with the lowest $R_{\text{eff},0}$ that satisfies the ESD criteria (500 Ω in this case) for a rapid time-domain response. Overall, the cross-coupled 1N-16P layout is recommended because it provides the required $R_{\text{eff},0}$ for ESD reliability and saves at least 50%–60% on gate leakage.

To summarize, at 90 nm and below, standard-cell decap design should follow the layout strategy shown in Fig. 11. By using the smallest nMOS device and the largest multi-fingered pMOS device in the cross-coupled form, the decap has the lowest leakage and is able to satisfy the ESD requirements.

IV. Conclusion

This paper investigated the tradeoffs between high-frequency performance of decaps and ESD protection and its impact on the layout of standard cell decaps. We introduced a design metric to determine the optimal number of fingers to use in the standard cell layout to obtain a desired capacitance level over a target operating frequency. Models were developed to capture the frequency responses of R_{eff} and C_{eff} for a given technology with only a few parameters. As a result, the models can be used to predict the same characteristics of future technologies.

For ESD protection, a cross-coupled design was proposed by cell library developers to provide a large series resistance, but it suffers from reduced frequency response and provides no savings in gate leakage. This paper shows that more fingers are needed with the cross-coupled standard-cell layouts to provide the target resistance value for ESD protection. We show that the layout with the smallest nMOS device and a multi-fingered pMOS device delivers acceptable frequency response and ESD reliability, while providing the lowest leakage.

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References

[1] S. Pant and E. Chiprout, "Power grid physics and implications for CAD," in *Proc. 43rd ACM/IEEE Des. Autom. Conf.*, Jul. 2006, pp. 199–204.

[2] H. H. Chen and S. E. Schuster, "On-chip decoupling capacitor optimization for high-performance VLSI design," in *Proc. Int. Symp. VLSI Technol., Syst., Appl.*, May–Jun. 1995, pp. 99–103.

[3] H. H. Chen, J. S. Neely, M. F. Wang, and G. Co, "On-chip decoupling capacitor optimization for noise and leakage reduction," in *Proc. Symp. Integr. Circuits Syst. Des.*, Sep. 2003, pp. 319–326.

[4] M. Popovich, E. G. Friedman, M. Sotman, A. Kolodny, and R. M. Secareanu, "Maximum effective distance of on-chip decoupling capacitors in power distribution grids," in *Proc. ACM/IEEE Great Lakes Symp. VLSI*, 2006, pp. 173–179.

[5] D. A. Hodges, H. G. Jackson, and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd ed. New York: McGraw-Hill, 2004.

[6] M. Popovich and E. G. Friedman, "Decoupling capacitors for multi-voltage power distribution systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 3, pp. 217–228, Mar. 2006.

[7] J. Chia, "Design, layout and placement of on-chip decoupling capacitors in IP blocks," M.A.Sc. thesis, Dept. Elect. Comput. Eng., Univ. British Columbia, Vancouver, BC, Canada, 2004.

[8] H. Su, S. S. Sapatnekar, and S. R. Nassif, "Optimal decoupling capacitor sizing and placement for standard-cell layout designs," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 22, no. 4, pp. 428–436, Apr. 2003.

[9] J. R. Hauser, "Bias sweep rate effects on quasi-static capacitance of MOS capacitors," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 1009–1012, Jun. 1997.

[10] P. Larsson, "Parasitic resistance in an MOS transistor used as on-chip decoupling capacitance," *IEEE J. Solid-State Circuits*, vol. 32, no. 4, pp. 574–576, Apr. 1997.

[11] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. Hoboken, NJ: Wiley, 2002.

[12] Artisan Components Inc., Sunnyvale, CA, "TSMC 90 nm CLN90G Process SAGE-X v3.0 standard cell library databook, release 1.0," 2004.

[13] W. Liu, *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*. Hoboken, NJ: Wiley, 2001.

[14] H. Johnson and M. Graham, *High-Speed Digital Design*. Upper Saddle River, NJ: Prentice-Hall, 1993.

[15] X. Meng, K. Arabi, and R. Saleh, "Novel decoupling capacitor designs for sub-90 nm CMOS technology," in *Proc. Int. Symp. Quality Electron. Des.*, Mar. 2006, pp. 266–272.

[16] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[17] K. Cao, W.-C. Lee, W. Liu, X. Jin, P. Su, S. K. H. Fung, J. X. An, B. Yu, and C. Hu, "BSIM4 gate leakage model including source drain partition," in *Tech. Dig. Int. Electron Devices Meet.*, Dec. 2000, pp. 815–818.

[18] W.-C. Lee and C. Hu, "Modeling gate and substrate currents due to conduction- and valence-band electron and hole tunneling," in *Dig. Tech. Papers: Symp. VLSI Technol.*, Jun. 2000, pp. 198–199.

[19] F. Hamzaoglu and M. Stan, "Circuit-level techniques to control gate leakage for sub-100 nm CMOS," in *Proc. Int. Symp. Low Power Electron. Des.*, 2002, pp. 60–63.

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