LDO With Improved Common Gate Class-AB OTA Handles any Load Capacitors and Provides Fast Response to Load Transients

Cristian Răducan, Alina-Teodora Grăjdeanu, Cosmin-Sorin Plesa, Marius Neag, *Member, IEEE*, Andrei Negoiţă, and Marina Dana Ţopa, *Member, IEEE*

***Abstract*— This article proposes an LDO with fast response to load transients that can handle any practical capacitive loads. These features are mainly due to a novel frequency compensation circuit tailored for its error amplifier, which is based on an improved version of the popular common gate amplifier. A simple yet effective approach to the small-signal analysis of LDO with multiple feedback loops is employed to analyse intuitively the LDO and derive key design constraints. Simulation and measurement results performed on a test chip implemented in standard 130nm CMOS process validated the proposed LDO. It requires only 0.7μA quiescent current but exhibits an excellent response to load transients: when the load current jumps from 0A to 100mA in 1μs the output voltage presents an undershoot of 76mV and an overshoot of 198mV, without decoupling capacitors. It compares well against seven LDOs designed with common gate error amplifiers for similar levels of supply voltage, output voltage and current and against seven fast LDOs employing different error amplifiers. A figure-of-merit that considers the quiescent current, the maximum load current and capacitance, as well as the output voltage deviation, yielded a value for our LDO 39.8 times better than for the nearer competitor that employs common gate amplifier and 6 times better than the one employing a different error amplifier. When considering edge time and process scaling the performance of the proposed LDO is 4.8, respectively 4.5, times better than the second best in both comparisons.**

***Index Terms*— Class AB, common gate, fast LDO, any- capacitor LDO, multiple-feedback analysis.**

I. Introduction

LOW-DROPOUT voltage regulators (LDOs) are often used in switch-mode power supplies (SMPS) and large Systems-on-Chip (SoC) to separate the supply lines of analog sections sensitive to supply noise from the ones provided to the supply-polluting digital and power-switching sections [1]. For the latter, fast response to load transients is paramount. LDOs with very small output voltage variations are necessary for analog blocks such as precision amplifiers, ramp generators and voltage-controlled oscillators.

The number of pins available for external decoupling of internal LDOs is severely limited in these applications. Often, the LDOs must handle fast load and line transients without the aid of a large - thus external - decoupling capacitor, ensuring that the resulting output voltage undershoot/overshoot remain within the allowed range, usually no larger than +/- 20% of the nominal Vout value.

The various sections within an SMPS or SoC present significantly different capacitive loadings to the LDOs that supply them. The usual solution is to design different LDOs, each optimized for its specific load current. Obviously, it is more time- and effort-efficient to design an LDO capable of handling a wide range of output current and load capacitance.

Error amplifiers (EA) based on, or derived from, the push-pull common gate amplifier with large slew-rate proposed in [2] have been used extensively to implement LDOs with fast response to load and line transients.

The main improvements proposed over the years to the circuit in [2] are briefly analysed in the followings. In [3] the input stage was doubled and adaptive biasing was employed to speed up the LDO response to transients. The same authors introduced in [4] a slew-rate enhancement circuit, realized by embedding an RC network into the current mirrors within the main Gm cell of the EA.

To obtain even larger gain and slew-rate values, the initial circuit topology was modified in [5] to include the local common mode feedback (LCMFB) circuit proposed in [6]. The phase margin of the resulting LDO remained above 10° even at zero load current. However, the load capacitance range was limited to 0-100pF. Two important changes to the LDO proposed in [5] were introduced in [7]: a simple NMOS buffer was used to drive the input stage of the push-pull amplifier and the resistors within the LCMFB circuit were replaced NMOS transistors driven by fast comparators that monitor the output voltage. These changes improved significantly the LDO response to fast load and line transients in comparison to [5], but the load capacitance range was not enlarged.

Adaptive biasing of the push-pull amplifier was employed in [8] to further improve the LDO proposed in [5]. The transient performance of the resulting LDO was comparable with the one reported in [7], but at the cost of increasing the minimum load current necessary to ensure the LDO stability.

Manuscript received March 15, 2020; revised June 5, 2020 and July 7, 2020; accepted July 20, 2020. Date of publication September 1, 2020; date of current version October 30, 2020. This work was supported by the European Regional Development Fund through the Operational Program Competitiveness, POC-A1.2.3-G-2015, Project PartEnerIC under Grant 19/1st September 2016, project code P_40_437, SMIS 105742. This article was recommended by Associate Editor Y. Qin. *(Corresponding author: Cristian Răducan.)*

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Digital Object Identifier 10.1109/TCSI.2020.3012376

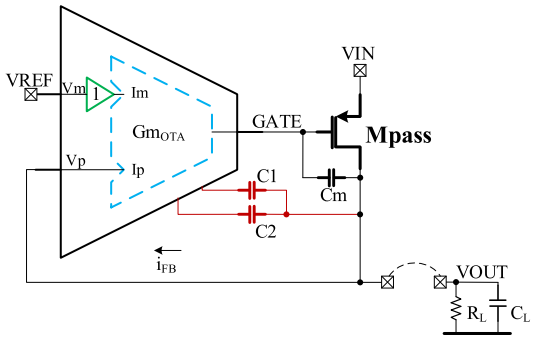

Fig. 1. Conceptual schematic of the any-CL fast LDO.

In [9] the current capability of the error amplifier was enhanced by implementing a local adaptive bias based on doubling the EA input stage and by using a current mirror with signal-dependent gain between the EA core and the pass transistor gate. The idea of doubling the EA input stage was also used in [10], but in conjunction with the current recycled folded cascode proposed in [11].

This article presents a novel improvement to the push-pull amplifier introduced in [5], based on which a fast LDO is proposed. Besides providing fast response to load and line transients, the proposed LDO can handle a wide range of load capacitors. The next section introduces the new LDO and presents an approximate, yet intuitive and effective, analysis of its stability. Section III presents a design example, validated through simulation results and measurements performed on a test chip. The final Section comprises a comprehensive comparison with state-of-the-art and a summary of main points presented in, and of conclusions drawn from, this work.

II. Proposed Any-CLoad Fast LDO

A. Schematic and Principle of Operation

Fig. 1 presents the conceptual schematic of the proposed LDO while Fig. 1 depicts its transistor level implementation. It employs a novel OTA, derived from the OTA proposed in [2] by employing two techniques for achieving a higher transconductance we described in [12]:

1) the current recycling introduced in [11] – implemented here by using two additional transistors for each input (M1A_B & M2A_B) and the current mirrors M3A-M3B & M4A-M4B.

2) the local common mode feedback (LCMFB), introduced in [6] to further increase the gain and slew-rate, implemented here by resistors R0.

The resulting fast OTA at the centre of the LDO is highlighted in Fig. 2. Its non-inverting and inverting inputs are formed by interconnecting the sources of transistors M1A_B and M2C, respectively M2A_B and M1C. Therefore, the reference voltage is applied to the non-inverting input through the buffer implemented by M11-M14 and Mbuff. The current outputted by the Fast OTA at node 1 is conveyed by the cascode M5 to the pass transistor gate; the current from the other OTA output is conveyed by cascode M6 to the cascoded current mirror M7-M10, which injects it into the pass transistor gate.

A novel frequency compensation is implemented by the capacitors C_1 and C_2 and the resistors R connected in the sources of transistors M4B and M9. Its operation will be analysed in the next Section. Circuit symmetry demands that resistors R are connected in the sources of transistors M3B and M10. Also, resistors k times larger than R are placed in the sources of transistors M3A and M4A, which have aspect ratios k times smaller than M3B and M4B.

By sizing R so that the products $Rg_{m3,4B}$ & $Rg_{m9,10}$ are much smaller than unity one ensures that the equivalent transconductance of the transistors with source degeneration is $Gmx_{ech} = \frac{g_{mx}}{1+Rg_{mx}} \cong g_{mx}$. Therefore, the transconductance of the OTA shown in Fig. 2 can be expressed as follows:

$$Gm_{OTA} = \frac{Io^+ - Io^-}{Vid} = 2g_{m1,2}(1 + g_{m3,4B}R_{g3,4B}) \quad (1)$$

in which $R_{g3,4B} = R0 \parallel r_{ds3,4A} \parallel r_{ds1,2B}$.

This transconductance is $(1 + g_{m3,4B}R_{g3,4B})$times larger than the transconductance the EA proposed in [2] can provide for same biasing and transistor sizes, and $\left(\frac{1}{g_{m3,4B}R_{g3,4B}} + 1\right)$ times larger than the one yielded by the EA proposed in [5] for same conditions.

Sizing R such that $Rg_{m3,4B}$ & $Rg_{m9,10} \ll 1$ also ensures suitable low-impedance nodes for connecting the capacitors C_1 and C_2. This arrangement is efficient not only for frequency compensation but also for boosting the slew-rate current that charges/discharges the large parasitic capacitance present at the Mpass gate. A variation of the output voltage is converted into displacement current through C_1 and C_2 and fed back to the gate of Mpass by means of current buffers M4B and M9.

It can be argued that the same effect can be achieved with fewer components by connecting capacitors C_1 and C_2 to nodes 1 & 2 (the sources of M5 and M7, respectively), as proposed in [13] and [14]. But this is only true if V1&V2 exhibit relatively small variations during LDO output voltage transients. This is not the case here – in fact, neither is in [13] or [14]. Transistors M4B/M9 (M7/M4 in [13], M20/M23 in [14]) will pull V1&V2 to GND/VIN during large output voltage undershoots/overshoots, significantly reducing the voltage variation dV/dt across C_1 and C_2. In turn, this leads to significantly less current available for discharging/charging the gate of Mpass. The circuit shown in Fig. 2 has the additional advantage that, during output voltage transients, the signal driving the gate of transistors M4B and M9 is in opposite phase to the one delivered by C_1 and C_2 to their sources. As a result, the impedance seen at the sources of M4B and M9 is dynamically reduced, thereby improving the transient performance of the circuit.

A small value capacitor, C_m, was placed between the Mpass gate and drain. It helps speed up the LDO response during the initial phase of the output voltage transient, when the currents generated by the class-AB Fast OTA and the capacitors C_1 & C_2 are relatively small. Note that C_m plays no major role in the LDO frequency compensation.

The available bias current should be split between stages considering the trade-off between the gain-bandwidth product (GBW) of the LDO and its slew-rate. As a rule of thumb, 70-80% should be allocated to the fast OTA while

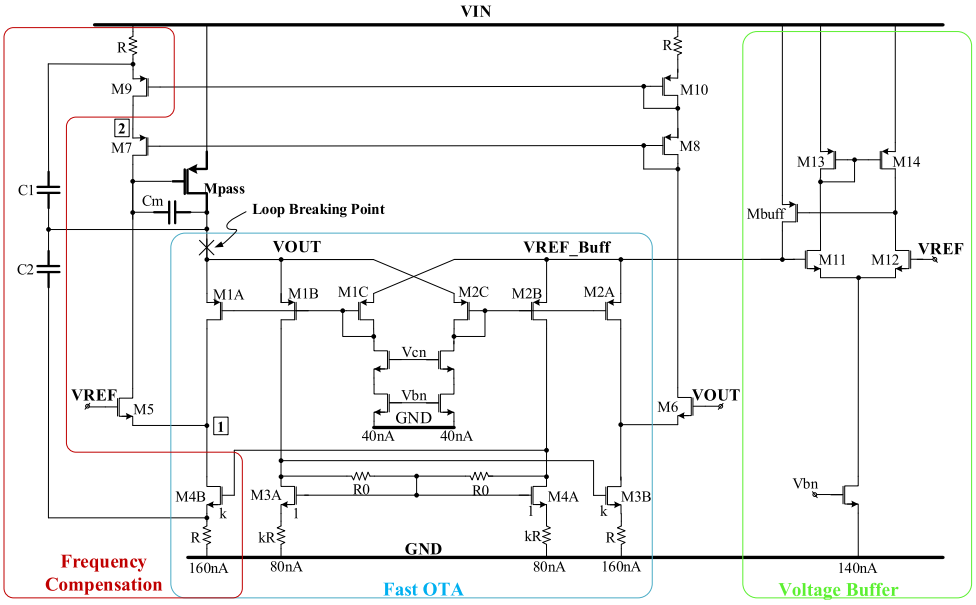

Fig. 2. Transistor level schematic of the proposed LDO.

the remaining 20-30% are necessary for the voltage buffer. An example is given in Fig. 2, for a total quiescent current of 700nA: the values of biasing currents are indicated there for each circuit branch.

B. Stability Analysis

Most stability analyses presented so far focused on the loop-gain of the main voltage-control loop, derived by breaking the loop between the LDO output and the error amplifier input, as indicated in Fig. 2. The common-gate amplifier does not present a large input impedance, so it has to be properly taken into consideration. In turn, this results in rather cumbersome expressions for the loop gain.

This Section aims to provide an effective, yet simple and intuitive, stability analysis of the proposed LDO that considers the impact of the main voltage and local current feedback loops, both individually and combined, as well as the impact of the small input impedance of the error amplifier.

Starting from the approximate graphical analysis method introduced in [15] and [16] we developed a method for analysing the circuit proposed in Fig. 2 that provides qualitative insight into the operation of the novel frequency compensation circuit. The first step is to represent the frequency compensation circuit as an inner feedback loop within the main voltage-control feedback loop. Next, the circuit encompassed by the inner loop is replaced by its closed-loop equivalent, according to the classical feedback theory. This process is to be repeated if multiple feedback loops are present. Eventually, one obtains an equivalent circuit that consists of only one feedback loop. The LDO stability is analysed by considering both the inner feedback loops and the return ratio of the equivalent single loop.

The return ratio is obtained by using Rosenstark's formula [17]. It does not depend on the point the loop is broken at [18].

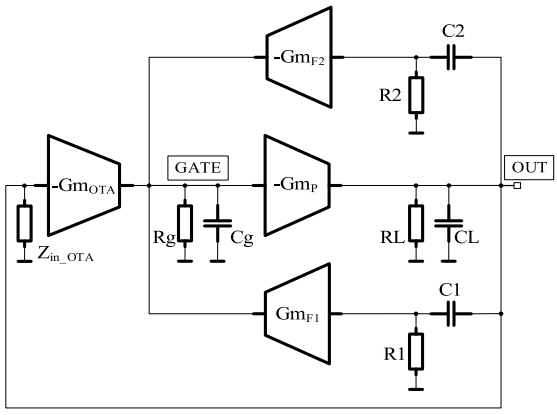

Fig. 3. Small signal block diagram of the proposed LDO.

Fig. 3 presents the small signal model of the circuit proposed in Fig. 2: Gm_{OTA} is the equivalent transconductance of the OTA, given by (1), Gm_P is the transconductance of the pass transistor and Gm_{F1}, Gm_{F2} are the transconductances of transistors M4B and M9, respectively. By making Gm_{F1}=Gm_{F2} = Gm_F, C1 = C2 = C and R1 = R2 = R the LDO model shown in Fig.3 can be reduced to the simplified one presented in Fig. 4.a). This model highlights the fact that the local compensation circuit closes a parallel-parallel feedback loop around the pass transistor. The inner loop we alluded to can be easily identified: it comprises a direct gain path (a_{INNER}) and a feedback path (f_{INNER}). It can be replaced by its closed-loop equivalent, as shown in Fig 4.b). The natural closed-loop gain corresponding to the parallel-parallel feedback topology is the transimpedance, $Z_{t_{INNER}}$:

$$Z_{t_{INNER}} = \frac{v_{out}}{i_\Sigma} = \frac{1}{f_{INNER}} \frac{T_{INNER}}{1 + T_{INNER}} \tag{2}$$

In (2) T_{INNER} is the loop gain of the inner loop and has the following expression:

$$T_{INNER} = a_{INNER} f_{INNER} \tag{3}$$

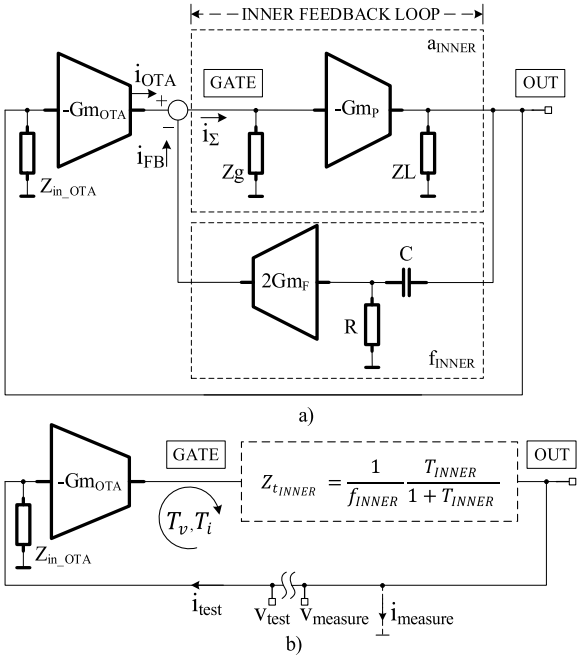

Fig. 4. Simplified representations of the small-signal model for the proposed LDO: a). derived directly from the circuit shown in Fig. 3 for Gm_{F1}=Gm_{F2} = Gm_F, C1 = C2 = C, R1 = R2 = R and b). inner loop represented by its equivalent circuit, derived by using classical feedback theory.

where:

$$a_{INNER} = \frac{G_{mP} R_g R_L}{(1 + sR_gC_g)(1 + sR_LC_L)} \tag{4}$$

$$f_{INNER} = 2\frac{sRCG_{mF}}{(1 + sRC)} \tag{5}$$

From (3),(4) and (5) T_{INNER} can be written as:

$$T_{INNER} = \frac{2sRC(G_{mF}G_{mP}R_gR_L)}{(1 + sR_gC_g)(1 + sR_LC_L)(1 + sRC)} \tag{6}$$

The LDO stability depends on both the inner loop and the single-feedback loop equivalent small-signal representation shown in Fig 4.b). The return ratio is used for the latter [17]:

$$T_{LDO} = \frac{T_iT_v}{T_i + T_v} \tag{7}$$

where T_v and T_i are, respectively, the voltage and the current transfer ratios. They are derived by breaking the loop to create a pair of "Test" and "Measure" nodes; then, a test voltage and a test current are applied successively to the "Test" node and the resulting open-circuit voltage and short-circuit current are measured at node "Measure", as shown in Fig 4.b).

The LDO is stable when both the inner loop and the equivalent single-feedback loop meet the usual stability criteria:

$$T_{INNER} \neq -1 \& T_{LDO} \neq -1 \tag{8}$$

Analysis of T_{LDO}

Direct circuit analysis performed on the small-signal model shown in Fig 4.b) yields the voltage transfer ratio T_v:

$$T_v = \frac{v_{measure}}{v_{test}} = G_{mOTA}Z_{t\_INNER} \tag{9}$$

Fig. 5 presents the small-signal model of the circuit shown in Fig. 2 used to derive the current transfer ratio T_i. Note that

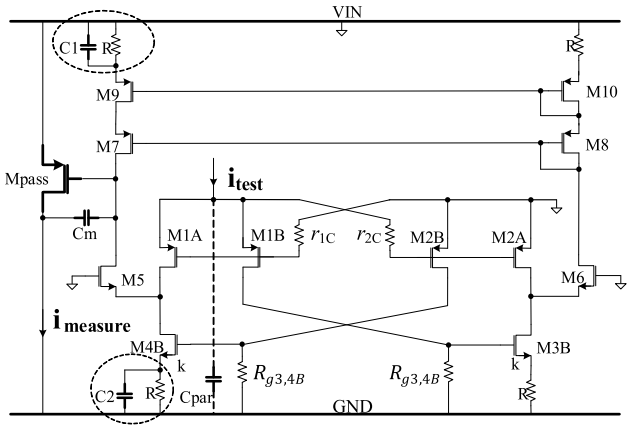

Fig. 5. Small-signal model of the circuit shown in Fig. 2 used to derive the current transfer ratio T_i.

the LDO output is shorted to ground in order to determine the short-circuit current, $i_{measure}$. Capacitors $C1$ and $C2$ appear in parallel with resistors R; this introduces a non-dominant pole and a zero in the current transfer ratio, T_i, approximately given by $\omega_{p2}^{Ti} = \frac{1+gm_{9,4B}R}{R(C_1+C_2)}$ and $\omega_z^{Ti} = \frac{1}{R(C_1+C_2)}$. The products gm_9R and $gm_{4B}R$ are set by design to a value much smaller than one – as explained in Section II A. Therefore, ω_z^{Ti} will cancel the effect of ω_{p2}^{Ti}. It follows that the frequency characteristics of the current transfer ratio, T_i, are set mainly by the dominant pole given by the equivalent resistance, R_g, and the parasitic capacitance, C_g, seen at the Mpass gate:

$$T_i = \frac{i_{measure}}{i_{test}} \cong \left(1 + g_{m3,4B}R_{g3,4B}\right) R_gG_{mP} \frac{1}{1 + sR_gC_g} \tag{10}$$

in which $R_{g3,4B} = R0 \parallel (g_{m3,4A}r_{ds3,4A})kR \parallel r_{ds1,2B}$.

The loop gain of the LDO can now be derived by combining T_i and T_v according to (7).

Note that the voltage and current transfer ratios appear "in parallel"; this suggests that, if one of these ratios is far smaller than the other one, the resulting loop gain T_{LDO} is mainly determined by the smaller transfer ratio. The ratio between the DC gain of the current and voltage transfer ratios is given by:

$$\frac{|T_i|}{|T_v|} = \frac{1}{2g_{m1,2}R_L} \propto IL \tag{11}$$

From (11) it follows that at small load currents, the overall LDO DC gain is mainly determined by the current transfer ratio. It will be shown later that the dominant pole of T_v appears at much lower frequencies than the dominant pole of T_i shown in (10). Therefore, the phase margin of T_{LDO} is determined by the frequency characteristic of T_v, as illustrated in Fig. 6.

At high load currents, the LDO DC gain and phase margin are determined mainly by the voltage transfer ratio, which has a far smaller gain than the current transfer ratio, as shown in Fig. 7. The high frequency non-dominant pole of T_i, ω_{ndp}^{Ti}, is due to the small value parasitic capacitance, $Cpar$, ranging in tens of fF which is present at the input of the error amplifier.

To conclude, the frequency characteristics of T_{LDO} are determined near the unity gain frequency by the characteristics of T_v. Therefore, the analysis will focus on T_v.

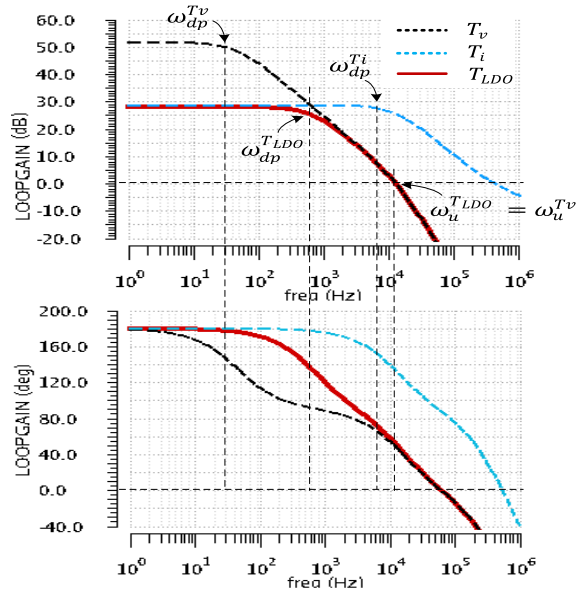

Fig. 6. Frequency characteristics of the transfer ratios described by (7) & (9) and return ratio described by (10) for small values of IL.

From (9) it follows that:

$$T_v = G_{mOTA}\, a_{INNER} \text{ if } T_{INNER} \ll 1 \tag{12}$$

$$T_v = G_{mOTA}\, \frac{1}{f_{INNER}} \text{ if } T_{INNER} \gg 1 \tag{13}$$

Let us define $A_h = |G_{mOTA} \frac{1}{f_{INNER}}|$ for $\omega \gg \omega_z$. From Fig. 5 it follows that:

$$A_h = \frac{G_{mOTA}}{G_{mF}} \tag{14}$$

An effective way of ensuring a good phase margin is to force the T_v magnitude characteristic to cross the 0dB axis with a slope of -20dB/decade. This is equivalent to ensuring that $A_h < 1$. Fig. 8 indicates that for pulsations larger than the value of the T_v secondary pole, $\omega_{sp}^{T_v}$, the magnitude characteristic of T_v rolls off with a slope of -40dB/decade. Considering that $\omega_{dp}^{T_v} \ll \omega_u^{T_v}$, the phase margin of T_v can be approximated by:

$$PM_{T_v} = 90° - tan^{-1}(A_h) \tag{15}$$

It follows that A_h can be written as:

$$A_h = \tan(90° - PM_{T_v}) \tag{16}$$

The T_v unity-gain frequency, ω_u, can be obtained by finding the intersection between $G_{mOTA} \frac{1}{f_{INNER}}$ and the 0dB axis:

$$\omega_u^{T_v} = \frac{G_{mOTA}}{2RCG_{mF}} = \frac{1}{2} A_h \frac{1}{RC} \tag{17}$$

Analysis of T_{INNER}

For a $PM_{T_{INNER}} \geq 45°$ the second zero-crossing of the T_{INNER} module characteristic, denoted by pulsation ω_{u2}, must happen before the occurrence of the third pole pulsation, ω_3.

$$\omega_{u2} \leq \omega_3 \tag{18}$$

This condition is met if the following inequality is true:

$$1 < |T_{INNER}|_{max} \leq \frac{\omega_3}{\omega_2} \tag{19}$$

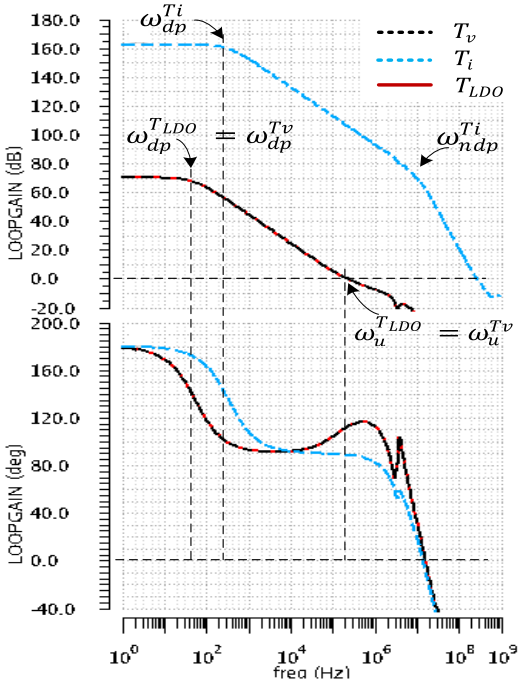

Fig. 7. Frequency characteristics of transfer ratios described by (7) & (9) and return ratio described by (10) for large values of IL.

The expression of $|T_{INNER}|_{max}$ depends on the position of the dominant pole, ω_1. In turn, ω_1 is set by the loading conditions. $R_L C_L < R_g C_g$ for large load currents or if the output capacitor has a small value. In these conditions, the dominant pole of T_{INNER} is given by $\omega_1 = \frac{1}{R_g C_g}$, which translates (19) into:

$$1 < \frac{C}{C_L}(G_{mF} G_{mP} R_g R) \leq \frac{R_L C_L}{RC} \tag{20}$$

At small load currents and/or large load capacitance one the $R_L C_L$ time constant becomes larger than $R_g C_g$. Thus, the dominant pole changes to $\omega_1 = \frac{1}{R_L C_L}$. This translates (19) into:

$$1 < \frac{C}{C_g}(G_{mF} G_{mP} R_L R) \leq \frac{R_g C_g}{RC} \tag{21}$$

The main design constraints result by combining (20) and (21):

$$max\left\{\frac{C_L}{G_{mF} G_{mP} R_g}, \frac{C_g}{G_{mf} G_{mP} R_L}\right\} \leq RC \leq \sqrt{\frac{C_g C_L}{G_{mF} G_{mP}}} \tag{22}$$

The frequency compensation circuitry shown in Fig. 2 - capacitors C_1, C_2 and resistors R connected to the sources of transistors M4B and M9 – implements a capacitance multiplier with the gain approximately $2G_{mF} Z_G$, largely independent on the load current and capacitance. As explained in Section II.A, [13], [14] proposed a fairly similar, but less effective, topology.

III. Design Example

A. LDO Requirements and Simulation Results

The circuit proposed in Fig. 2 was used to implement the LDOs required to separate the supply lines of digital control circuitry and PWM generator within and integrated SMPS.

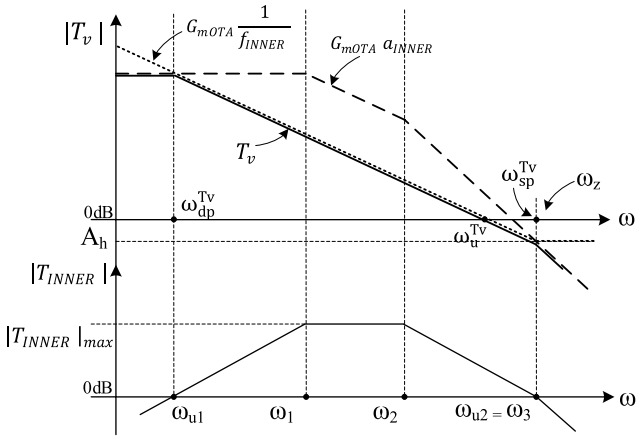

Fig. 8. Frequency characteristics of the transmittance and transfer ratio described by (4), (5), (6) and (9).

The LDO was implemented in a standard 130nm CMOS process for the following requirements: output voltage VOUT=1V when VIN varies between 1.2V and 1.5V, the load current, IL, varies from 0 to100mA and the load capacitance, CL, takes values from practically 0 to 1μF. Quiescent current consumption: nominal value 700nA, at room temperature.

The LDO phase margin had to be maintained above 5 degrees over the entire range of values given above for the load current and capacitance, and over the full automotive temperature range, -40°C to +150°C. The LDO response to line and load transients should maintain the output voltage undershoot (-ΔVout) and overshoot (+ΔVout) within 20% of the nominal VOUT value.

The design constrains (22) are key factors for sizing the circuit shown in Fig. 2. Fig. 9 presents a 3D representation of (22), considering the design requirements listed above. The lower limit represents the term $max\left\{\frac{C_L}{G_{mF}G_{mP}R_g}, \frac{C_g}{G_{mF}G_{mP}R_L}\right\}$ while the upper limit represents the term $\sqrt{\frac{C_gC_L}{G_{mF}G_{mP}}}$. The space between these surfaces encompasses all suitable RC values.

One notices that a complete $RC = constant$ plane cannot be placed between these limits. This means that no singular RC value can meet (15) for all possible combinations of IL and CL values. Fortunately, the frequency compensation needs only to deal with the IL and CL values for which the uncompensated voltage loop has a smaller-than-required phase margin. Here, this occurs only when both IL and CL take small or large values, at the limits of their respective ranges (0 to100mA and 0 to 1μF). Consequently, the RC value is chosen so that the area of the corresponding RC = constant plane that remains between the lower and upper limits is maximized and includes these combinations of extreme values for IL and CL.

In this case, the RC value should be chosen so that the constraints defined by (22) are met at small load currents for CL values up to 10nF and at large load current for CL values ranging from 40nF up to 1μF. The frequency compensation network of the circuit shown in Fig. 2 was sized as follows: C1=C2=15pF, R=20kΩ and R0=300kΩ. The value of Cm was set to only 4pF, as this capacitor is effective only during the initial phase of the LDO response to output voltage transients.

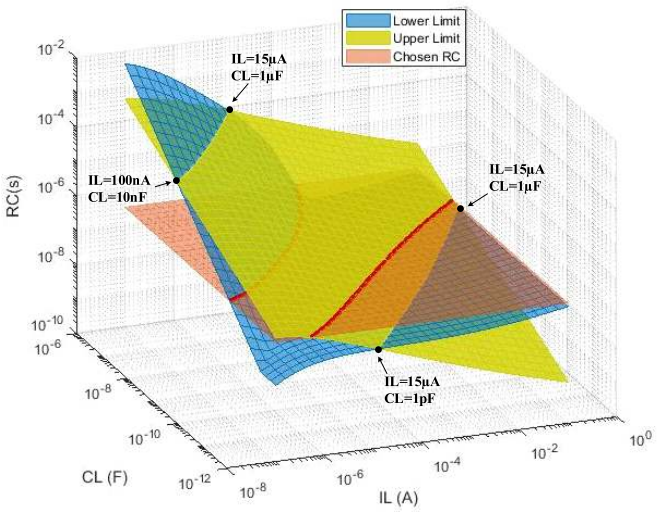

Fig. 9. A 3D representation of (22) illustrating the lower and upper limits for the acceptable values of RC, four intersection points between lower and upper limits and the chosen RC value (R=20kΩ and C1=C2=C=15pF).

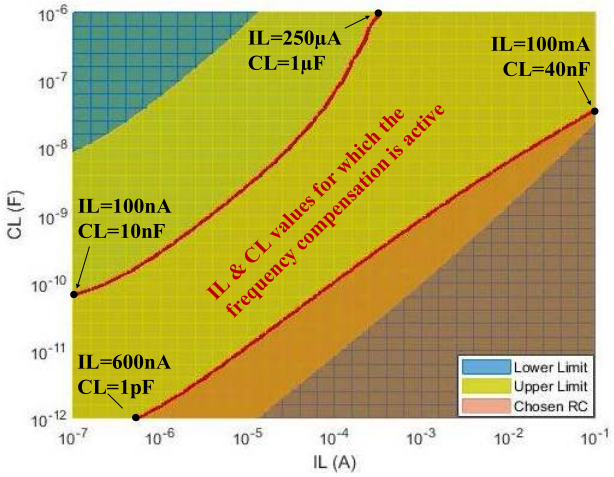

Fig. 10. Top view of the 3D representation of (22) shown in Fig. 9, that highlights the (IL, CL) area for which the feedback compensation is active.

Fig. 10 illustrates the top view of the 3D representation of (22) shown in Fig. 9. The red curves resulted from the intersections between the chosen RC = constant plane and the lower and upper limits defined by (22). One notices that the conditions mentioned above are met: the part of the RC = constant plane that fits between the limits is delimited by the following points: IL=100nA & CL=10nF, IL=600nA & CL=1pF, IL=100mA & CL=40nF, IL=250μA & CL=1μF.

Fig. 11 presents the frequency characteristics of the LDO loop gain, T_{LDO}, at room temperature for CL=0F and seven values of the load current, between 0 and 100mA. At zero load current the current transfer ratio has a relatively small DC value and sets the DC loop gain value to 28dB. The DC gain of the current transfer ratio increases with the load current, and so does the overall DC loop gain, up to the point where it gets close to the DC gain of the voltage transfer ratio. From there on, the voltage transfer ratio limits the DC loop gain. The inner voltage compensation loop ensures that the poles of T_{LDO} are widely separated, which results in large values for the phase margin, up to 113 degrees at IL=100mA.

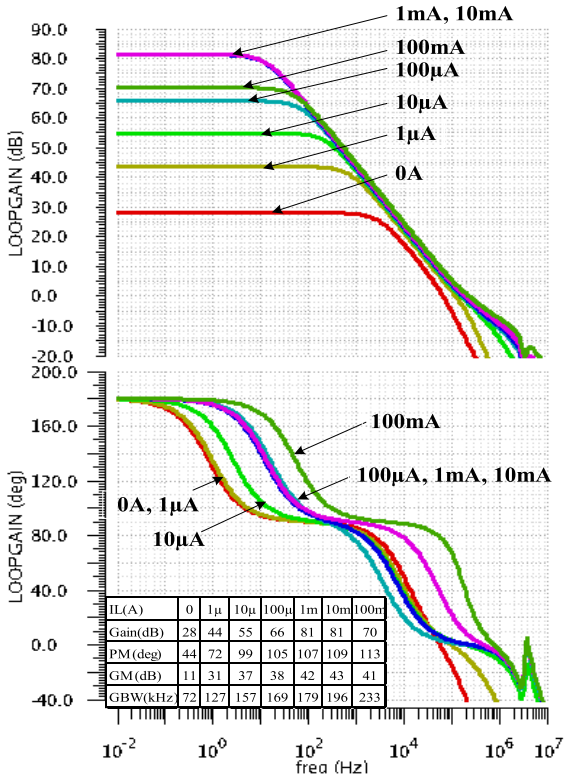

Fig. 11. Frequency characteristics of the LDO loop gain, T_{LDO}, at room temperature, for CL=0 and seven IL values between 0 and 100mA.

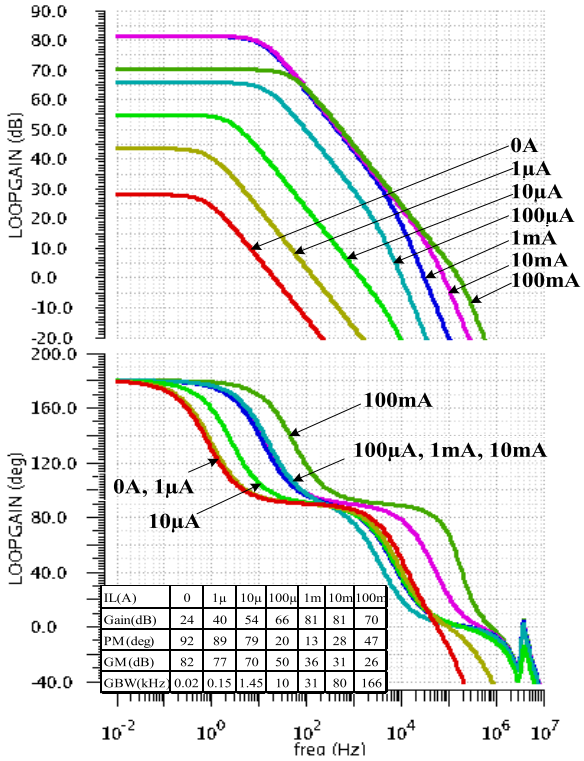

Fig. 12. Frequency characteristics of the LDO loop gain, T_{LDO}, at room temperature, for CL=1μF and seven IL values between 0 and 100mA.

Fig. 12 presents the loop gain characteristics at room temperature for CL=1μF and the same seven values of the load current. At zero load current the characteristics are determined by the current transfer ratio; the dominant pole is set by CL and is located at a very low frequency. Thus, the DC loop gain has a relatively small value, similar to the CL=0F case, but the loop gain bandwidth is determined by the load capacitor. The DC loop gain increases with the load current, and the unity-gain frequency gets closer to the second pole. However, the LDO poles remain sufficiently far apart, even for the maximum load current where the phase margin value is 47 degrees.

Fig. 13 depicts the way the LDO Phase Margin at room temperature depends on the CL and IL values. The global minimum value for the Phase Margin, over the entire range of values defined for CL (0 to 1μF) and IL (0 to100mA) is 10° and occurs for CL=1μF and IL=316μA.Therefore, the case CL=1μF should be analysed in more detail.

Fig. 14 presents the LDO Phase and Gain Margins for CL=1μF and IL varying between 0 and 100mA, at three die temperatures: -40°C, +25°C and +150°C. The smallest Phase Margin value is obtained for -40°C and IL=150μA; at 7° it is only three degrees smaller than minimum value obtained at room temperature and meets the design requirements. The Gain Margin values are larger than 20dB at all temperatures.

This analysis was repeated for several other CL values, with similar results: die temperature does not a have a major impact on the minimum values of the LDO Phase and Gain Margins, which remain above the set limits for all test conditions. This validates the theoretical analysis presented in Section II B.

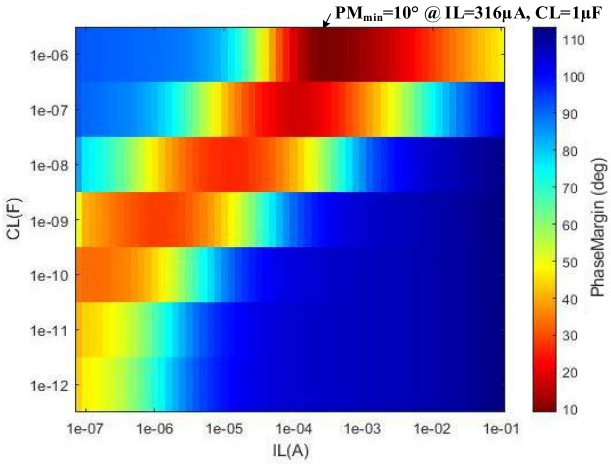

Fig. 13. Phase Margin (PM) at room temperature when CL and IL are swept over their entire range of values: CL = 0 to 1μF, IL= 0 to 100mA.

Fig. 15 shows the frequency characteristic of the LDO Power Supply Rejection (PSR), for CL values starting from 1pF up to 1μF. These characteristics start from the same low- frequency value, -60dB, have a common zero at 750Hz, present a peak at a frequency inversely proportional to CL, then drop with the expected slope of -20dB/decade.

The LDO output noise is shown in Fig. 16 for a load current of 1mA. The main noise contributors are the input transistors of the fast OTA, of which size was optimized for maximum speed.

Fig. 17 shows the LDO response to large load variations for CL=0. At t=100us, the load current jumps from zero up to

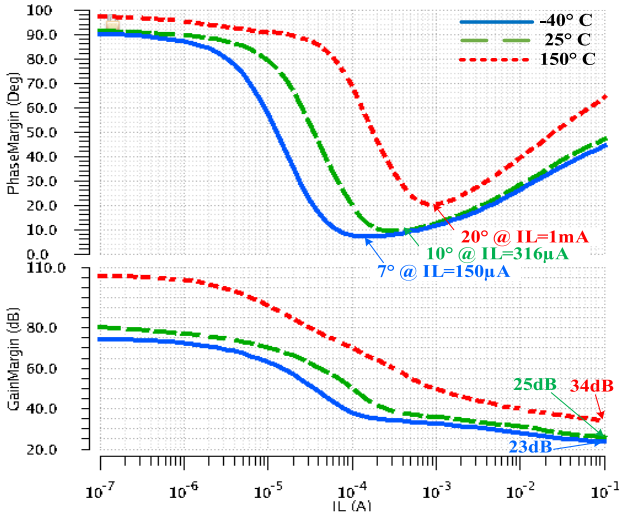

Fig. 14. Phase and Gain Margin for CL = 1μF and IL varying from zero to 100mA, at three die temperatures: -40°C, +25°C and +150°C.

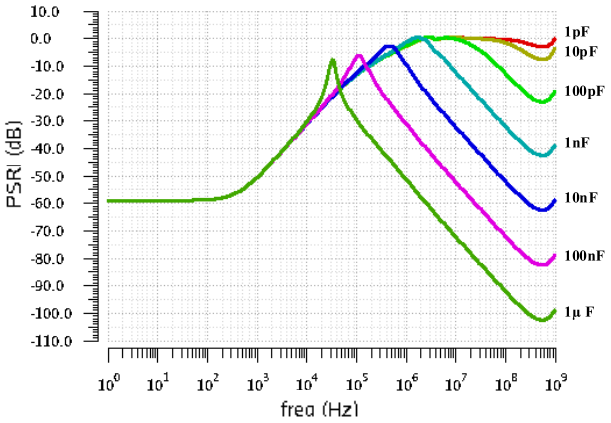

Fig. 15. PSR for CL values from 1pF to 1μF at IL=1mA.

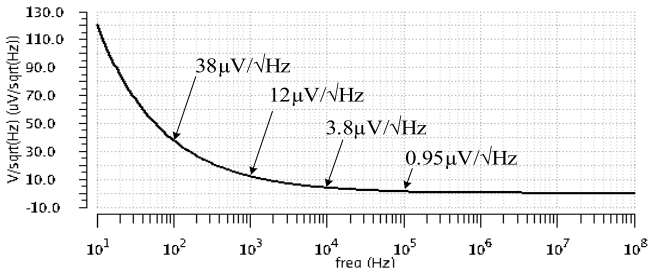

Fig. 16. LDO output noise for IL=1mA.

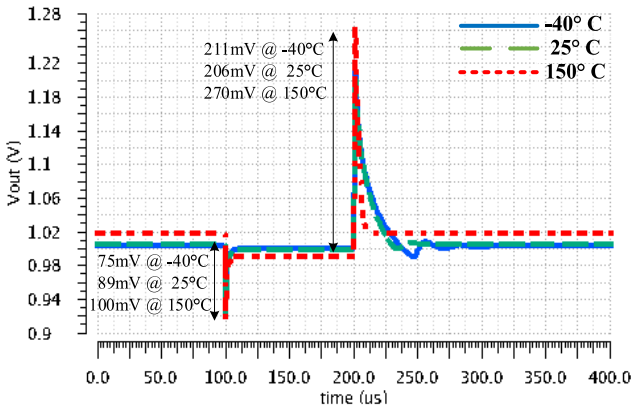

Fig. 17. LDO response to load current stepping up from zero to 100mA (at t=100us) and back to zero (at t=200us); VDD=1.5V, CL=0F, Trise=Tfall = 1μs.

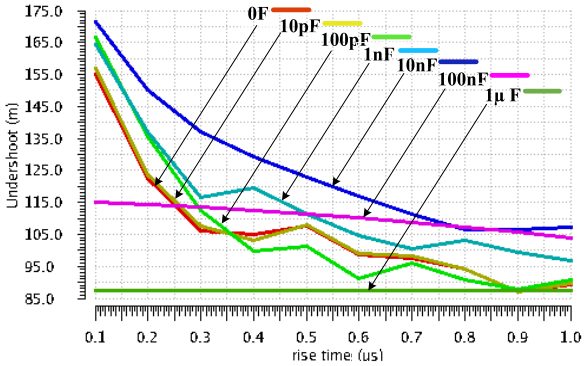

Fig. 18. Output voltage undershoot caused by load current stepping up from zero to 100mA with Trise from 100ns to 1μs, for CL between zero and 1μF.

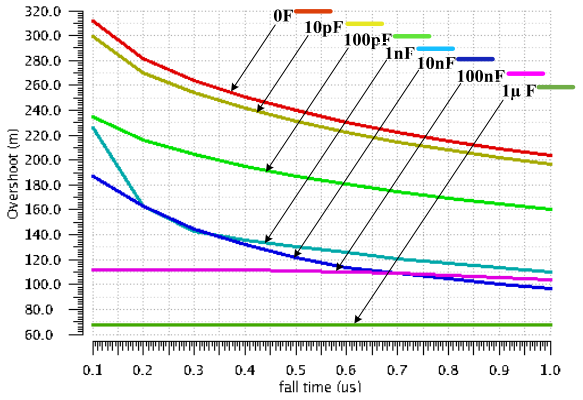

Fig. 19. Output voltage overshoot caused by load current stepping down from 100mA to zero with Tfall from 100ns to 1μs, for CL between zero and 1μF.

100mA in 1μs; at t=200us the load current jumps back, from 100mA down to zero, again in 1μs. The resulting LDO output voltage undershoot, respectively overshoot, values are detailed for three die temperatures. At temperatures above 125°C the leakage currents have a significant impact on the LDO performance, leading to larger voltage undershoot/overshoot, and on the LDO precision, leading to a DC offset to the output voltage.

Another factor that impacts the voltage undershoot/overshoot is the rise and fall time of the load current step. Fig. 18 presents the variation of the LDO output voltage undershoot caused by the load current jumping from zero up to 100mA, when the rise time varies between 100ns and 1μs.

Fig. 19 presents the LDO output voltage overshoot caused by the load current jumping from 100mA down to zero, when the fall time varies between 100ns and 1μs. One notices that the output voltage variation depends strongly on the rise/fall time for CL values smaller than 10nF. For CL values above 100nF the undershoot & overshoot values remain below 115mV, respectively 120mV, for all rise/fall times.

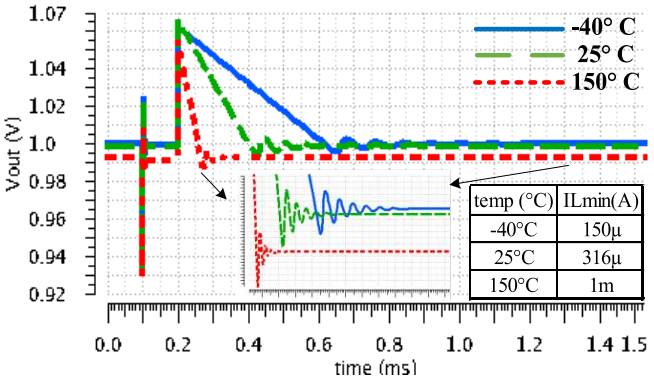

Fig. 20. LDO response to a load current step from ILmin to 100mA (at t=100us) and back to zero (at t=200us) in 100ns for three values of ILmin, at three temperatures (-40C, 25C and 150C). VDD=1.5V and CL=1μF.

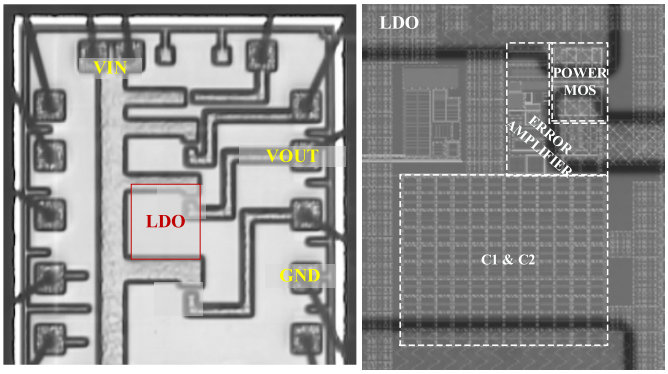

Fig. 21. Left: Micrograph of the test chip that comprises the proposed LDO. Right: Zoom-in that reveals the LDO floorplan. High-density capacitors were not available for this test chip.

Fig. 20 shows the LDO response to load current jumps related to the three settings that yielded the smallest Phase Margin values recorded in Fig. 14. The load current was first set to the values indicated in Fig. 14: 150μA for -40°C, 316μA for +25°C, 1mA for +150°C. At t=100us the load current jumps up to 100mA in 100ns; at t=200us the load current jumps back to the initial value, again in 100ns. The LDO output voltage presents a small ringing that settles fairly quickly; this confirms that the LDO is stable, even if for these conditions the Phase margin values are under 10°.

B. Silicon Implementation and Measurement Results

The LDO described in the previous Section was integrated in a larger test chip. Fig. 21 presents the chip micrograph, with a zoom-in that details the floorplan of the integrated LDO. One notices the relatively large area occupied by the compensation capacitors C1 and C2. In future implementations the die area can be substantially reduced by employing high-density metal capacitors, which were not available for this test chip.

This Section presents measurement results for the novel LDO presented in this article, focusing on its main features: fast response to line and load transients.

First, let us analyse the test setup described in [14] for measuring the load transient response of an LDO, depicted in Fig. 22.a). One notices that the gate-drain parasitic capacitance of the NMOS, denoted Cpar in Fig. 22.a), creates a

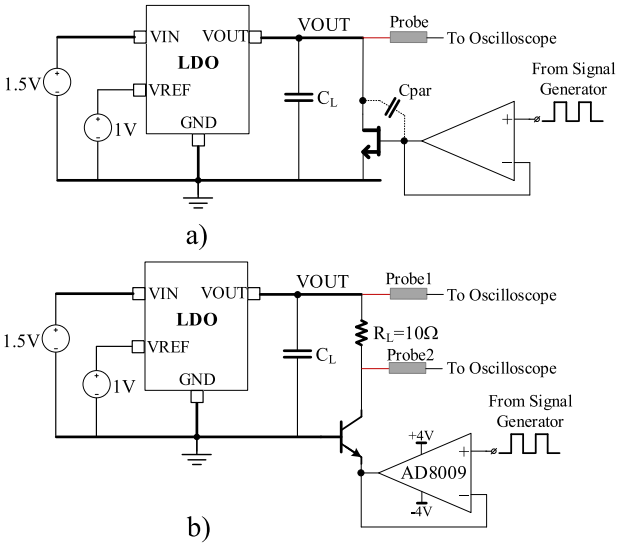

Fig. 22. Test setup for investigating the load transient response of an LDO, a) conventional [14] and b) proposed.

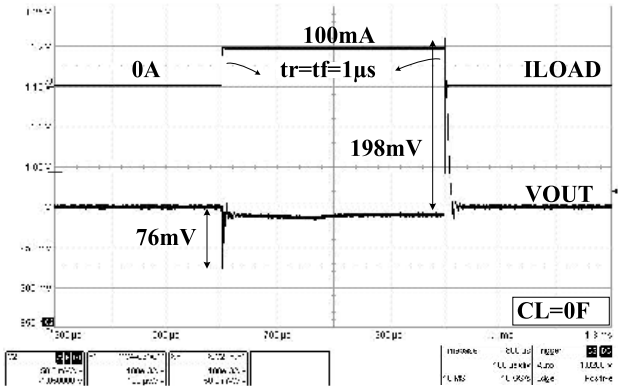

Fig. 23. Measured response to a load step of 100mA in 1μs for VDD=1.5V and CL=0F (plus 50pF from the scope probe).

charge-injection path between the large control signal applied to the NMOS gate and CL. Therefore, the output voltage undershoot/overshoot cannot be accurately measured with this setup [14]. The new test setup proposed in Fig. 22.b) significantly reduces the charge injection into CL. First, an NPN, with smaller parasitic capacitances than the NMOS shown in Fig. 22.a), was used as a switching transistor. Second, the NPN was placed in a common-base connection, with the control signal applied to its emitter. The load current is monitored in real time, but indirectly: Probes 1 & 2 allow the voltage drop it causes across the load resistor RL to be measured accurately. By using a very fast OpAmp, with large output current capability (the AD8009 has GBW=1GHz, SR=5500V/μs and Iout_max=175mA) the LDO load current could be stepped up/down with slopes up to 100mA/μs.

Fig. 23 and Fig. 24 show the measured LDO response to load transients for the extreme values of the load capacitance, zero and 1μF, respectively. The maximum load capacitor employed in measurements was 1μF only for practical reasons, but the LDO can handle even larger loads, as indicated by Fig. 14.

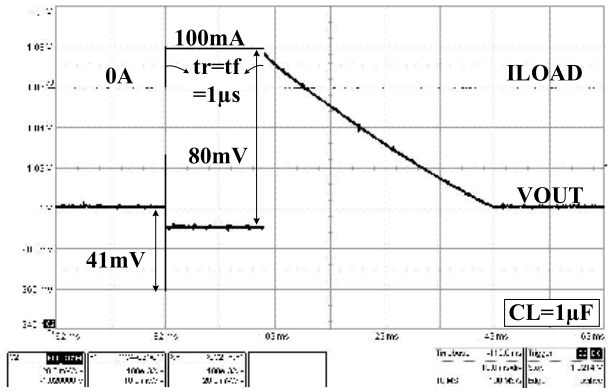

Fig. 24. Measured response to a load step of 100mA in 1μs for VDD=1.5V and CL=1μF.

Measurement and simulation results are in good correlation:

- For CL=0F, Fig. 23 gives a measured undershoot of 76mV and an overshoot of 198mV; these data compare well against the corresponding simulated results shown in Fig. 17: the simulated values for the voltage undershoot and overshoot are 89mV and 206mV, respectively.

- For CL=1μF, Fig. 24 shows a measured undershoot of 41mV and an overshoot of 80mV.

The simulated LDO response for these conditions – not shown due to space constraints - is similar to the one shown in Fig. 20.

Fig. 25 shows the LDO response to a line jump - that is, Vin stepping up and down between 1.2V and 1.5V with a slope of 120mV/μs. An output voltage overshoot of 31mV and an undershoot of 28mV are measured when no decoupling capacitor is present.

IV. Comparison With State-of-the-Art & Conclusions

A. Comparison With State-of-the-Art

For a comprehensive comparison of the LDO presented in Section III against state-of-the art we employ three of the most popular Figures-of-Merit (FOM) proposed in the literature:

- FOM1 proposed in [19] is effective for comparing LDOs with widely different values for the quiescent current, I_q, maximum load capacitance C_L and load current, I_{L_max}:

$$FOM1 = \frac{\Delta V_{out\_pkpk} \cdot C_L \cdot I_q}{I_{L\_max}^2} \tag{23}$$

where ΔV_{out_pkpk} is the maximum output voltage variation (undershoot + overshoot) caused by a large current load step.

- FOM2 introduced in [20] allows the comparison of capacitorless LDOs. It takes into account the rise/fall time of the load current step, which has a particularly large impact on the step response of LDOs that operate with no, or only a small decoupling capacitor, at their output:

$$FOM2 = K\frac{\Delta V_{out\_pkpk} \cdot I_q}{\Delta I_L} \tag{24}$$

where $K = \frac{\Delta t \ used \ in \ measurement}{the \ smallest \Delta t \ among \ desings \ for \ comparison}$ and ΔI_L is the amplitude of the load current step.

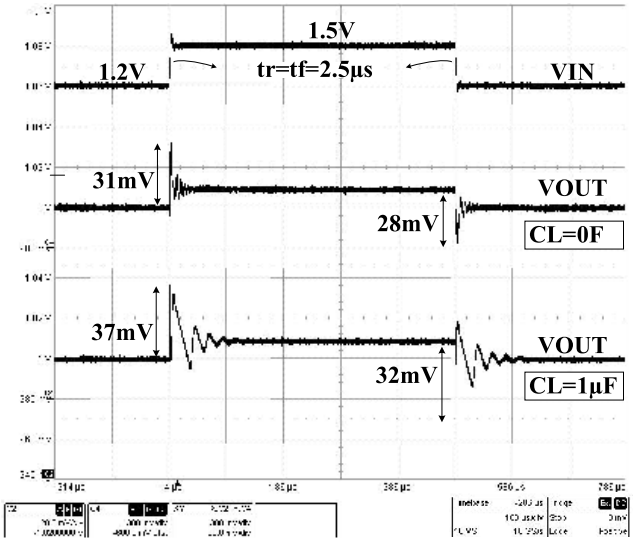

Fig. 25. Measured response to a line step of 300mV in 2.5 μs for CL=0&1μF at IL=1mA.

- FOM3 was proposed in [21] as an expanded version of FOM2. First, it introduces a sublinear relationship between ΔV_{out_pkpk} and K; next, it includes a process-dependent factor – $FO4_{Delay}$, the propagation delay of a standard CMOS invertor with fan-out of four – to obtain a process normalized FOM:

$$FOM3 = K^{1/3}\left[\frac{\Delta V_{out\_pkpk}(I_q + I_{L\_min})}{FO4_{Delay} \cdot \Delta I_L}\right] \tag{25}$$

For all three cases the smaller the FOM value, the better the LDO transient performance.

Table I lists the main parameters of the LDO proposed in Fig. 2, and the resulting values of the three FOMs described above, along with the corresponding data for seven LDO reported previously, which also use common gate amplifiers. Table II allows for a direct comparison between the LDO presented here and a second set of LDOs published recently, [22]–[28], which use other types of error amplifiers.

The LDO presented in this work can handle the widest range of CL values, of all LDOs listed in Tables I and II. Note that an own implementation of the topology proposed in [13], [14] in 0.13μm CMOS was able to handle CL between 40pF and 1μF.

Let us first analyse comparatively the LDO with common gate error amplifiers listed in Table I. The LDO proposed here boasts the smallest voltage undershoot, denoted $-\Delta$Vout in Table I, two time smaller than nearest competitor, [9]. However, its voltage overshoot, denoted $+\Delta$ Vout in Table I, is among the largest reported by the LDOs there. Our LDO ranks second in respect to the maximum output voltage variation, ΔV_{out_pkpk}.

The best overall performance measured by the FOMs defined by (23)-(25), is provided by the LDO described in this work:

- best FOM1, with a value 39.8 times better than the nearest competitor, the LDO proposed in [13];

- best FOM2 value, 1.5 times better than the second best, [9];

TABLE I
PERFORMANCE COMPARISON WITH LDOs EMPLOYING COMMON GATE ERROR AMPLIFIERS

PARAMETER	[2]	[4]	[21]	[5]	[9]	[13]	[14]	**This work**
Year	2007	2012	2013	2013	2016	2019	2020	**2020**
CMOS [μm]	0.35	0.35	0.5	0.18	0.35	0.065	0.065	**0.13**
FO4Delay(ps)[c]	90	90	130	47	90	17	17	**35**
Supply Voltage [V]	1-1.8	2.5-4	2	1.2	1.8	0.95-1.2	0.95-1.2	**1.2-1.5**
Output Voltage [V]	0.9	2.3	1.5	1	1.6	0.8	0.8	**1**
Dropout Voltage [mV]	100	150	123	100	200	150	150	**100**
Iq [μA]	1.2	7	5.34	3.7	14	13.9	14	**0.7**
DC Line Reg.[mV/V]	4.75	1	–	–	–	0.48	12	**16.6**
DC Load Reg. [μV/mA]	148	80	–	–	–	8.03	90	**100**
PSR [dB]	–	–	–	–	–	-47@10kHz	-33@10kHz	**-30@10kHz[d]**
CL [F]	0-100p	0-100p	100p	10p-100p	0-50p	0-100p[e]	0-100p [e]	**0-1μ**
–ΔVout [mV]	–	236[b]	-	277	147	404	230	**76**
+ΔVout [mV]	–	227 [b]	-	-	57	145	133	**198**
ΔVout_pkpk= +ΔVout – (–ΔVout) [mV]	750[a]	463	585.2	377[a]	204	549	363	**274**
IL_{MIN} – IL_{MAX}	50μA-50mA	50μA-100mA	1μA-100mA	10μA - 100mA	1mA-100mA	0-100mA	0-100mA	**0-100mA**
Avg. IL t_{rise} (ns)	–	500	100	1000	100	50	132.5	**1000**
Rise time ratio (K)	–	10	2	20	2	1	2.65	**20**
FOM1 [fs]	36.07	33.03	125.05	14.23	14.56*	7.63**	50.82	**0.19****
FOM2 [mV]	–	0.33	0.13	0.28	0.06	0.08	0.13	**0.04**
FOM3 [V/μs]	–	6.38	0.72	3.01	29.25	4.49	4.14	**0.15**

a) Estimated from Fig. 8 in [5]; b) For CL=100pF; c) Values taken from [21]; d) From simulation; e) Simulations run on an own 0.13um implementation of the topology proposed in [13]-[14] shown that it can drive up to 1μF. *Computed for CL=50p; **A CL value of 10pF was considered instead of 0F

- best FOM3 value, 4.8 times better than the nearest competitor, the LDO proposed in [21].

The LDO proposed here also compares well against the recently published fast LDOs presented in Table II, which do not employ the common gate topology for their error amplifiers:

- second best with respect to current consumption. Note that the LDO with the lowest Iq, [25], has the largest ΔV_{out_pkpk}.
- best FOM1 value, 6 times better than the second best, [22]
- best FOM3 value, 4.5 times better than the nearest competitor, the LDO proposed in [22].

It should be noted that the best values for FOM2 were obtained by two LDOs implemented in 65nm processes. The LDO described in this work yielded an FOM2 value close to the other LDO implemented in 130nm CMOS process, [24], even if that LDO requires a much larger quiescent current and can handle a far smaller load current and capacitance.

B. Summary and Conclusions

This article describes a new LDO with fast response to load transients that can handle any practical capacitive loads.

Starting from a popular common gate OTA with large slew rate, an improved version was developed for the main error amplifier: under same biasing conditions it yields a transconductance several times larger than previous designs based on the same topology. Also, the OTA output stage, that drives the pass transistor gate, operates in class-AB. Finally, a novel frequency compensation was devised for this OTA, which also helps improve the LDO response to load transients. It implements a capacitance multiplier with the gain largely independent of the load current and capacitance, which realizes an effective Miller-type compensation. Moreover, it helps improve the large-signal transient performance of the LDO.

An intuitive yet effective approach to the stability analysis of the proposed LDO was introduced:

- the small-signal representation of the circuit, that included the main voltage feedback loop and two local, fast current feedback loops, was reduced to increasingly simpler equivalent models: first, the local loops were represented by one inner feedback loop; next, an equivalent single-feedback model for the entire LDO was derived.
- the return ratio of the resulting small-signal model was analysed by using Rosenstark's theorem but avoiding cumbersome algebraic expressions. Instead of a complete mathematical analysis, the analysis focused on the interplay between the voltage and current transfer ratios, considering various scenarios for the load current and capacitance. This analysis demonstrated that, for the worst-case situations with respect to stability, the frequency characteristics of the LDO return ratio are determined near the unity-gain frequency by the characteristics of the voltage transfer ratio.
- finally, the relationship between the LDO voltage transfer ratio and the gain of the inner feedback loop was analysed by using a graphical method. This yielded key design constraints that needed to be observed in order to ensure the LDO stability.

This method for stability analysis can be extended to a wide class of circuits with multiple feedback loops.

TABLE II
PERFORMANCE COMPARISON WITH RECENT PUBLICATIONS

PARAMETER	[22]	[23]	[24]	[25]	[26]	[27]	[28]	**This work**
Year	2017	2017	2018	2018	2019	2019	2019	**2020**
CMOS [um]	0.18	0.18	0.13	0.065	0.065	0.18	0.18	**0.13**
FO4Delay(ps)*	47	47	35	17	17	47	47	**35**
Supply Voltage [V]	1.2	1.4-1.8	1-1.4	1	1.3	1.2-1.8	1.2-1.8	**1.2-1.5**
Output Voltage [V]	1	1.2	0.8	0.8	0.6-1.1	0.8-1.6	1	**1**
Dropout Voltage [mV]	200	200	200	200	200	–	200	**100**
Iq [µA]	3.14	16.6-31.6	112	0.03	50-190	10.2	43	**0.7**
DC Line Reg.[mV/V]	0.69	0.13	2.25	–	1	–	0.24	**16.6**
DC Load Reg. [µV/mA]	15	2.7	173	1220	40	–	1.76	**100**
PSR [dB]	-20@10kHz	-65@1kHz -53@10kHz	−57@1MHz −22@10MHz	-24@1MHz	-35@10kHz [a]	–	-58.8@1kHz -48.7@10kHz	**-50@1kHz** **-30@10kHz**[b]
CL [F]	10p	0-300p	0-25p	10p	0-2n	0-100p	100p	**0-1µ**
–ΔVout [mV]	220	39	13	487.5	80	190	131.6	**76**
+ΔVout [mV]	150	42	22	163.6	77	200	126.3	**198**
ΔVout_pkpk= +ΔVout – (–ΔVout) [mV]	370	81	35	651.1	157	390	257.9	**274**
$IL_{MIN} - IL_{MAX}$ [A]	0-100m	0-100m	120µ-25m	100n-10m	100µ -50m	1m-100m	0-100m	**0-100m**
Avg. IL t_{rise} (ns)	1000	300	10	600	2	100	300	**1000**
Rise time ratio (K)	500	150	5	300	1	50	150	**500**
FOM1 [fs]	1.16	19.52**	31.66	1.95	75.66**.***	40.59	110.89	**0.19*** **
FOM2 [mV]	5.81	2.93**	0.79	0.59	0.38**	2.01	16.63	**0.96**
FOM3 [V/µs]	1.9 6	2.21**	15.95	3.33	40.72**	311.93	12.54	**0.43**

a) Estimated from Fig.19 in [26]; b) From simulation; *Values taken from [21]; **The average value of Iq was used; ***CL =10pF was considered instead of 0F

Simulation and measurement results performed on a test chip demonstrated the potential of the novel circuit and validated the analysis. The LDO was implemented in standard 130nm CMOS process, and its quiescent current was set to only 700nA in typical conditions. It shown excellent response to load current stepping up and down between zero and 100mA in 1μs: the output voltage presented an undershoot of 76mV and an overshoot of 198mV, without decoupling capacitors.

A comprehensive comparative analysis against state-of-the-art was also presented. Three Figure-of-Merit were used to assess the performance of the new LDO compared to fourteen previously published LDOs, designed for similar levels of supply voltage, output voltage and load current.

The LDO presented in this work can handle the widest range of load capacitances of all LDOs considered here. Measurements were performed only for CL values from zero and 1μF but simulation results indicated that the LDO remained stable as the CL value increases beyond 1μF, over the full automotive temperature range, -40°C to +150°C.

The improvements to the popular common-gate topology introduced in this article were validated by direct comparison against seven LDOs with error amplifiers based on the same topology. The new LDO came up best in respect to all three FOM metrics for overall performance, with scores between 1.5 and almost 40 times better than the second best.

Another contribution worth noting is the improved test setup for monitoring the LDO response to load transient response: it significantly reduced the charge injection into CL that occurred in testbenches proposed previously.

REFERENCES

[1] Q. Duong *et al.*, "Multiple-loop design technique for high-performance low-dropout regulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2533–2549, Oct. 2017.

[2] T. Y. Man, P. K. T. Mok, and M. Chan, "A high slew-rate push–pull output amplifier for low-quiescent current low-dropout regulators with transient-response improvement," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 9, pp. 755–759, Sep. 2007.

[3] X. Ming, Z.-K. Zhou, and B. Zhang, "A low-power ultra-fast capacitor-less LDO with advanced dynamic push-pull techniques," in *Proc. IEEE/IFIP 19th Int. Conf. VLSI Syst. Chip*, Oct. 2011, pp. 54–59.

[4] X. Ming, Q. Li, Z.-K. Zhou, and B. Zhang, "An ultrafast adaptively biased capacitorless LDO with dynamic charging control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 1, pp. 40–44, Jan. 2012.

[5] A. Saberkari, R. Fathipour, H. Martinez, A. Poveda, and E. Alarcon, "Output-capacitorless CMOS LDO regulator based on high slew-rate current-mode transconductance amplifier," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 1484–1487.

[6] J. Ramirez-Angulo and M. Holmes, "Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS op-amps," *Electron. Lett.*, vol. 38, no. 23, p. 1409, 2002.

[7] S. S. Chi, W. Hu, M. H. Fan, Y. S. Xu, and G. L. Chen, "Transient response enhancement with fast transient controller for capacitor-less LDO regulator," *Appl. Mech. Mater.*, vols. 543–547, pp. 800–805, Mar. 2014.

[8] C.-C. Lim, N.-S. Lai, G.-H. Tan, and H. Ramiah, "A low-power fast transient output capacitor-free adaptively biased LDO based on slew rate enhancement for SoC applications," *Microelectron. J.*, vol. 46, no. 8, pp. 740–749, Aug. 2015.

[9] S. Zhen, J. Wang, D. Yang, C. Cao, and P. Luo, "A load-transient-enhanced output-capacitor-free low-dropout regulator based on an ultra-fast push-pull amplifier," in *Proc. IEEE 11th Int. Conf. ASIC (ASICON)*, Nov. 2015, pp. 1–4.

[10] C. Desai, D. Mandal, B. Bakkaloglu, and S. Kiaei, "A 1.66 mV FOM output cap-less LDO with current-reused dynamic biasing and 20 ns settling time," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 2, pp. 50–53, Feb. 2018.

[11] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2535–2542, Sep. 2009.
[12] C. Raducan and M. Neag, "Capacitorless LDO with fast transient response based on a high slew-rate error amplifier," in *Proc. Int. Semiconductor Conf. (CAS)*, Oct. 2015, pp. 285–288.
[13] H. Qian and J. Guo, "A 1.26-ps-FoM output-capacitorless LDO with dual-path active-feedback frequency compensation and current-reused dynamic biasing in 65-nm CMOS technology," in *Proc. IEEE 13th Int. Conf. ASIC (ASICON)*, Oct. 2019, pp. 1–4.
[14] G. Li, H. Qian, J. Guo, B. Mo, Y. Lu, and D. Chen, "Dual active-feedback frequency compensation for output-capacitorless LDO with transient and stability enhancement in 65-nm CMOS," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 415–429, Jan. 2020.
[15] K. H. Lundberg, "Internal and external op-amp compensation: A control-centric tutorial," in *Proc. Amer. Control Conf.*, 2004, pp. 5197–5211.
[16] S. Tepwimonpetkun, B. Pholpoke, and W. Wattanapanitch, "Graphical analysis and design of multistage operational amplifiers with active feedback miller compensation," *Int. J. Circuit Theory Appl.*, vol. 44, no. 3, pp. 562–583, Mar. 2016.
[17] S. Rosenstark, "Loop gain measurement in feedback amplifiers," *Int. J. Electron.*, vol. 57, no. 3, pp. 415–421, Sep. 1984.
[18] M. Neag, R. Onet, I. Kovacs, and P. Martari, "Comparative analysis of simulation-based methods for deriving the phase- and gain-margins of feedback circuits with op-amps," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 625–634, Mar. 2015.
[19] P. Hazucha, T. Karnik, B. Bloechel, C. Parsons, D. Finan, and S. Borkar, "An area-efficient, integrated, linear regulator with ultra-fast load regulation," in *Symp. VLSI Circuits. Dig. Tech. Papers*, vol. 40, Oct. 2004, pp. 218–221.
[20] J. Guo and K. N. Leung, "A 6-μW chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896–1905, Sep. 2010.
[21] P. M. Furth, S. Krishnapurapu, S. H. Pakala, and M. A. Haque, "A 5.3μA quiescent current fully-integrated low-dropout (LDO) regulator with transient recovery time enhancement," in *Proc. IEEE 56th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Dec. 2013, pp. 9–12.
[22] V. Shirmohammadli, A. Saberkari, H. Martinez-Garcia, and E. Alarcon-Cot, "Low power output-capacitorless class-AB CMOS LDO regulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 2–5.
[23] Y. Zeng, Y. Li, X. Zhang, and H.-Z. Tan, "A push-pulled FVF based output-capacitorless LDO with adaptive power transistors," *Microelectron. J.*, vol. 64, pp. 69–77, Jun. 2017.
[24] S. Bu, J. Guo, and K. N. Leung, "A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth >100 MHz in 130-nm CMOS," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3232–3246, Apr. 2018.
[25] Y. Huang, Y. Lu, F. Maloberti, and R. P. Martins, "Nano-ampere low-dropout regulator designs for IoT devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 4017–4026, Nov. 2018.
[26] M. Huang, H. Feng, and Y. Lu, "A fully integrated FVF-based low-dropout regulator with wide load capacitance and current ranges," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11880–11888, Dec. 2019.
[27] J. Tang, J. Lee, and J. Roh, "Low-power fast-transient capacitor-less LDO regulator with high slew-rate class-AB amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 3, pp. 462–466, Mar. 2019.
[28] X. Xin, J. Cai, Y. Shen, Y. Huang, and K. Yang, "A 99.96% efficiency capacitor-free low-dropout regulator with cross-couple class-AB push–pull input stage for wireless Internet of Things chip," *Anal. Integr. Circuits Signal Process.*, vol. 99, no. 2, pp. 455–466, May 2019.

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