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# Leakage and Breakdown Mechanisms of GaN Vertical Power FinFETs

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This work studies the leakage and breakdown mechanisms of 1.2 kV GaN vertical power FinFETs with edge termination. Two competing leakage and breakdown mechanisms have been identified. The first mechanism is dominated by electric field, with the leakage current dominated by electric field in the drift region and destructive breakdown voltage by peak electric field at the edge termination. The second leakage and breakdown mechanism is controlled by an energy (or potential) barrier in the fin channel. This energy barrier suffers the drain-induced barrier lowering (DIBL) effect, and is highly dependent on gate/drain biases, fin geometries and GaN/oxide interface charges. The electrons injected into the drift region due to the DIBL effect further lead to a trap-assisted space-charge-limited conduction, which results in a non-destructive early breakdown. The barrier height in the fin channel determines which mechanism is dominant; the same device could show either destructive or non-destructive breakdown at different gate biases. To enable the normally-off power switching, it is important to suppress the leakage from the second mechanism and maintain a sufficiently high energy barrier in the fin channel up to high drain voltages. Finally, key device parameters determining the energy barrier in the fin channel have been identified. The findings in this work provide critical device understanding and design guidelines for GaN vertical power FinFETs and other 'junctionless' vertical high-voltage power transistors.

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Wide bandgap semiconductors, such as SiC, GaN, diamond and $Ga_2O_3$, are promising candidates for power electronics applications.[1-7] At present, GaN are becoming a mainstream power semiconductor material as a consequence of its outstanding physical properties, commercial availability of large-diameter wafers, and maturity of technological processes.[1-2] Lateral GaN power transistors have been commercialized up to 650 V recently.[2] Vertical GaN transistors have been regarded as the next-generation technologies to push GaN beyond 650 V, due to their advantages over lateral GaN transistors: 1) higher breakdown voltage (*BV*) and current for a given chip area; 2) potential superior reliability, as high electric field regions are far away from device surface, and 3) easier thermal management.[8] Until now, several structures have been demonstrated for vertical GaN power transistors, including current-aperture vertical electron transistors (CAVETs),[9-11] trench MOSFETs,[12-13] and power FinFETs.[14-16]

The vertical power FinFET was recently proposed that combines the fin-shaped channels, similar to the ones used in the FinFETs for digital applications, [17-18] and a thick and lightly-doped drift region which accommodates high current and high voltage needed for power switching applications. In addition, the narrow fin channels can deplete all electrons at zero gate bias due to the work function difference between the gate metal and GaN, enabling the normally-off operation. Compared to CAVETs and trench MOSFETs, GaN vertical power FinFETs (Fig. 1 (a)) only need n-GaN layers and do not require epitaxial regrowth, which greatly reduces the fabrication complexity and cost. Following the first demonstration,[14] GaN vertical power FinFETs have demonstrated promising performance, with a *BV* of 1.2 kV and a specific on-resistance ($R_{on,sp}$) of 1 m$\Omega\cdot$cm$^2$.[15] A large-area 1.2 kV, 5 A transistor was recently demonstrated with a record switching figure-of-merit (i.e. product of $R_{on}$ and switching charges) among all 0.9-1.2 kV Si, SiC and GaN power transistors.[16]

Despite this excellent performance, the leakage and breakdown mechanisms of GaN vertical power FinFETs have not been fully understood. In conventional power MOSFETs, the breakdown is typically determined by the buried pn junctions. Due to the lack of p-type material in power FinFETs, the leakage and breakdown mechanisms in the vertical power FinFET, a 'junctionless' power transistor, are expected to be quite different. Prior studies have reported a destructive breakdown in vertical GaN power FinFETs with a ~200 nm fin width.[14-16] Although the FinFETs with larger fin widths also showed a positive threshold voltage,[15] their leakage and breakdown mechanisms were not clear. Understanding the dependence of these mechanisms on the fin width is key to evaluate the device design trade-offs. In addition, the leakage and breakdown mechanisms at different gate biases have not been clarified, which is important to the design of gate driver for vertical GaN power FinFETs in converter applications. This work fills these gaps in knowledge regarding the vertical GaN power FinFETs. Two completing leakage and breakdown mechanisms are unveiled, one leading to destructive breakdown while the other leading to non-destructive breakdown. The key factors determining the dominant mechanism is also identified.

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The epitaxial structure in this work consists of a 0.3 μm-thick $n^+$-GaN cap layer (Si: $3\times10^{19}$ $cm^{-3}$) and ~9 μm-thick $n^-$-GaN drift layer on 2-inch $n^+$-GaN substrates. The net donor concentration and electron mobility were revealed to be ~$5\times10^{15}$ $cm^{-3}$ and ~1000 $cm^2$/V·s in the drift region, by characterizing a vertical GaN Schottky barrier diode fabricated in the wafer. FinFETs with various fin widths from 200 nm to 500 nm were fabricated in the same wafer. The fin height and gate length are 1.3 μm and 0.75 μm, respectively, for all devices. Device fabrication started with the fin etch and corner rounding.[19] Edge termination was then formed by argon (Ar) implantation (dose: $10^{16}$ $cm^{-2}$, energy: 150 keV) at the device periphery. This termination technique had only been used in our GaN diodes[20-21] but not in GaN FinFETs before. A diode structure was fabricated in the same wafer to access the effectiveness of edge termination in boosting the *BV*, as shown in Fig. 1(b). Significant *BV* improvement was observed, enabling a *BV* over 1.2 kV (Fig. 1(c)). After edge termination, the remaining fabrication steps for spacer oxides and gate, source and drain contacts were similar to our previous report.[15] Fig. 1(d) shows a cross-sectional scanning electron microscopy image of the fin region in the fabricated device with a 200 nm fin width.

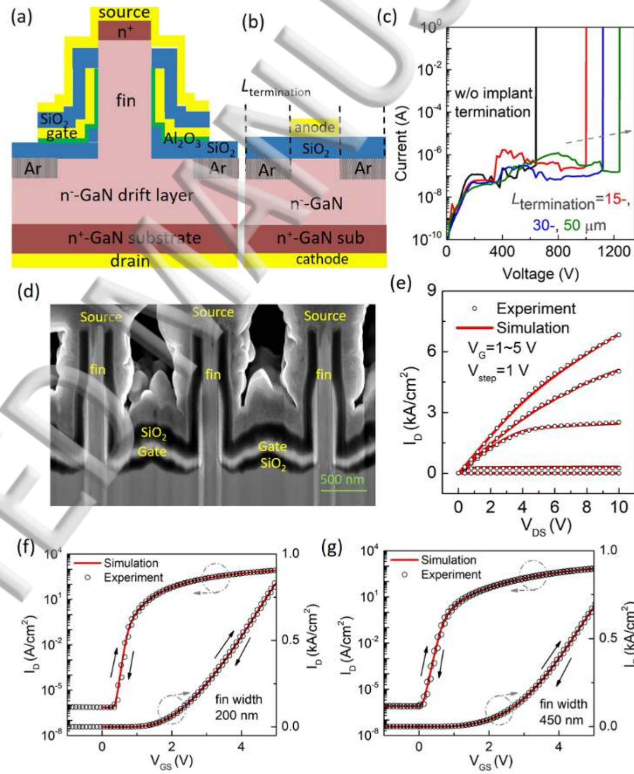


FIG 1. (a) Schematics of a unit-cell of GaN vertical power FinFETs with argon-based edge implantation and (b) a diode test structure for the evaluation of edge termination. (c) Reverse *I-V* characteristics of the diode test structure with different distances between the metal edge and termination edge. (d) Cross-sectional scanning electron microscopy image of the fin area in a fabricated GaN vertical FinFET with 200 nm fin width. (e) Representative output characteristics of GaN vertical power FinFETs from experiment (pulse measurement) and simulation. Double-sweep transfer characteristics for devices with (f) 200- and (g) 450-nm fin widths at $V_{DS}$=1 V, with the current in both log scale and linear scale. Simulation data are also shown, exhibiting good agreement with experimental data.



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To assist the device analysis, physics-based device simulation was developed for our GaN vertical power FinFETs, by using the TCAD simulator Silvaco Atlas. The physical models were based on our previous simulation for vertical GaN power transistors.[8] Self-heating was not accounted in the simulation model, as it has negligible impact on device leakage and breakdown. The device simulation models were calibrated to the experimental *I-V* characteristics in pulse measurements (to avoid self-heating), as shown in Fig. 1(e). Excellent agreement between simulation and experiment has been achieved.

Fig. 1 (f) and (g) show the double-sweep transfer characteristics of the fabricated GaN FinFETs with the fin width of 200 nm and 450 nm, respectively. All the current densities used in this work were normalized with respect to the total device active area, which includes fin areas and fin spacing areas but does not include edge termination areas. Both devices exhibit a positive threshold voltage ($V_{th}$) with a hysteresis below 0.1 V, indicating very small interface states/traps in our devices.[22] As shown in Fig. 1(f) and (g), the simulations without consideration of interface traps agree well with the experiment. Further incorporation of interface traps in simulation could allow to fit this small hysteresis,[23] which is beyond the technical scope of this paper. The $V_{th}$ was extracted by the constant current method at 1 mA/cm$^2$, being ~0.5 V and ~0.3 V for FinFETs with 200-nm and 450-nm fin width. The $V_{th}$ is slightly higher for narrower fins, due to the stronger fin depletion by the sidewall gate stacks. The extracted $V_{th}$ is lower than the $V_{th}$ calculated merely considering the fin depletion and the work functions of metal and GaN [see Equation (1) below], indicating the existence of fixed positive charges at the GaN/$Al_2O_3$ interfaces ($Q_{ox}$).[15,24] The amount of $Q_{ox}$ can be estimated from the following equation for $V_{th}$[15,24]

$$V_{th} \approx [W_M - \chi_{GaN} - kTln(N_C/N_D)] - qN_D W^2/8\varepsilon_{GaN} - Q_{ox}/C_{ox} \quad (1)$$

where $W_M$ is the metal work function (4.95 eV in our devices); $\chi_{GaN}$, $N_C$ and $\varepsilon_{GaN}$ are the electron affinity, conduction band density of states and permittivity of GaN, respectively; $N_D$ and $W$ are the net donor concentration and width of the fin channel; $C_{ox}$ is capacitance per unit area of the gate oxide (15 nm $Al_2O_3$ in our devices). From (1), a consistent $Q_{ox}$ of ~$10^{12}$ cm$^{-2}$ was derived for FinFETs with different fin widths. This $Q_{ox}$ amount was further verified by our simulation.

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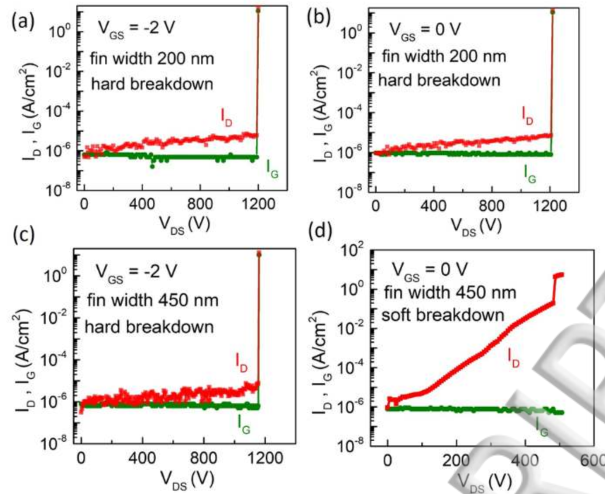


FIG. 2. Representative off-state drain and gate leakage characteristics for the FinFETs with 200- and 450-nm fin widths, measured at $V_{GS}$ of 0 V and -2 V, respectively.

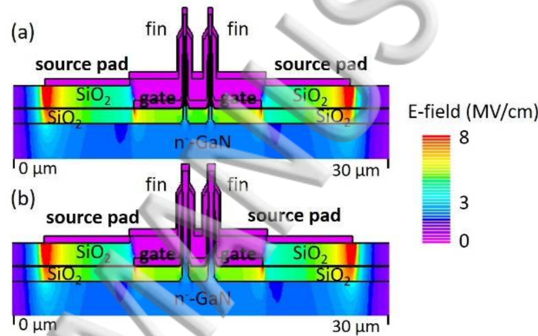


FIG. 3. Simulated E-field distribution in GaN vertical FinFETs with the fin width of (a) 200 nm and (b) 450 nm, both at $V_{DS}$=1200 V and $V_{GS}$=0 V.

Fig. 2 (a)-(d) show the representative off-state leakage curves of the FinFETs with 200 nm and 450 nm fin widths, measured at two different gate bias ($V_{GS}$) conditions: 0 V and -2 V. For each of these four conditions, at least five identical devices were measured in different wafer locations, to achieve statistically significant results. As shown in Fig. 2 (a)-(c), the leakage and breakdown behaviors were found to be almost identical in the 200-nm FinFETs at $V_{GS}$ of 0 V and -2 V and the 450-nm FinFETs at $V_{GS}$ of -2 V. Destructive breakdown was observed occurring in the spacer oxide below the edge of gate/source pads at a drain bias ($V_{DS}$) of ~1200 V. This phenomenon was validated by the fact that both gate and drain leakage suddenly shoot up at *BV*. Fig. 3 shows the simulated electric-field (E-field) distribution in the FinFETs at $V_{DS}$=1200 V and $V_{GS}$=0 V. As shown, the location of peak E-field is consistent with the observed breakdown location. Also, the simulation revealed that the location and magnitude of peak E-field is almost independent of the fin width and $V_{GS}$, which is consistent with experiment [see similar *BV* in Fig. 2 (a)-(c)]. In all these three conditions, the leakage current before

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breakdown exhibits a $\ln(I) \propto V$ relation. This indicates the dominant leakage mechanism to be the electron variable-range-hopping (VRH) through threading dislocations (TDs) under the high E-field in the drift region.[25] The slope between $\ln(I)$ and $V_{DS}$ is positively correlated to the TD density.[25] Based on an empirical model[25], the TD density in the drift region is estimated to be $10^6$~$10^7$ cm$^{-2}$ in our GaN-on-GaN wafer.

As shown in Fig. 2 (d), the leakage and breakdown behaviors are significantly different for the FinFET with 450-nm fins at $V_{GS}$ of 0 V. While the gate leakage remains low, the drain leakage $I_{DS}$ increases much faster with $V_{DS}$, until reaching the current compliance for $BV$ measurements, exhibiting a non-destructive breakdown at $V_{DS}$ of ~500 V. This indicates the leakage and breakdown are not dominated by the high E-field in the drift region and at the device edge termination, but are possibly controlled by the fin channel.

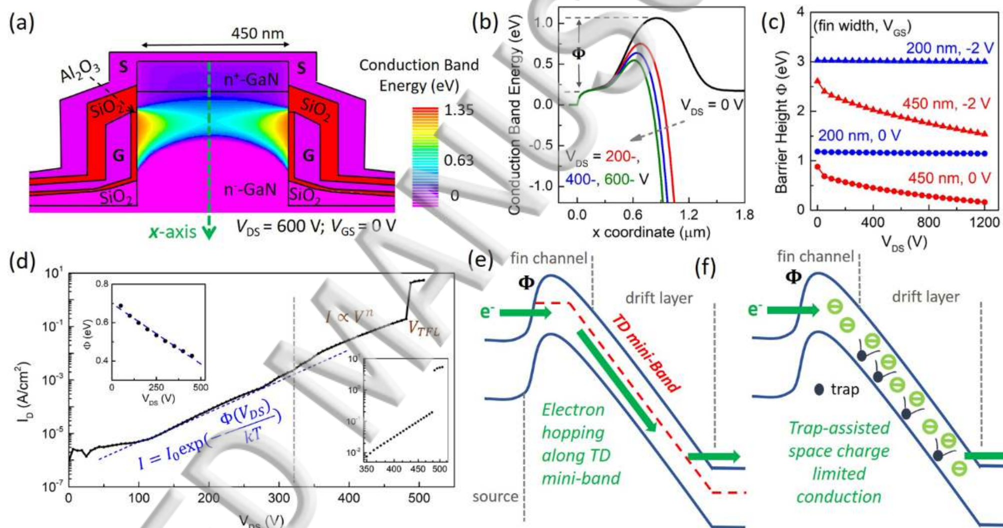


FIG. 4. (a) Simulated contour of the conduction band energy in the 450-nm fin channel, at $V_{DS}$ of 600 V and $V_{GS}$ of 0 V. Only positive energy with respect to the source is shown. (b) Simulated conduction band energy extracted from the cutline shown in (a), at different $V_{DS}$. (c) Simulated barrier heights as a function of $V_{DS}$, in 200- and 450-nm fin channels at $V_{GS}$ of 0 and -2 V, respectively. (d) Off-state *I-V* curve for 450-nm FinFETs at $V_{GS}$=0V, from experimental data and theoretical models. (inset left) linear fitting of the simulated barrier height as a function of $V_{DS}$. (inset right) *I-V* data at high $V_{DS}$ plotted in the log-log axis to illustrate the $\boldsymbol{I \propto V^n}$ relation. Physical illustration of (e) the VRH through TDs and (f) the trap-assisted space charge limited current.

The electric potential (and band energy) within the fin channel is determined by the opposite actions of $V_{GS}$ and $V_{DS}$: a zero or negative $V_{GS}$ depletes the fin channel and lift the energy band; the high positive $V_{DS}$ lowers the energy band towards the drift region. This is similar to the drain-induced barrier lowering (DIBL) effect in short-channel MOSFETs. To quantitatively study this effect, the band energies within the device structure were simulated at different off-state biases in

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Silvaco Atlas. Fig. 4 (a) shows the simulated conduction band energy in the fin channel of the 450-nm FinFET at $V_{DS}$ of 600 V and $V_{GS}$ of 0 V. As shown, the lowest energy barrier in the fin channel is along the vertical axis in the middle. Fig. 4 (b) shows the extracted conduction band energy along the vertical direction in the middle of a 450-nm-wide fin channel at different $V_{DS}$. The barrier height decreases with the increased $V_{DS}$. Fig. 4 (c) shows the simulated barrier heights for 200- and 450-nm fin channels at $V_{GS}$ of 0 V and -2 V. As shown, due to the strong gate control in 200-nm fin channels, the barrier height sees no dependence on the drain bias. In contrast, the barrier height in 450-nm fin channels is dependent on $V_{DS}$ and approaches zero at a high $V_{DS}$ and zero $V_{GS}$.

The current flowing through an energy barrier typically has an exponential dependence on the barrier height $\Phi$. As shown in Fig. 4 (c), the simulated $\Phi$ for 450-nm fin channel approximately decreases linearly with $V_{DS}$. Based on the linearly fitted $\Phi$ [see inset of Fig. 4 (d)], the calculated drain leakage current agrees well with the experimental data at the $V_{DS}$ from ~100 V to ~320 V, as shown in Fig. 4 (d). This verifies that the leakage current in the 450-nm FinFETs at $V_{GS}$ of 0 V is dominated by the energy (or potential) barrier in the fin channel.

As shown in Fig. 4 (d), the leakage current becomes higher than the exponential term when $V_{DS}$ is above ~320 V ($\Phi$ lower than ~0.5 eV). This is possibly due to the electron VRH through TDs, as the TD mini-band[25] further reduces the energy barriers for electron injection (Fig. 4 (e)). With a large amount of electrons injected into the drift region, the current then becomes limited by space charge conduction, as shown in Fig. 4 (f). This is supported by a $I \propto V^n$ relation [see inset of Fig. 4 (d)], indicating the trap-assisted space-charge-limited conduction to be the dominant leakage mechanism.[26,27] A current hump is observed at the trap-filled-limited voltage ($V_{TFL}$) (i.e. voltage at which all traps are filled),[28,29] which indicates the complete filling of traps in the drift region. Electrons further injected into the drift region will induce a large leakage current, inducing a non-destructive breakdown as the current reaches the compliance of breakdown measurement.

From the above discussion, it can be seen that the FinFET leakage current is the result of two competing mechanisms: VRH conduction in the drift region and the electron injection due to the lowered energy barrier in the fin channel. From Fig. 4 (d), the barrier-controlled leakage begins to be dominant for a $V_{DS}$ of 100 V in the 450-nm FinFETs, corresponding to a barrier height of 0.63 eV. From Fig. 4 (c), the barrier heights for the other three measurement conditions are at least 0.5 eV higher, which corresponds to around $10^8$-fold lower in current. This explains why the VRH in the drift region dominates the leakage behaviors for those three conditions.

Optimal design of power transistors requires the breakdown to be determined by the drift region and edge termination. Therefore, it is important to maintain a sufficiently high energy barrier in the fin channel at $V_{GS}$ of 0 V to prevent the punch-through at high $V_{DS}$. In the discussion above, a barrier of ~0.63 eV was extracted corresponding to the onset of fin-channel

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domination over the leakage current. Interestingly, as revealed by simulation, the barrier height corresponding to the onset of subthreshold current increase in log-scale transfer characteristics [see Fig. 1(e)] is also ~0.6 eV. This indicates that this barrier height can be considered as a critical value for normally-off GaN FinFETs, although slightly higher barriers (e.g. 0.7~0.8 eV) may be preferred in the device design to ensure the robust normally-off operation.

Finally, the well-calibrated simulation was used to quantify the dependence of the fin-channel barrier height on fin geometries and interface charges. Vertical GaN power FinFETs with different fin widths, gate lengths and oxide/GaN interface charges were simulated at $V_{DS}$ of 1200 V and $V_{GS}$ of 0 V. The fin-channel barrier height was then extracted in each simulated device, as plotted in Fig. 5(a) and (b). As shown, a smaller fin width and longer gate could increase the energy barrier as they strengthens the gate control over the electrostatics in the fin channel. The removal or reduction of $Q_{ox}$ could also effectively lift the energy barrier, as the $Q_{ox}$ shields the gate from the electrostatic control over the fin channel. As an example, the barrier height can be lifted to be above 0.7 eV in the FinFETs with a $Q_{ox}$ of $10^{12}$ cm$^{-2}$, either by shrinking the fin width to below 300 nm (while keeping the 750 nm gate length) or increasing the gate length to beyond 1 μm (while keeping the 450 nm fin width).

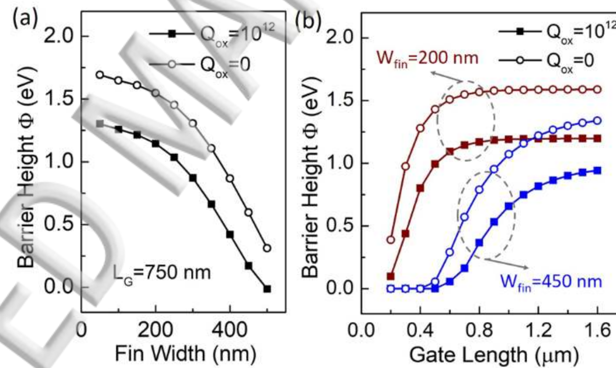


FIG. 5. Simulated channel energy barrier in the FinFETs with (a) different fin widths from 50 nm to 500 nm (for 750 nm gate length) and (b) different gate lengths from 0.2 μm to 1.6 μm (for two fin widths 200 nm and 450 nm), with and without oxide/GaN charges $Q_{ox}$, all at $V_{DS}$=1200 V and $V_{GS}$=0 V.

In summary, this work unveils two distinct leakage and breakdown mechanisms in GaN vertical power FinFETs. We believe that these two competing mechanisms are also important for the understanding and design of other junctionless power transistors, such as static induction transistors, metal-semiconductor FETs, etc., based on GaN and other materials, such as $Ga_2O_3$. For example, device punch-thorough was also observed in β-$Ga_2O_3$ power FinFETs due to the DIBL effect in the fin channel,[7,30] although the quantitative models may be different. Two general implications can be obtained in this work for



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vertical junctionless power transistors: (a) $V_{th}$>0 is not a sufficient criterion for normally-off operation; the device should also be able to sustain the high $V_{DS}$ at $V_{GS}$=0 V; (b) it is crucial to maintain a sufficiently high energy barrier in the channel at high $V_{DS}$; this should be carefully considered in the device design.


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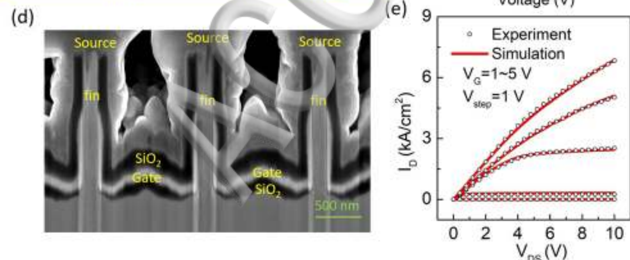
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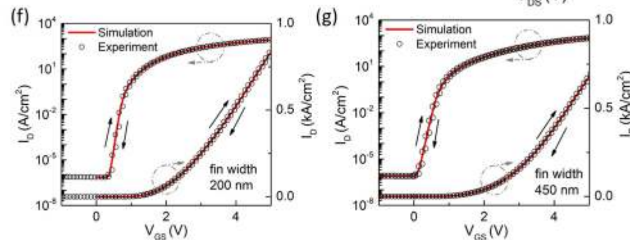
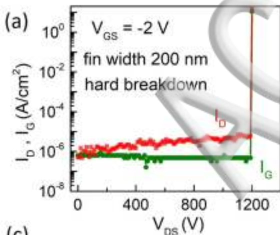
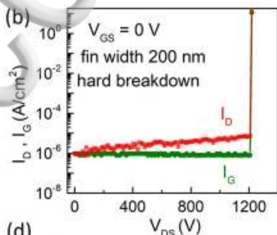
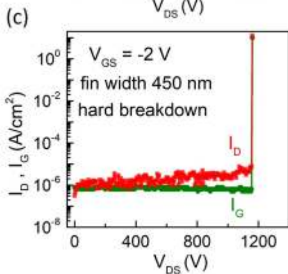
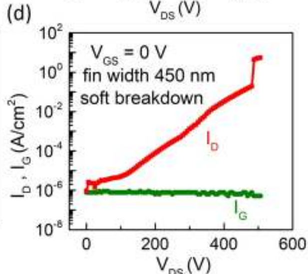
Ar
n−-GaN drift layer
n+-GaN substrate
drain
(b)
Ltermination
anode
SiO2
Ar
Ar
n−-GaN
n+-GaN sub
cathode
(c)
w/o implant
termination
Current (A)
Ltermination=15-,
30-, 50 μm
Voltage (V)
(d)
Source
Source
Source
fin
fin
fin
SiO2
Gate
Gate
SiO2
500 nm
(e)
Experiment
Simulation
VG=1~5 V
Vstep=1 V
ID (kA/cm2)
VDS (V)

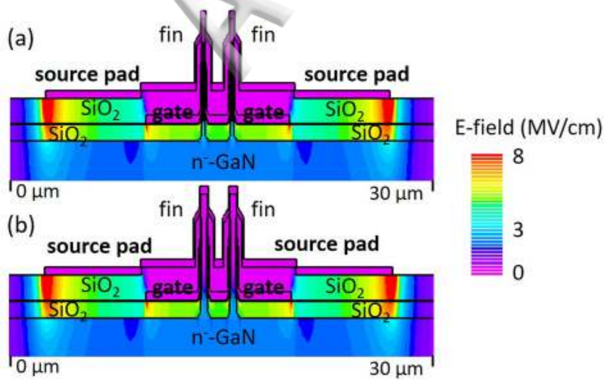

(f)
Simulation
Experiment
ID (A/cm2)
ID (kA/cm2)
fin width
200 nm
VGS (V)
(g)
Simulation
Experiment
ID (A/cm2)
ID (kA/cm2)
fin width
450 nm
VGS (V)

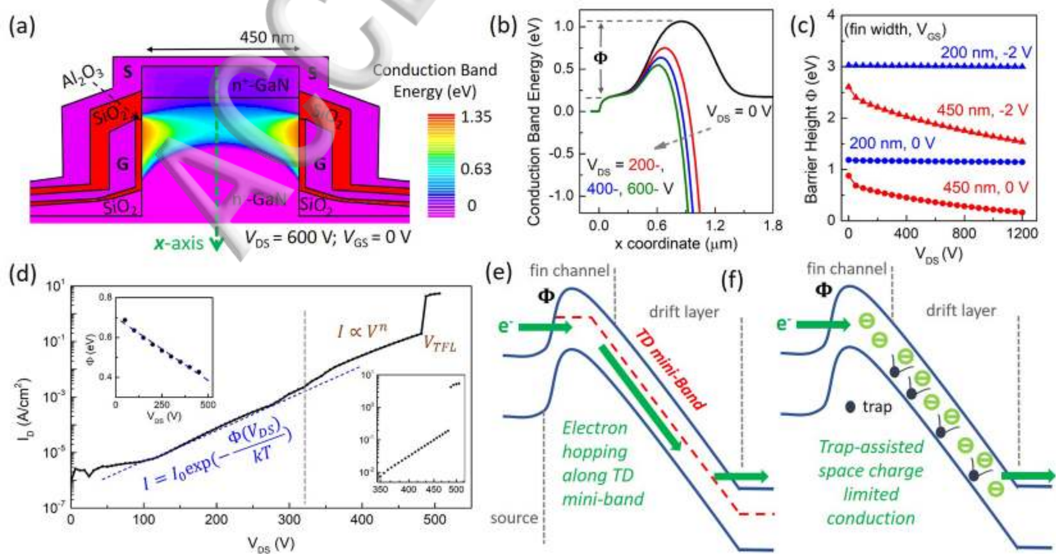

(a)
V_GS = -2 V
fin width 200 nm
hard breakdown
I_D
I_G
I_D , I_G (A/cm^2)
V_DS (V)


(b)
V_GS = 0 V
fin width 200 nm
hard breakdown
I_D
I_G
I_D , I_G (A/cm^2)
V_DS (V)


(c)
V_GS = -2 V
fin width 450 nm
hard breakdown
I_D
I_G
I_D , I_G (A/cm^2)
V_DS (V)


(d)
V_GS = 0 V
fin width 450 nm
soft breakdown
I_D
I_G
I_D , I_G (A/cm^2)
V_DS (V)


(a)
fin
fin
source pad
source pad
SiO$_2$
gate
gate
SiO$_2$
SiO$_2$
SiO$_2$
n$^-$-GaN
0 μm
30 μm
(b)
fin
fin
source pad
source pad
SiO$_2$
gate
gate
SiO$_2$
SiO$_2$
SiO$_2$
n$^-$-GaN
0 μm
30 μm
E-field (MV/cm)
8
3
0


(a)
450 nm
$Al_2O_3$
S
S
$n^+$-GaN
$SiO_2$
$SiO_2$
G
G
n⁻-GaN
$SiO_2$
$SiO_2$
Conduction Band Energy (eV)
1.35
0.63
0
x-axis
$V_{DS}$ = 600 V; $V_{GS}$ = 0 V
(b)
Conduction Band Energy (eV)
Φ
$V_{DS}$ = 0 V
$V_{DS}$ = 200-, 400-, 600- V
x coordinate (μm)
(c)
(fin width, $V_{GS}$)
200 nm, -2 V
450 nm, -2 V
200 nm, 0 V
450 nm, 0 V
Barrier Height Φ (eV)
$V_{DS}$ (V)
(d)
$I_D$ (A/cm²)
$V_{DS}$ (V)
$I \propto V^n$
$V_{TFL}$
$I = I_0 \exp(-\frac{\Phi(V_{DS})}{kT})$
Φ (eV)
$V_{DS}$ (V)
(e)
fin channel
Φ
drift layer
e⁻
TD mini-Band
Electron hopping along TD mini-band
source
(f)
fin channel
Φ
drift layer
e⁻
trap
Trap-assisted space charge limited conduction

(a)

$Q_{ox}=10^{12}$

$Q_{ox}=0$

$L_G$=750 nm

Barrier Height Φ (eV)

Fin Width (nm)

(b)

$Q_{ox}=10^{12}$

$Q_{ox}=0$

$W_{fin}$=200 nm

$W_{fin}$=450 nm

Barrier Height Φ (eV)

Gate Length (μm)

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