Leakage and Leakage Sensitivity Computation for Combinational Circuits

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ABSTRACT

Leakage power is emerging as a new critical challenge in the design of high performance integrated circuits. Leakage is increasing dramatically with each technology generation and is expected to dominate system power. This paper describes a static (i.e input independent) technique for efficient and accurate leakage estimation. A probabilistic technique is presented to compute the average leakage of combinational circuits. The proposed technique gives accurate results with an average error of only 2% for the ISCAS benchmarks and accurately predict both subthreshold and gate leakage as well as the leakage sensitivities to process and environmental parameters.

Categories and Subject Descriptors

[I.6.5] [**Simulation and Modeling**]: Model Development.

General Terms

Algorithms, Performance, Verification.

Keywords

Leakage power, Iddq analysis, power estimation, sensitivity.

1. INTRODUCTION

Technology scaling is causing a drastic increase in subthreshold and gate leakage [2]. Leakage power accounts for about 10-20% of the total chip power in current technologies, and is already significantly important for the standby operation for low-power devices. With new technologies, threshold voltage and gate oxide scaling are causing leakage to dominate the total chip power. Leakage is emerging as one of the key variables in the design process along with timing, noise and dynamic power. Accurate and efficient estimation of leakage is required for both power estimation and circuit optimization.

Early work on leakage estimation mainly focused on subthreshold leakage and the dependence of leakage on the state (input) of the circuit. Typically, CMOS circuits were macromodeled by transistor stacks for which leakage is computed using analytical expressions. In [4][7], simple analytical expressions are derived for the leakage current of a transistor stack. A statistical approach to discover low leakage patterns was presented in [8]. For full-chip total leakage power estimation, regression models based on gate and transistor counts are presented in [9]. However, the accuracy of simple regression models are generally difficult to control. Furthermore, this technique ignores the dependence of leakage on circuit topology. A more accurate approach [6] estimates total leakage power after an effective stacking approximation. However, even in this model circuit functionality is not considered. More recently, [5] described an estimation method based on the concept of dominant leakage states. By ignoring low leakage states, the authors proposed a graph-based approach. The leakages of connected partitions are estimated via DC analysis using Newton-Raphson iterations.

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Circuit	*# cells*	*# inputs*	I_{max}*(mA)*	I_{min} *(mA)*	*cv.*
c432	187	36	0.073899	0.0597	0.0237
c499	222	41	0.21463	0.153863	0.0337
c880	383	60	0.132035	0.095789	0.0335
c1355	566	41	0.173451	0.127854	0.0301
c1908	996	33	0.312824	0.210898	0.0610
c2670	1255	233	0.427436	0.325011	0.0363
c5311	2485	178	0.842406	0.670118	0.0279
c7752	3692	270	0.713998	0.665011	0.0483

Table 1. The dependency of leakage currents on input vectors (cv=coefficient of variation=std. deviation/mean)

Leakage has been predicted either by detailed input-dependent analysis or by higher-level models based on total transistor width or gate count. There is a need for more efficient but accurate leakage power estimation for proper design and optimization. Hence, we propose an efficient *static* (input-independent) analysis technique for leakage estimation. We do want to mention that *dynamic* (input-dependent) techniques may be needed in evaluating special circuit topologies for leakage mitigation, however for most common combinational circuits, static methods are highly applicable.

Leakage current depends on key circuit variables such as input vectors, device characteristics (threshold voltage, gate oxide thickness, channel length) and operating conditions (VDD and temperature). Let us first investigate the input dependence of leakage for a basic logic gate in a leading process technology. We have observed that for a 3-input nand gate for the pattern (111) creates 10 times more leakage than the pattern (000). However, as the size of combinational circuit increases, input dependence becomes weaker. This is mainly due to an averaging effect that balances high and low leakage states. To illustrate this, we computed total leakage for the ISCAS circuits. The circuits are synthesized with a typical gate library satisfying specified delay targets. The results are given in Table 1. For each benchmark circuit, the extreme statistics and coefficient of variation (standard deviation/mean) of leakage currents with 10000 random input patterns are reported. From the table, we see that total leakage varies by about 15% with the input applied to the circuit. For larger size circuits, a similar trend is observed.

Leakage dependency on input may still be significant, but we believe it is much less than the effect of environmental variables (Vdd, temperature) and process variations. The impact of process variations on leakage is summarized in Figure 1. This figure shows how leakage varies with different process conditions. A normalized process parameter (Z) is used to model the process conditions between the "fast" and "slow" corners. Z=0.5

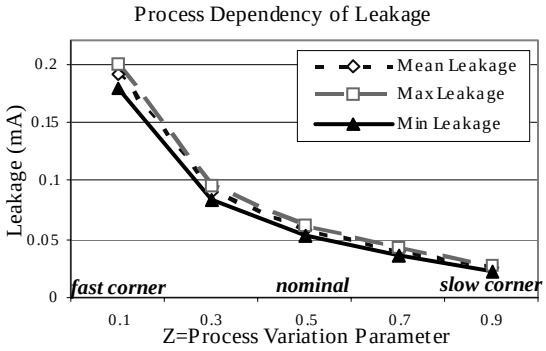


Figure 1. Impact of process variations on leakage for c432. To display input-patter dependency, min and max leakage observed from 10000 input patterns are also plotted.

represents the nominal conditions. At each process point, the variation of leakage due to input vectors is also shown by the maximum, average and minimum leakage obtained for a large sample of inputs. We see that leakage varies much more with the process parameter than with input variations. Similarly leakage is more affected by temperature and power supply voltage (VDD) compared to the impact of input vectors.

In light of these observations, we can say that while the input dependence remains important and needs to be captured for standby mode, the dependence on process parameters, temperature and VDD is far more important. Therefore, a static method is desired to account for average leakage power for all possible input patterns. In this paper, we extend our estimation method to compute leakage sensitivity to environmental and process parameters. Leakage sensitivities can be very instrumental in design optimization and planning. With little additional effort, the sensitivities of average leakage with respect to a designated parameter can be computed along with the leakage estimate. The efficacy of the proposed methods will be important for future technologies. We assume that other elements of an integrated circuit, such as caches, registers and latches can be modeled directly because they are more regularly structured and hence easier to pre-characterize.

The remaining part of the paper is organized as follows. Section 2 describes the proposed static leakage estimation technique. Experimental results are presented in Section 3. Section 4 describes the method for estimating the leakage sensitivity and we present some results in Section 5.

2. STATIC LEAKAGE ESTIMATION

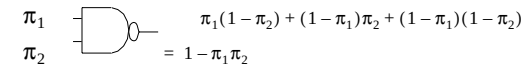
2.1 Background

Combinational logic circuits are generally partitioned into smaller cells, in the form of gates, channel-connected regions or other primitive structures. The node variables at the cell boundaries are assumed to hold full logic values (VDD or 0). Total leakage power dissipation is basically the sum of the leakage dissipated in each cell. Let us assume that the leakage power for each cell is pre-characterized for all circuit input states. This can be done via accurate circuit simulation during library generation. Let us denote by $L_i(x_i)$ the leakage power for cell i for input vector x_i; the total leakage power for a given input vector will be:

$$L_{tot} = \sum_i L_i(x_i) \qquad (1)$$

Note that the current state of the circuit, i.e. the inputs for each cell, will depend on the connectivity in the circuit.

We now introduce the concept of occurrence probabilities to compute the average leakage power. Previous probabilistic approaches were reported in [3][10][11] but were applied for switching power estimation. Leakage, however is delay-independent and hence *more suitable* for a probabilistic approach.



State	*Gate Leakage*	*Subthres. Leakage*	*Total Leakage*	*State Occur. Prob.*
00	G_{00}	S_{00}	$L_{00}=G_{00}+S_{00}$	$(1-\pi_1)(1-\pi_2)$
01	G_{01}	S_{01}	$L_{01}=G_{01}+S_{01}$	$(1-\pi_1)\pi_2$
10	G_{10}	S_{10}	$L_{10}=G_{10}+S_{10}$	$\pi_1(1-\pi_2)$
11	G_{11}	S_{11}	$L_{11}=G_{11}+S_{11}$	$\pi_1\pi_2$

Figure 2. Calculating output node occurrence probability with independence assumption and the table of pre-characterized leakage components for a 2-input nand gate.

Node Occurrence Probability: Let us assume that node *n* is either a primary input or an output of a particular cell, and holds a full logic value. We define the *node occurrence probability* of *n* as the likelihood of observing the node *n* at logic value 1: $\pi_n = Pr(n = 1)$. Hence, the probability of observing *n* at 0 would be $1 - \pi_n$.

State Occurrence Probability: We define the state occurrence probability $\Pi_i(x)$, as the probability of observing the cell *i* at the state uniquely imposed by input *x*. State occurrence probability can be referred to as the joint probability of the input nodes of cell *i*. If the cell inputs are independent, computation of $\Pi_i(x)$ is simply the multiplication of the associated node occurrence probabilities. An example is given in Figure 2 for a 2-input nand gate.

Average Leakage Power: The true probabilistic mean of the total leakage power $\mu_{L_{tot}}$ is the weighted sum of the leakage for all cells in each state. The weights are the state occurrence probabilities:

$$\mu_{L_{tot}} = \sum_i \mu_{L_i(x_i)} = \sum_i \sum_{x_i} \Pi_i(x_i) L_i(x_i) \qquad (2)$$

Note that $L_i(x_i)$'s are available for each cell from library pre-characterization. Hence, the exact computation of (2) requires the true state occurrence probabilities, $\Pi_i(x_i)$, for each cell and state. However, the exact computation for $\Pi_i(x_i)$ for combinational circuits is shown to be a NP-hard problem [13].

2.2 Static Probabilistic (SP) Method

We propose a practical approach to predict the state occurrence probabilities using circuit and input information. Like [3], we will ignore spatial dependencies within the circuit for the sake of simplicity and efficiency. The results will later demonstrate that spatial dependencies do not contribute greatly, since the estimates are already very accurate. Furthermore, this approach can exploit input probabilities if they are specified.

Consider the cell *C* with an input vector $x = x_1 x_2 \ldots x_n$ and the output node *o*. Under the spatial independence assumption, the node occurrence probability for *o* will be:

$$\pi_o = Pr(x_1, x_2 \ldots | st \;\; O(x) = 1) = \sum_{o_i \in m(o)} Pr(x = o_i) \qquad (3)$$

where *O(x)* represents the logic function and *m(o)* is the set of minterms for *o* in terms of inputs x_i. With the independence assumption, the state occurrence probability for *C* becomes the multiplication of node occurrence probabilities of all its inputs: $\Pi_i(x) = \Pi_i(x_1 x_2 \ldots x_n) = \pi_{x_1} \pi_{x_2} \ldots \pi_{x_n}$. Moreover, once the state occurrence probabilities are computed, they can be separately used for calculations involving the leakage components (i.e. gate and subthreshold) which exist in the library.

Circuit	*Ave. Leakage (W)*	*SP Method (W)*	*Rel. Error (%)*
c432	0.06599	0.06800	3.056
c499	0.17885	0.17786	-0.556
c880	0.10857	0.10927	0.643
c1355	0.13828	0.14236	2.950
c1908	0.22508	0.21437	-4.758
c2670	0.34197	0.34638	1.290
c5315	0.70782	0.71171	0.549
c7552	0.99772	0.97618	-2.158

Table 2. Average leakage power estimates with SP method.

Based on the estimates of $\hat{\Pi}_i(x_i)$ under the spatial independence assumption, the Static Probabilistic (SP) method estimates the average leakage power as:

$$\hat{\mu}_{SP,L_{tot}} = \sum_i \sum_{x_i} \hat{\Pi}_i(x_i) L_i(x_i) . \quad (4)$$

The spatial independence assumption guarantees that node and state occurrence probabilities can be computed simultaneously via a level-order traversal of the circuit in linear time. Hence, its runtime complexity grows with the depth of the circuit and the number of cell inputs. In comparison to switching probability, the described approach can easily solve circuits with feedback. But the effects of reconvergent fanout or existing primary input correlation will be ignored by the spatial independence assumption.

The SP method can be also used to estimate the variance of the leakage power of a combinational circuit. The estimate for the variance of the total leakage, $\sigma^2_{L_{tot}}$, would be the sum of each cell's leakage variance:

$$\hat{\sigma}^2_{SP,L_{tot}} = \sum_i \sum_{x_i} \left\{ \hat{\Pi}_i(x_i) L_i^2(x_i) - \left(\sum_{x_i} \hat{\Pi}_i(x_i) L_i(x_i) \right)^2 \right\} . \quad (5)$$

The variance estimate predicts the amount of variability of leakage due to input variations, and can be used as an indicator of input dependencies. In an complete analysis framework, this may trigger a dynamic estimation of a particular circuit that display significant input dependency (large variance).

The SP method provides an added accuracy in leakage power estimation over simple device-count based methods, since it exploits more information of the circuit including topology and connectivity. If better accuracy is desired, sophisticated methods [11][12][13] can be implemented to account for spatial correlations. But this may significantly increase the overall runtime complexity and is observed as unneeded.

3. LEAKAGE ESTIMATION RESULTS

The combinational ISCAS circuits were synthesized using a library of basic gates with delay constraints in a state-of-art process technology. The total leakage of each circuit for a given input vector is obtained via SPICE. For each circuit, we evaluated a sample of 10000 randomly generated input vectors. Primary inputs are assumed to have binary occurrence probability of 0.5. The average leakage is computed simply by taking the arithmetic mean. We observed that 10000 samples are sufficient for an accurate estimation.Then, we ran a small C-program that calculates the SP estimate for average leakage. Table 2 shows the results obtained with the SP method. Note the excellent agreement between the actual results and SP estimates, as the average relative error is about 2%. For these circuits, the SP estimate is calculated many orders of magnitude faster than running SPICE with even a single input vector. This illustrates the computational advantages of using the static approach in leakage estimation.

In previous section, we mentioned that the SP method can be used to predict different leakage components. Figure 3 shows gate and subthreshold leakage power estimates separately. The figure shows

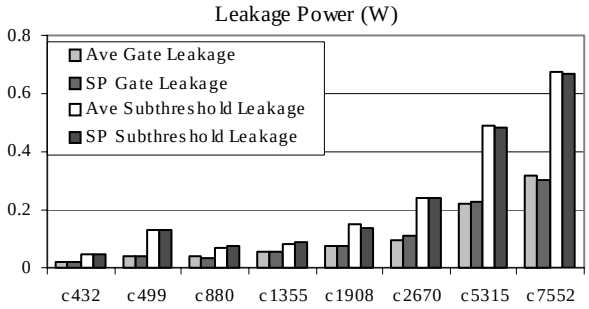


Figure 3. Estimation for leakage power components.

that the SP method can provide reasonably accurate and efficient estimates for critical leakage components.

To illustrate the handling given input probabilities by the SP method, we varied the node occurrence probability for the first four inputs of c1908 from 0.1 to 0.9 with 0.1 increments. Other inputs have an occurrence probability of 0.5. With this setting, we generated 10000 random input samples and calculated the average leakage using circuit simulation. The relative error of the SP estimate is well bounded by 5% at each datapoint. The special handling of the input probabilities is more useful when the occurence probabilities of a circuit (or a macro) are obtained from a higher-level analysis and simulation tool, possibly from a behavioral or architectural level analysis.

4. LEAKAGE SENSITIVITY

Leakage analysis must explore dependencies on key model parameters. One approach to assess the leakage dependency on a particular process/environmental parameter, *p*, is to estimate the average leakage at different *p*'s. This requires the design components (gates) to be pre-characterized for all *p*'s and leakage estimates to be calculated using different tables. An alternative for modeling the parametric dependency is estimating the sensitivity of average leakage with respect to *p*.

We assume that the leakage sensitivities for a gate at each input, i.e. $dL_i(x_i)/dp$'s, are obtained in pre-characterization. Moreover, we assume that the variation in *p* does not change the logical state of the circuit. This assumption is fairly valid due to the assumed robustness of logic functionality with respect to process/environmental conditions. This would imply that state occurrence probabilities are independent of *p*. Therefore, the estimate for the n^{th} order leakage sensitivity to *p* can be written in the same manner as the nominal estimate (4) as:

$$\frac{d^n \hat{\mu}_{SP,L_{tot}}}{dp^n} = \sum_i \sum_{x_i} \hat{\Pi}_i(x_i) \frac{d^n L_i(x_i)}{dp^n} \quad n=1,2... \quad (6)$$

The sensitivities to process and environmental parameters are essential for making realistic design decisions and optimization.

5. SENSITIVITY ESTIMATION RESULTS

We investigated the leakage dependency of the ISCAS circuits on *Z*, a standardized parameter that represents process conditions. (see Figure 1). We calculated the leakage sensitivites of ISCAS circuits at different *Z* values using a SPICE-like simulator. We also pre-characterized the leakage of the library elements (i.e. gates) at each input pattern and process conditions. The leakage sensitivities to *Z* for each gate and pattern were also pre-characterized.

Figure 4 shows the first order leakage sensitivities to *Z* for the ISCAS circuits, estimated both with the SP method and obtained from simulation results using 10000 random inputs (noted as MC). The SP estimates agree well with the simulation results. In Table 3, the SP estimates for the first and second order sensitivities at the nominal process condition and relative estimation errors are

Circuit	$d\hat{\mu}_{SP,L_{tot}}/dZ$			$d^2\hat{\mu}_{SP,L_{tot}}/dZ^2$		
	Actual	*SP*	*relerr.(%)*	*Actual*	*SP*	*relerr.(%)*
c432	-9.40e-2	-9.32e-2	-0.68	2.43e-1	2.42e-1	-0.28
c499	-6.85e-2	-6.59e-2	-3.76	1.78e-1	1.72e-1	-3.12
c880	-2.74e-1	-2.74e-1	0.05	7.33e-1	7.33e-1	0.07
c1355	-3.59e-1	-3.48e-1	-2.9	9.56e-1	9.19e-1	-3.86
c1908	-5.29e-1	-5.30e-1	0.22	1.42e0	1.42e0	0.00
c2670	-8.75e-1	-8.81e-1	0.68	2.37e0	2.37e0	0.33
c5315	-1.76e0	-1.78e0	1.16	4.74e0	4.79e0	0.88
c7552	-2.49e0	-2.48e0	-0.28	6.73e0	6.71e0	-0.27

Table 3. Sensitivities of average leakage power to *Z* at nominal process conditions (Z=0.5).

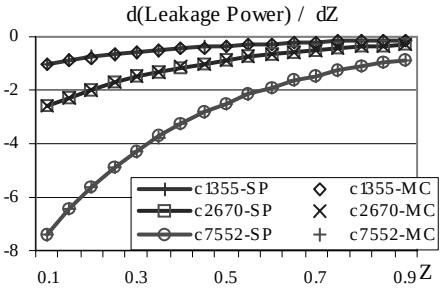


Figure 4. The sensitivity of average leakage to Z. MC refers to simulation results, SP for the proposed estimate

also given. The results show that the SP method captures the sensitivities very accurately and can be calculated after the state occurence probability calculation. Similarly, one can perform similar analyses for sensitivities to threshold voltage, oxide thickness and VDD.

The leakage sensitivities are instrumental in optimizing and controlling the leakage, in yield calculations and in statistical analysis steps for leakage power. It may be also useful to approximate the parametric dependencies of leakage. This would obviate the need for pre-characterization of the gate library and estimating average leakage for these *Z* values. Hence, the leakage estimation process will be shortened. These emprical models and the use of sensitivities reduce the characterization effort at many sample points, and give important intuition on the parametric dependencies of average leakage.

At last, we compare our results with an effective-width based approach for leakage and sensitivity estimation. Figure 5 shows the scatter plots of the relative error of estimates for ISCAS circuits, displaying the important added accuracy of the SP method as compared to the simple effective width-based methods. From the figure, the relative errors made by the SP method remain at only a few percents, whereas the effective-width based methods result in far greater errors especially for the sensitivity estimation.

6. CONCLUSIONS

Input-independent leakage estimation techniques are presented in this paper. We demonstrated that the input dependency of the leakage is less important than dependencies on process and environmental parameters. The proposed method uses a probabilistic method to estimate the average leakage of a combinational circuit, its components and also its sensitivities to process and environmental parameters. The efficient and accurate estimation of leakage and its sensitivities will be crucial in developing future power-aware design methodologies.

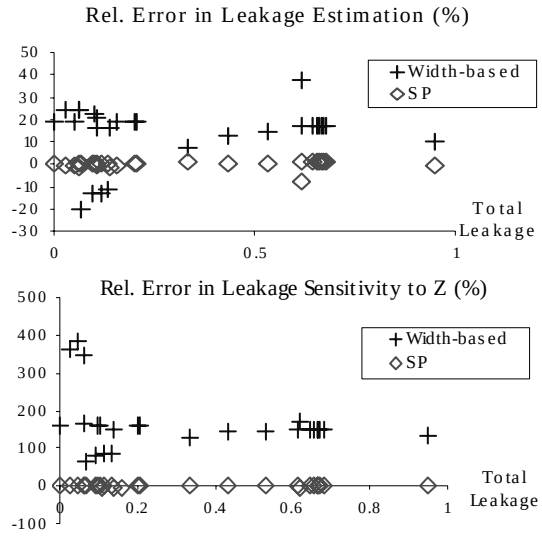


Figure 5. Comparisons with effective width based methods showing the added accuracy of SP method by exploiting circuit topology

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