Leakage Current Modeling of Test Structures for Characterization of Dark Current in CMOS Image Sensors

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Abstract—**In this paper, we present an extensive study of leakage current mechanisms in diodes to model the dark current of various pixel architectures for active pixel CMOS image sensors. Dedicated test structures made in 0.35-μm CMOS have been investigated to determine the various contributions to the leakage current. Three pixel variants with different photo diodes—n$^+$/pwell, n$^+$/nwell/p-substrate and p$^+$/nwell/p-substrate—are described. We found that the main part of the total dark current is coming from the depletion of the photodiode edge at the surface. Furthermore, the source of the reset transistor contributes seriously to the total leakage current of a pixel. From the investigation of reverse current–voltage (I–V) characteristics, temperature dependencies of leakage current, and device simulations we found that for a wide depletion, such as n-well/p-well, thermal Shockley–Read–Hall generation is the main leakage mechanism, while for a junction with higher dope concentrations, such as n$^+$/p-well or p$^+$/n-well, tunneling and impact ionization are the dominant mechanisms.**

Index Terms—**Image sensors, leakage currents, modeling.**

I. Introduction

DARK current is an important parameter to characterize the performance of an image sensor. Lowering the dark current will improve the dynamic range due to a reduction of the shot noise of the dark current. Furthermore, dark current reduction is correlated with a decrease of the fixed pattern noise and a reduction of the amount of white pixels defects in dark. Therefore, the reduction of dark current has been an important subject in the history of solid-state imagers. The main part of the work that has been reported by our department about this subject is related to dark current reduction in CCDs [1]–[4]. Nowadays, we use this knowledge to improve the technology and pixel architecture of image sensors made in Philips' 0.35-μm CMOS imaging process. To optimize the performance of an active CMOS image pixel, its architecture and photo diode structure have to be optimized [5]–[7].

Manuscript received April 18, 2002; revised November 5, 2002. The review of this paper was arranged by Editor E. Fossum.

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Digital Object Identifier 10.1109/TED.2002.807249

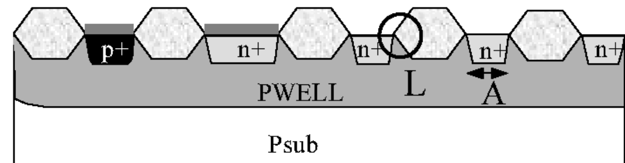

Fig. 1. Cross section of an n+/p-well test structure. L and A indicate where length- and area-dependent contributions are located, respectively.

To get a good insight into the mechanisms of dark current generation and the location in the pixel where the leakage current is generated, we have investigated dedicated test structures. First, we have determined the leakage current per surface junction length (A/μm) and the contribution of the area part (A/μm^2) for various diodes. Using these contributions, we model the leakage current of different pixel architectures and compare the calculated values with dark current measurements of pixel matrix test structures with pixels of 5.6 $\times$ 5.6 μm^2. Next, we describe the different dark current mechanisms on the basis of measured and simulated reverse current–voltage (I–V) characteristics of n$^+$/n-well/psb, p$^+$/n-well, and n$^+$/p-well diodes. Also, the temperature dependence of the leakage current has been used to distinguish the different mechanisms. Using the reverse voltage dependencies of the various junctions and the leakage generation mechanisms, we are able to analyze the dark current behavior of the various pixel architectures in detail.

II. Dark Current Modeling Based on Diode Measurements

Various dedicated diode structures have been designed and processed in Philips' 0.35-μm CMOS baseline process in order to determine the leakage current of different diodes, such as n$^+$/p-well, n$^+$/n-well/psb and p$^+$/n-well/psb. A schematic drawing of a cross section of an n$^+$/p-well test structure is shown in Fig. 1. The LOCOS regions have been designed as stripes in active region, so all n$^+$ areas are connected to each other.

The total leakage current of a diode is assumed to be the sum of three components: the length-dependent leakage from the p-n junction at the surface (mainly in the area where depletion comes to the surface), the area-dependent leakage current generated in the depletion in the bulk, and a contribution which does not depend on either area or surface, for example, the contact area. Using this simple model, the leakage current per sur-

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TABLE I
LEAKAGE CURRENT PER AREA AND LENGTH FOR THREE DIFFERENT DIODE STRUCTURES

	J_1 (*10^{-16} A/μm²)	J_2 (*10^{-16} A/μm)
n^+/pwell/psb	0.22	2.1
n^+/nwell/psb	0.20	1.5 (nwell/pwell junction)
p^+/nwell/psb	0.09	0.03 (1.9, junction not screened)

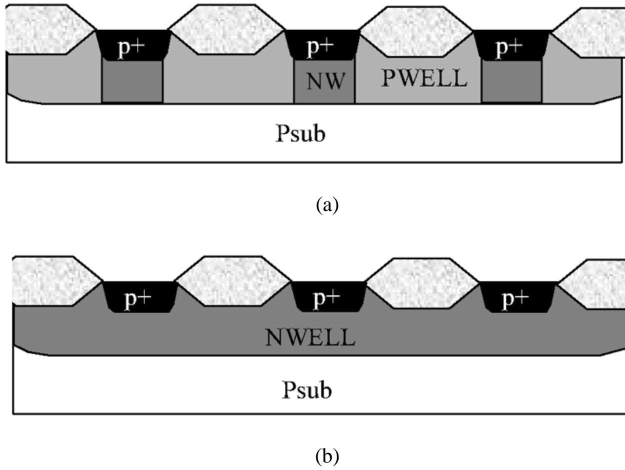

Fig. 2. Schematic drawing of p+/n-well/psb diode where (a) the depletion of the junction is screened from the surface by the p+ layer that is connected to the p-well and (b) the junction at the surface is not screened and causes a length-dependent contribution to the leakage current.

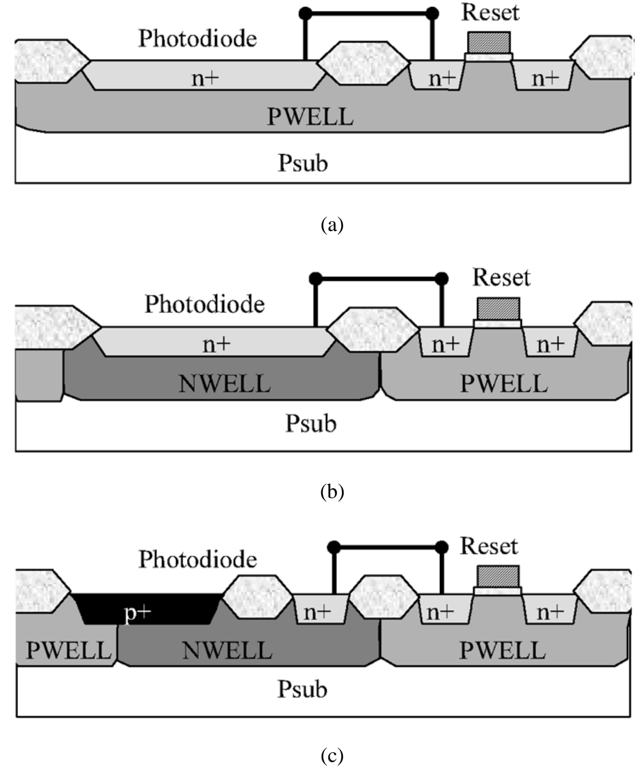

Fig. 3. Cross section of (a) n+/p-well/psb pixel architecture, (b) n+/n-well/psb pixel architecture, and (c) p+/n-well/psb pixel architecture.

face junction length (A/μm) and the contribution of the area part (A/μm^2) of the diode can be determined from the measured reverse current of three structures with different ratios between the area and the length.

The general equation that is used in the calculation can be written as follows:

$$I = J_1 \cdot A + J_2 \cdot L + I_3 \quad (1)$$

where I is the measured leakage current, J_1 is the current density (A/μm^2) generated in the bulk, A is the area of the junction in the bulk, J_2 is the current per μm generated at the surface, L is the length of the depletion at the surface, and I_3 is a current offset. For the diode structures under study, the current offset $I3$ is negligible since the contact area is a p+/p-well junction or a p+/psub junction (see Fig. 1). By solving the equations with two unknowns using the three different area/length ratios, we have determined J_1 and J_2 for the three diodes: n^+/p-well, n^+/n-well/psb, and p^+/n-well/psb. In the pinned diode p^+/n-well/psb, the length-dependent leakage is negligible if the depletion of the junction is screened from the surface by the p^+ layer [Fig. 2(a)]. In the situation depicted in Fig. 2(b), the p^+/n-well junction at the surface causes a length-dependent contribution to the leakage current. The leakage currents of the different diodes have been measured at 60 °C for 2.2-V reverse voltage. The obtained area- and length-dependent contributions are presented in Table I.

Using these values for leakage current per area and length of the various junctions, we can model the leakage current of different pixel architectures. To validate this model, we have made test structures with pixel arrays of 13 × 231 pixels with a pixel size of 5.6 × 5.6 μm^2, using a basic three-transistor configuration [5]. All photodiodes are connected in parallel, so the total leakage current of the pixel matrix can be measured. Schematic drawings of the cross sections of three different pixel architectures are shown in Fig. 3. We have measured the leakage current a at 2.2-V reverse bias at 60 °C.

For these pixel architectures, we have calculated the dark current using the contributions as tabulated in Table I. The length of the p-n junction at the surface (photodiode edge) was multiplied by the contribution J_2. The area of the p-n junction (photodiode area) was multiplied by the contribution J_1. The sum gives the calculated leakage current of the photodiode. In addition to this contribution from the photodiode, the area and length contributions of the source of the reset transistor are taken into account. For all pixel matrix test structures, the source area is an n^+/p-well junction.

Fig. 4 shows the calculated leakage currents compared with the measured leakage currents. The calculated leakage currents match very well with the measured data, which validates the model. In Table II, the calculated contributions are tabulated. The main part of the leakage current is generated by the edge of the photodiode at the surface. In the n^+/n-well/psb diode,

TABLE II
CALCULATED LEAKAGE CURRENT CONTRIBUTIONS FOR THREE DIFFERENT PIXEL MATRIX STRUCTURES

	Edge of the photodiode	Bulk of the photodiode	Reset transistor source
n^+/pwell/psb	7.0 pA	0.7 pA	1.6 pA
n^+/nwell/psb	4.4 pA	0.3 pA	1.6 pA
p^+/nwell/psb	4.0 pA	0.1 pA	1.6 pA

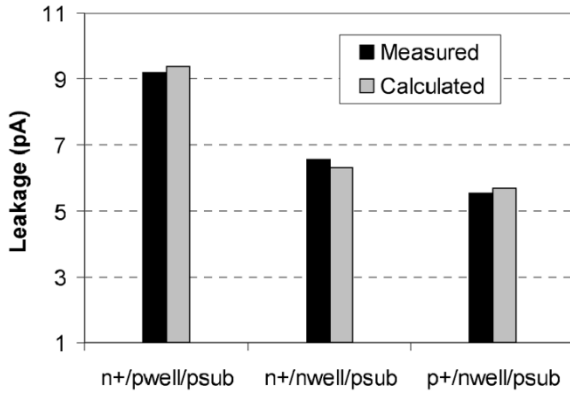

Fig. 4. Measured and calculated leakage current for three different pixel matrix structures with a 2.2-V reverse voltage at 60 °C.

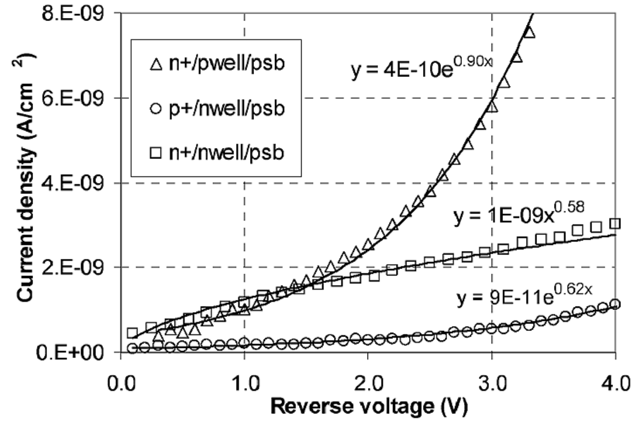

Fig. 5. Measured reverse I–V characteristics for n+/n-well/psb, p+/n-well/psb, and n+/p-well/psb together with fitted functions.

70% of the leakage current was caused by the depletion of the photodiode at the surface (n-well/p-well junction) and only 5% was generated by the depletion in the bulk. The source area of the reset transistor, an n^+/p-well region, generates around 25%. For the n^+/p-well pixel, the results are similar: around 75% is generated by the depletion region of the photodiode at the surface, 8% by the depletion in the bulk and 17% by the reset transistor. In the pinned pixel [Fig. 3(c)], the depletion is only partly screened from the surface by the p+ layer, because the contact of the n-well requires a p^+/n-well junction. Due to this junction, still 70% of the leakage current is generated by the depletion regions that reach the surface, 2% is generated in the bulk of the photodiode and 28% is generated by the source of the reset transistor.

So, using this model, we can divide the (measured) leakage current of a certain pixel architecture into the various contributions. For the pixels described here, the depletion at the photodiode edge at the surface is the main source of the total leakage current in the pixel. Furthermore, the contact area of the reset transistor, an n^+/p-well region, contributes seriously to the total leakage current of a pixel.

III. DIFFERENT DARK CURRENT MECHANISMS

A. Diffusion Current and Thermal Generation

The leakage current of a p-n junction consists of diffusion current from the quasi-neutral areas and generation current from the depletion area [8]

$$J_R \cong q\sqrt{\frac{D_n}{\tau_n}}\,\frac{n_i^2}{N_A} + q\,\frac{n_i}{\tau_{gen}}\,W \qquad (2)$$

where D_n is the electron diffusivity, τ_n is the electron life time, N_A is the doping level of the p-type region assumed to be the lower concentration part of the junction, n_i is the intrinsic concentration of silicon, $\tau_{\rm gen}$ is the generation lifetime, and W is the depletion width. A similar expression holds for holes. The first term is associated with diffusion current and the second one is thermal generation current described by the Shockley–Read–Hall recombination [9]–[11].

The absolute value of the leakage current depends on the doping of the p and n regions and on the defect density (through $\tau_{\rm gen}$). Besides, thermal generation depends on the square root of the applied voltage, because of the depletion width dependency [8]

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V)} = f\left(\sqrt{(V - V_{\rm bi})}\right) \qquad (3)$$

where ε_s is the dielectric constant of silicon, N_A, N_D are doping levels of the p- and n-type regions, respectively, $V_{\rm bi}$ is the built-in potential in the junction, and V the applied voltage. So, the leakage current has the following dependence:

$$J_R \cong J_{\rm diff} + J_{\rm gen}\left(\sqrt{V}\right). \qquad (4)$$

In Fig. 5, the reverse I–V characteristics for n^+/n-well/psb, p^+/n-well and the n^+/p-well diodes are shown. The reverse characteristic of the n^+/n-well/psb diode shows approximately a square root dependence on the voltage (V to the power 0.58), which corresponds to the description given in (4). However, the n^+/p-well and p^+/n-well diodes have a different behavior. These curves can be better approximated by an exponential function. So, diffusion current and thermal generation are not sufficient to describe the reverse current of these diodes. Apparently other generation mechanisms such as tunneling and/or impact ionization are dominant.

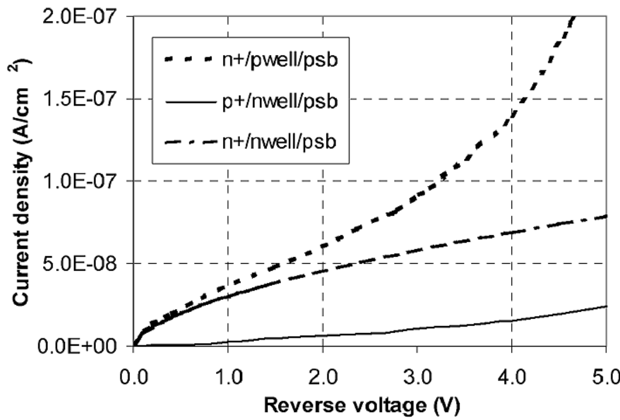

Fig. 6. Simulated leakage current densities for n+/n-well/psb, n+/p-well, and pinned p+/n-well/psb diodes.

B. Tunneling and Impact Ionization

Tunneling becomes important in highly doped junctions, which have a narrow depletion layer with relatively short tunneling distances [12]. At higher applied voltages, tunneling is usually overtaken by the impact ionization followed by avalanche breakdown. The depletion width of n$^+$/p-well or p$^+$/n-well junctions is more than twice as small as the depletion width of the n$^+$/n-well/psb junction, which increases the tunneling probability. To verify if tunneling and impact ionization can explain the fast exponential growth of the leakage current, two-dimensional (2-D) simulations have been performed using Suprem4 process simulator and MEDICI device simulator. In addition to thermal generation (Shockley–Read–Hall) band-to-band tunneling, trap-assisted tunneling [13] and impact ionization [8] mechanisms are incorporated in the simulation model. The simulated leakage current densities for n$^+$/n-well/psb, n$^+$/p-well, and pinned p$^+$/n-well/psb diodes are shown in Fig. 6.

There is a good qualitative agreement with the measurements shown in Fig. 5. Due to the tunneling and impact ionization mechanisms that are included in the simulations, the exponential behavior of the p$^+$/n-well and n$^+$/p-well diodes is described correctly. Note that the absolute values of the measurements and the simulations cannot be compared, since the simulations are not calibrated. From the simulations, it is found that already for low voltages (around 3 V) tunneling and impact ionization are the main mechanisms of the leakage generation for n$^+$/p-well and p$^+$/nwell junctions, while for n$^+$/n-well/psb it is still negligible in comparison with the Shockley–Read–Hall generation.

Both tunneling (band-to-band and trap-assisted) and impact ionization mechanisms depend strongly on the electric field inside the structure [12], [14]. The reverse current can be expressed as the sum of different contributions depending on the maximum electric field in the structure, depletion width, temperature, and dopings, with coefficients depending on the electric field and critical electric field [14]

$$J_R = \frac{A(F_m, F_{\mathrm{crit}})(J_{\mathrm{btb}} + J_{\mathrm{tat}}) + B(F_m, F_{\mathrm{crit}})(J_{\mathrm{SRH}} + J_{\mathrm{diff}})}{1 - \mu(F_m, F_{\mathrm{crit}})} \tag{5}$$

where F_m is the maximal electric field, F_{crit} is the electric field of the breakdown, J_{btb}, J_{tat}, J_{SRH}, and J_{diff} are the band-to-band, trap-assisted, Shockley–Read–Hall, and diffusion current densities, respectively, and μ is the parameter which determines the avalanche. J_{diff} and J_{SRH} were already discussed. J_{btb} and J_{tat} depend exponentially on the electric field

$$J_{\mathrm{btb}} \sim V \left(\frac{F_m}{F_0}\right)^{3/2} \exp\left(-\frac{F_0}{F_m}\right)$$
$$J_{\mathrm{tat}} \sim W \frac{F_\Gamma}{|F_m|} \left[\exp\left(\frac{F_m}{F_\Gamma}\right)^2 - \exp\left(\frac{F_m W_0}{F_\Gamma W}\right)^2\right]$$

with

$$F_\Gamma = \frac{\sqrt{24 m^* (kT)^3}}{q\hbar} \tag{6}$$

where V is the applied voltage, F_0 is a constant which depends on the temperature through the temperature dependence of the bandgap, W is the depletion width, W_0 is the depletion width at zero bias, and m^* is the effective mass of carriers. The strong electric field dependence explains the exponential behavior of the leakage current of the n$^+$/p-well and p$^+$/n-well diodes.

C. Temperature Dependence

The temperature dependence of the thermal generation current and diffusion current is mainly determined by the intrinsic concentration of silicon, which is of the first order in the generation term and of the second order in the diffusion term [see (2)]. The intrinsic concentration of silicon depends on the temperature in the following way [8]:

$$n_i = \sqrt{N_C N_V} \exp\left[-\frac{E_g}{2kT}\right] = A \left(\frac{T}{300}\right)^{3/2} \exp\left[-\frac{E_g}{2kT}\right] \tag{7}$$

where N_C and N_V are the carrier densities and E_g is the energy bandgap. When tunneling mechanisms are important, the temperature dependence of the leakage is mainly determined by the temperature dependence of the bandgap [see (6)]. At high voltages when impact ionization is the main mechanism and at avalanche breakdown the leakage current generation does not depend on the temperature any more.

In Fig. 7, the graphs for (a) n$^+$/n-well/psb and for (b) n$^+$/p-well b) are shown where the logarithm of the measured leakage current at different applied voltages are plotted versus 1000/T together with n_i and n_i^2 dependencies. As can be seen the temperature behavior of these two junctions is quite different. For n$^+$/n-well/psb, all the measured values of the current (on a logarithmic scale) are on straight lines that have smaller slopes than n_i^2. This indicates that already for a reverse bias of 0.15 V the diffusion current—proportional to n_i^2—is much smaller than the thermal generation current, which is proportional to n_i. At a 1-V reverse bias, the measured points are parallel to the n_i (T) curve, so the thermal generation is the main mechanism of the leakage generation. This situation remains up to 20 V, very close to the avalanche breakdown. Apparently the wide depletion reduces the probability of tunneling. Beyond 22 V, the avalanche starts and the temperature dependence disappears.

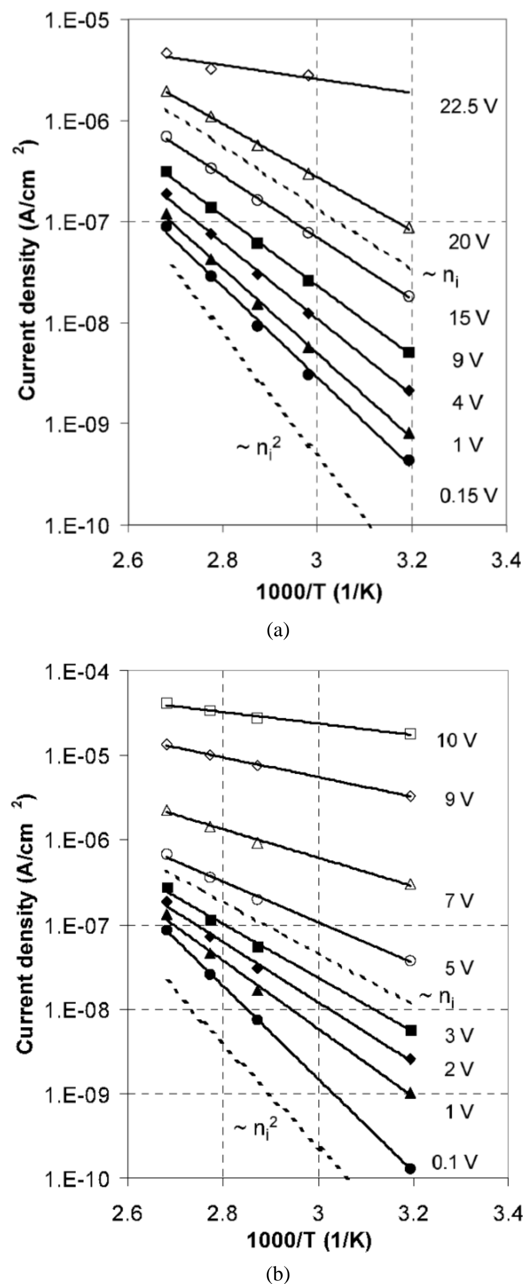

Fig. 7. Measured leakage current (in semi-logarithmic scale) at different applied voltages (a) for n+/n-well/psb and (b) for n+/p-well plotted versus 1000/T together with temperature dependencies of n_i and n_i^2.

For the n$^+$/p-well junction at very low reverse voltages (0.1–0.5 V), diffusion from the quasi-neutral regions is the main mechanism for leakage generation. Up to 2 V—about the voltage of sensor operation—the diffusion current still plays a role, because straight lines are not completely parallel to the n_i line. At 3 V, the leakage is generated thermally in the depletion, but already at 5 V the slope decreases. This implies that caused by the higher dope concentrations at the junction generation mechanisms become important that are less temperature-dependent, such as tunneling and impact ionization. While the reverse voltage grows, the temperature dependence gets weaker and disappears at avalanche.

As a summary in Fig. 8, we demonstrate the comparison between simulated (a) and measured (b) leakage current at 40 °C for the n$^+$/p-well, p$^+$/n-well/psb, and n$^+$/n-well/psb diodes. Comparison of absolute current density values cannot be made, because the simulations were not fully calibrated. Deviations in structure dimensions and inaccuracies in doping profiles and carrier lifetimes result in a different order of magnitude between the measurements and the simulations. However, if we focus on the trends, we see a quite good agreement between simulations and measurements. This resemblance shows which dark current generation mechanisms are responsible for the leakage current at every reverse bias voltage.

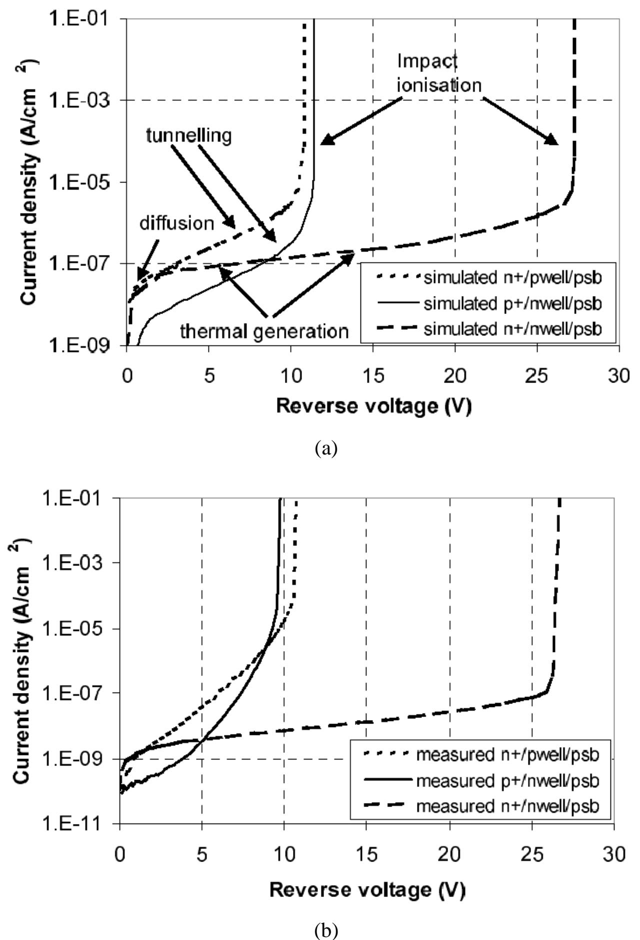

Fig. 8. (a) Simulated and (b) measured leakage current versus reverse voltage at 40 °C for the n+/p-well, p+/n-well/psb, and n+/n-well/psb diodes.

IV. Dark Current Analyses of Pixel Architectures

Knowing the reverse voltage dependencies of the various junctions and the leakage generation mechanisms, we are able to analyze the dark current behavior of the various pixel architectures in more detail. As an example we will briefly discuss, the n+/n-well/psb pixel architecture of Fig. 3(b). In Fig. 9 the reverse $I(V)$ characteristic of the n$^+$/n-well/psb pixel matrix measured at 40 °C is shown. The measured data has been fitted by the sum of two functions: one with square root voltage dependence and one with exponential voltage dependence. From the evaluation of the diode test structures (Fig. 5), we know that the square root dependent contribution can be ascribed to the n$^+$/n-well/psb junction while the exponential

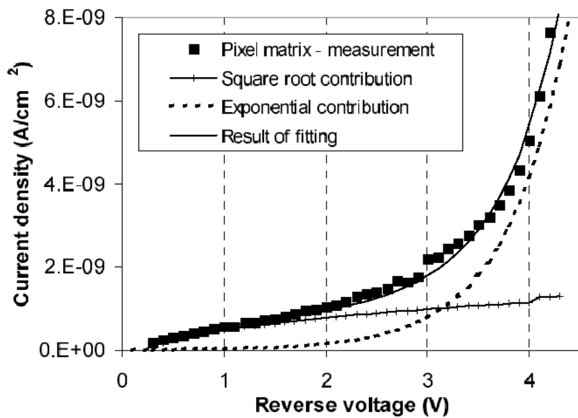

Fig. 9. Reverse I–V characteristic of the n+/n-well/psb pixel matrix measured at 40 °C and fitted by the sum of a square root and an exponential voltage dependence contribution.

contribution is due to the n^+/p-well. So the fast growing of the dark current at voltages above 2 V is caused by the leakage current of the reset transistor source and not due to thermal generation current in the photodiode.

V. Conclusion

We have evaluated dedicated diode and pixel matrix test structures fabricated in Philips' 0.35-μm CMOS baseline process to study the dark current behavior of the various pixel architectures for active pixel CMOS image sensors in detail. From the investigation of the diodes the area and length dependent contributions to the leakage current have been determined for three different structures: n^+/p-well, n^+/n-well/psb, and p^+/n-well/psb. It is shown that using these contributions the dark current of different pixel architectures can be modeled very well. We found that for the three pixel variants described here about 70% of the total dark current in a pixel is coming from the depletion of the photodiode edge at the surface and about 17%–28% is caused by the leakage of the source region of the reset transistor.

The various leakage generation mechanisms have been described and compared with the reverse I–V characteristics of n^+/n-well/psb, p^+/n-well, and n^+/p-well diodes. In the voltage range from 1 to 15 V the reverse characteristic of the n^+/n-well/psb diode shows approximately a square root dependence. The wide depletion reduces the probability of tunneling, leaving the thermal Shockley–Read–Hall generation as the main leakage mechanism. The n^+/p-well and p^+/n-well diodes can better be approximated by an exponential function due to the dominancy of band-to-band tunneling, trap-assisted tunneling, and impact ionization caused by the higher dope concentrations at the junction. At low voltages, especially for highly doped junctions, diffusion current from the quasi-neutral regions is also important. The theoretical discussion has been confirmed by the temperature dependence of the diode leakage measurements and by device simulations using MEDICI.

With the reverse voltage dependencies of the various junctions and the leakage generation mechanisms we can describe and understand the dark current behavior of the various pixel architectures in detail. In case of n+/n-well/psb pixel architecture it is shown that the reverse bias dependence of the dark current is composed of two contributions, one from the photodiode and one from the source of the reset transistor. The last one is responsible for the fast exponential growth of the reverse current due to the n+/p-well junction. Note that the working method and the theoretical description of the dark current mechanisms presented in this paper can be used for investigation and optimization of future more advanced CMOS imaging technologies.

Acknowledgment

The authors would like to thank D. Hermes for his valuable technical assistance and A. Heringa of Philips ED&T for the helpful discussions and TCAD support.

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In 1987, he joined the Philips–Bosch joint venture Broadcast Television Systems (BTS), Breda, The Netherlands, where he worked on the implementation of the first CCD image sensors in professional cameras and later on the introduction of aspect ratio switchable 16 : 9/4 : 3 cameras. In 1997, he joined Philips Research, Eindhoven, The Netherlands, and later Philips Semiconductors to work on the development of CMOS image sensors.

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In 1988, he joined the Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on very high-speed CCD delay lines. Later on he worked on various CCD imagers. In 1995 he started with CMOS imagers and became a Senior Device Engineer, involved with all aspects of the pixel design for CMOS imaging for the Product Line Imaging in Philips Semiconductors.

Edwin Roks (M'90) was born in Breda, The Netherlands, on July 5, 1964. He received the B.Sc. degree in 1985 and in the M.Sc. degree in 1990, both in electrical engineering from the Technical University Eindhoven, The Netherlands, and the Ph.D. degree from Twente University, Enschede, The Netherlands, in 1994. His dissertation was on advanced CCDs.

In 1985, he entered military service where he became an officer and lectured at the Royal Military Academy. In 1989, he joined the Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on semiconductor lasers and CCD's for imaging. Since 1993, he has been active as a Project Manager of different imaging projects both for CCD and CMOS imaging. In 1997 and 1998, he was a Member of the Selection Committee for "Detectors, Sensors and Display's" at the International Electron Devices Meeting (IEDM). In 1997 and 2002, he was a Member of the Organizing Committee of the IEEE Workshop on CCD's and Advanced Image Sensors and in 1999 and 2000 a Member of the Technical Program Committee of the European Solid State Device Research Conference (ESSDERC). Since 2001, he has been a Department Manager R&D for CMOS Imagers and a MT member of Product Line Imaging in Philips Semiconductors.

Albert J. P. Theuwissen (SM'95–F'02) was born in Maaseik, Belgium, on December 20, 1954. He received the degree in electrical engineering from the Catholic University of Leuven, Belgium, in 1977. His thesis work was based on the development of supporting hardware around a linear CCD image sensor. He received the Ph.D. degree in electrical engineering in 1983. His dissertation was on the implementation of transparent conductive layers as gate material in the CCD technology.

From 1977 to 1983, his work at the ESATLaboratory of the Catholic University of Leuven focused on semiconductor technology for linear CCD image sensors. In 1983, he joined the MicroCircuits Division of the Philips Research Laboratories, Eindhoven, The Netherlands, as Member of the Scientific Staff. Since that time he was involved in research in the field of solidstate image sensing, which resulted in the project leadership of respectively SDTV- and HDTVimagers. In 1991, he became Department Head of the Imaging Devices division, including CCD as well as CMOS solidstate imaging activities. He is author or coauthor of many technical papers in the solidstate imaging field and issued several patents. He is member of editorial board of the magazine *Photonics Spectra*. In March 2001, he became part-time Professor at the Delft University of Technology, the Netherlands, where he teaches courses in solid-state imaging and coaches Ph.D. students in their research on CMOS image sensors. In 1995, he authored a textbook *Solid State Imaging with Charge Coupled Devices*.

Dr. Theuwissen was a member of the International Electron Devices Meeting paper selection committee in 1988, 1989, 1995, and 1996. He was co-editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES Special Issues on SolidState Image Sensors, May 1991 and October 1997, and of *IEEE Micro* special issue on Digital Imaging, November/December 1998. He acted as general chairman of the 1997 IEEE International Workshop on Charge-Coupled Devices and Advanced Image Sensors. He is member of the Steering Committee of the aforementioned workshop and founder of the Walter Kosonocky Award, which highlights the best paper in the field of solid-state image sensors. During several years he was a member of the technical committee of the European Solid-State Device Research Conference. Since 1999 he is a member of the technical committee of the International Solid-State Circuits Conference. For the same conference he is acting as vice-chair in the European ISSCC Committee and member of the overall Executive Committee. In 1998 he became an IEEE Distinguished Lecturer. He is a member of SPIE.