

Leakage Power Reduction in CMOS VLSI Circuits

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ABSTRACT

Leakage power has become a serious concern in nanometer CMOS technologies. In the past, the dynamic power has dominated the total power dissipation of CMOS devices. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption. In the past many methods had been proposed for leakage power reduction like forced stack, sleepy stack, sleepy keeper, dual sleep approach etc. using techniques like transistor sizing, multi-V_{th}, dual-V_{th}, stacking transistors etc. In this paper, new methods have been proposed for the leakage power reduction in 90nm technology. The proposed methods will be compared with the previous existing leakage reduction techniques. The result is simulated using Microwind 3.1 in 90nm CMOS technology at room temperature.

Keywords

Leakage power, Dynamic power, Multi-threshold, Transistor stacking, Variable body biasing

1. INTRODUCTION

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries, threshold voltages must also decrease to gain the performance advantages of the new technology, but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current.

Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, in this paper several novel approaches for reducing both leakage and dynamic power with minimum possible area and delay trade off are proposed.

For the most recent CMOS feature sizes (e.g., 90nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18 μ technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to 0.09 μ and 0.065 μ , static power has become a great challenge for current and future technologies.

Technology scaling is one of the driving forces behind the tremendous improvement in performance, functionality, and power in integrated circuits over the past several years. Power dissipation has become a very critical design metric with miniaturization and the growing trend towards wireless communication. For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This to an extent reduces the dynamic (switching) power dissipation. However, the subthreshold leakage current increases exponentially thereby increasing static power dissipation [1]. Leakage current is the current that flows through a transistor when it is switched off. It depends on gate length, oxide thickness and varies exponentially with threshold voltage, temperature and other parameters.

Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. Power consumption has two components: Dynamic Power and Leakage power [2]. The dynamic power is consumed only when the circuit performs a function and signals change. Leakage or static power is consumed all the time, i.e., even when the circuit is idle. It is unnecessary and one would like to eliminate it [3]. Scaling and power reduction trends in future technologies will cause subthreshold leakage currents to become an increasingly large component of total power dissipation.

Leakage power mainly depends upon subthreshold leakage current, which increases with the decrease in threshold voltage. To reduce leakage power, several techniques have been proposed, including transistor sizing, multi-V_{th}, dual-V_{th}, optimal standby input vector selection, stacking transistors, dual V_{dd}, etc.

2. POWER DISSIPATION FACTORS

In CMOS, power consumption consists of leakage power and dynamic power. Dynamic power includes both switching power and short circuit power. Switching power is consumed when the transistors are in active mode and short circuit power is consumed when a pull-up and pull-down network are

on turning on and off. For 0.18u and above leakage power is small compared to dynamic power but, 0.13u and below leakage power is dominant. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation [4].

Static power dissipation is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The subthreshold leakage current increases exponentially, thereby increasing static power dissipation.

The leakage current of a transistor is mainly the result of reverse biased PN junction leakage and Sub threshold leakage. Compared to the subthreshold leakage, the reverse bias PN junction leakage can be ignored. The Subthreshold conduction or the subthreshold leakage or the subthreshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in subthreshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. [5].

It is given by:

$$I_{sub} = I_{s0} \exp\left(\frac{V_{gs}-V_{th}}{V_T}\right) \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (1)$$

$$I_{s0} = \mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} V^2 e^{1.8} \quad (2)$$

where μ_0 is the zero bias electron mobility, n is the subthreshold slope coefficient, V_{gs} and V_{ds} are the gate to source voltage and drain-to-source voltage, respectively, V_T is the thermal voltage, V_{th} is the threshold voltage, C_{ox} is the oxide capacitance per unit area, and W_{eff} and L_{eff} are the effective channel width and length, respectively. Due to the exponential relation between V_{th} and I_{sub} , an increase in V_{th} sharply reduces the subthreshold current.

3. LEAKAGE CURRENT REDUCTION

Reduction in threshold voltage results in the increase in sub-threshold leakage current. One of challenge with technology scaling is the rapid increase in subthreshold leakage power due to V_t reduction. In such a system it becomes crucial to identify techniques to reduce this leakage power component. The development of digital integrated circuits is challenged by higher power consumption [6].

Leakage current is a primary concern for low-power, high-performance digital CMOS circuits. The exponential increase in the leakage component of the total chip power can be attributed to threshold voltage scaling, which is essential to maintain high performance in active mode, since supply voltages are scaled. Numerous design techniques have been proposed to reduce standby leakage in digital circuits. Leakage power has become a serious concern in nanometer CMOS technologies, and power-gating has shown to offer a viable solution to the problem with a small penalty in performance [7].

Devices which are operated on battery are either idle (Standby) or Active mode. Leakage power can be divided in to two categories based on these two modes [8]:

- 1) Leakage Control in Standby Mode: Techniques like Power gating and super cutoff CMOS are used for leakage reduction in standby mode. In these techniques, circuit is cutoff from the supply rails, when it is in idle state.
- 2) Leakage Control in Active Mode: Techniques like forced stacking and sleepy stack can be used during the run time or active mode for leakage current reduction.

Leakage is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology. To reduce leakage power, many techniques have been proposed, including dual-V_{th}, multi-V_{th}, optimal standby input vector selection, transistor stacking, and body bias.

Multiple thresholds can be used to deal with the leakage problem in low-voltage high-performance CMOS circuits. The dual-V_{th} assignment is an efficient technique for decreasing leakage power. In this method, each cell in the standard cell library has two versions, low V_{th} and high V_{th}. Gates with low V_{th} are fast, but have high subthreshold leakage, whereas gates with high V_{th} are slower but have much reduced subthreshold leakage. The generation, distribution, and dissipation of power are at the forefront of current problems faced by the integrated circuit industry. The application of circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems [9]. Already existing methods like stack, sleepy stack, and sleep transistor are shown in Figure 1-5.

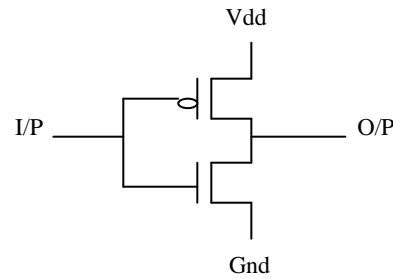


Fig 1: Base Case

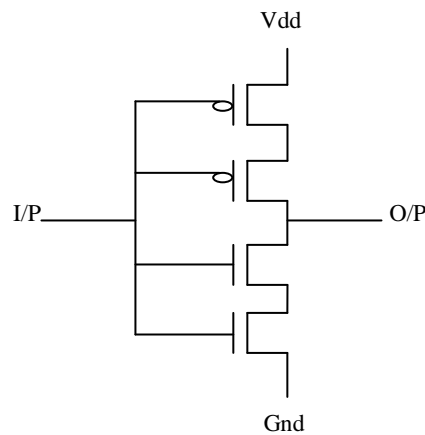


Fig 2: Forced Stack

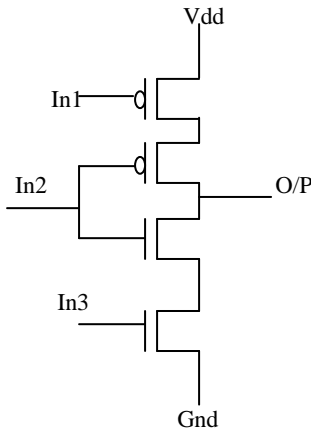


Fig 3: Sleep Transistor

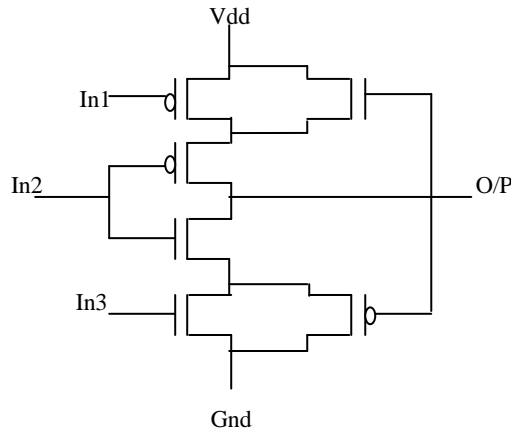


Fig 4: Sleepy Keeper

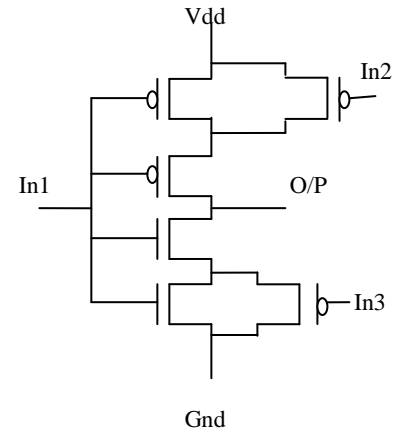


Fig 5: Sleepy Stack

The base case circuit shown in Figure 1 contains only the PMOS network and the NMOS network and there exists no method to reduce leakage. It is a state saving technique and has a minimum area requirement.

Another technique to reduce leakage power is to stack the transistors. The effect of stacking the transistor results in the reduction of subthreshold leakage current when two or more transistors are turned off together. Figure 2 shows its structure. The stack approach uses a stack effect by breaking down an existing transistor into two half size transistors [10]-[12]. The forced stack approach can achieve huge leakage power saving while retaining the logic state. When the two transistors are turned off together, induced reverse bias between the two transistors results in subthreshold leakage current reduction. Forced stack inverter does not use the high V_{th} (threshold) transistor.

Circuit optimization provides Low power and high performance. Circuit optimization can be obtained through simultaneous gate sizing and threshold voltage (V_t) assignment [13]-[14]. Sleep transistor method provides good reduction in leakage power, but it is a state destructive technique. It is shown in Figure 3. State -destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors. These types of techniques are also called gated V_{dd} and gated-GND (note that a gated clock is generally used for dynamic power reduction). The sleep transistors are turned off when the logic circuits are not in use. By isolating the logic networks using sleep transistors, the sleep transistor technique dramatically reduces leakage power during sleep mode. High threshold voltage is used for sleep transistor. Both dynamic and leakage power reductions can be achieved through threshold voltage adjustment [15].

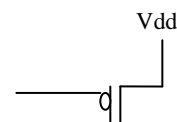
Sleepy keeper technique uses the traditional sleep transistors with two additional transistors to save state during sleep mode. Dual threshold voltages can also be applied in the sleepy keeper approach to reduce subthreshold leakage current [16]. In the traditional CMOS design the NMOS are placed always at the pull down network, because it is well known that NMOS transistors are not efficient at passing V_{dd} . On the other hand PMOS transistors are placed at the pull up network because PMOS transistors are not efficient at passing GND. But in Sleepy keeper approach as shown in Figure 4, an additional single NMOS transistor placed in parallel to the

pull-up sleep transistor connects V_{DD} to the pull-up network. When in sleep mode, this NMOS transistor is the only source of V_{DD} to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of '0' in sleep mode, given that the '0' value has already been calculated, the sleepy keeper approach uses this output value of '0' and a PMOS transistor connected to GND to maintain output value equal to '0' when in sleep mode.

The sleepy stack approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Figure 5 shows its structure. The sleep transistor and the stacked transistor in each network are made parallel. Here the width of the sleep transistors is reduced. Changing the width of the sleep transistors may provide additional tradeoffs between delay, power and area. The activity of the sleep transistors in sleepy stack is same as the activity of the sleep transistors in the sleep transistor technique. The sleep transistors are turned on during active mode and turned off during sleep mode. Sleepy stack structure achieves ultra low leakage power consumption during sleep mode while retaining the exact logic state. But the main drawback of this sleepy stack technique is that it increases area a lot.

4. PROPOSED MODELS

In this section, new leakage power reduction techniques are introduced. In the figure 6, first proposed technique has been shown which sleep transistor approach with NMOS, PMOS is and NMOS sleep transistors are used for leakage power reduction and an extra NMOS is added. Because sleep transistor technique is a state destructive technique, to retain the state NMOS is used here in this proposed method. Sleep transistors have high threshold voltage, i.e., multi-threshold technique is used here. Transistor stacking technique is also involved here in this method for the purpose of reducing leakage current during active mode or run time. Sleep transistors reduce leakage current during idle mode.



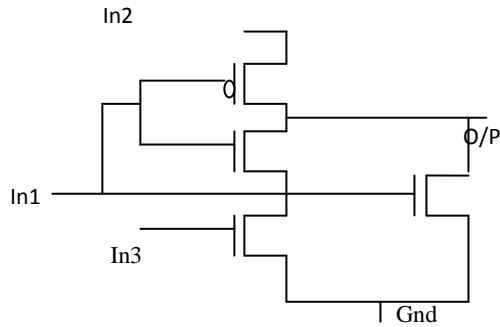


Fig 6: Sleep Transistor approach with NMOS

In figure 7, the second proposed sleep forced NMOS technique has been shown.

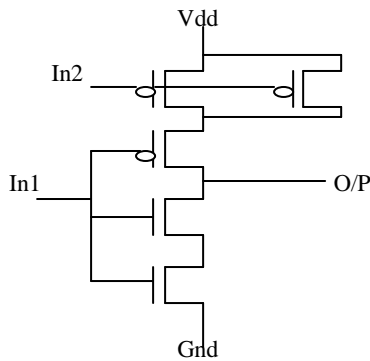


Fig 7: Sleep forced NMOS stack

In this concept of the forced stack technique and the sleep transistor technique is used. Forced sleep works during active mode and during sleep mode. The sleep transistors of forced sleep method operate similar to the sleep transistors used in the sleep transistor technique in which sleep transistors are turned on during active mode and turned off during sleep mode. The sleep forced NMOS stack method can achieve ultra-low leakage power consumption. To reduce leakage power stacking of the transistors is done here. The effect of stacking the transistor results in the reduction of subthreshold leakage current, whenever two or more transistors are turned off together.

Variable body biasing technique is used for the leakage power reduction. Third proposed technique Variable body biasing

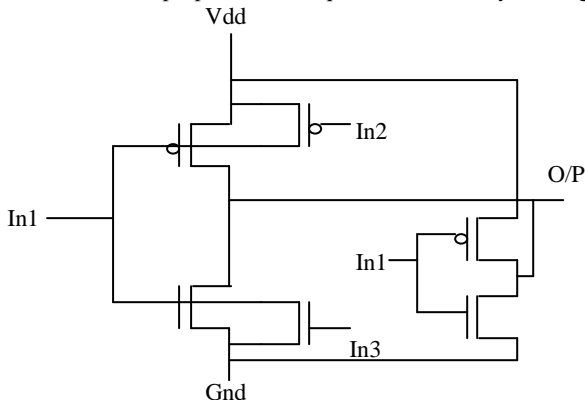


Fig 8: Variable body biasing with bypass

with bypass is shown in figure 8. Bypass is used for retaining the state at the output. The source of one of the PMOS sleep transistor is connected to the body of other PMOS sleep transistor for having so called body biasing effect. Similarly, for the NMOS sleep transistor.

Variable body biasing is increasing the threshold voltage for the purpose of reducing the leakage power. Because increase in threshold voltage results in decrease in leakage current. As mentioned above, sleep transistor technique is combined with variable body biasing technique. The sleep transistor is a state destructive technique, to get the exact state at o/p; bypass has been included in this method.

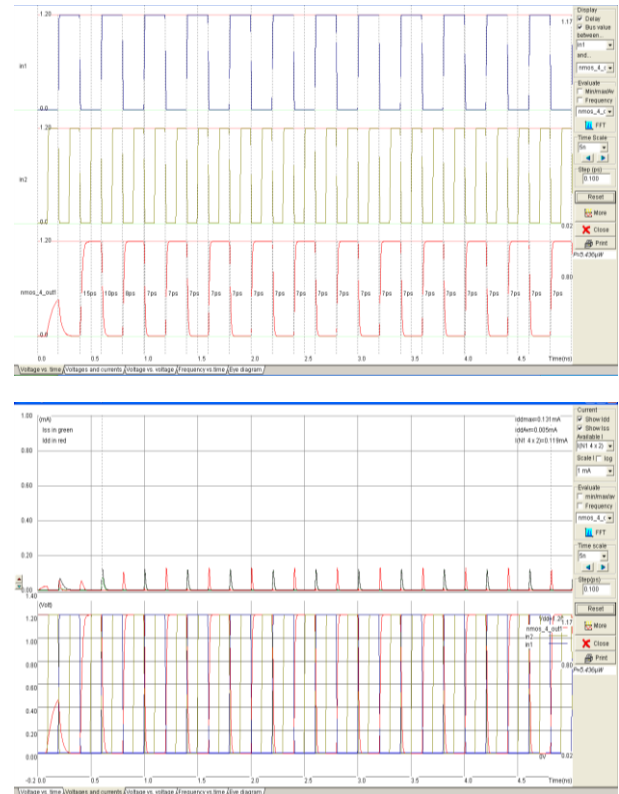


Fig 9: Sleep Transistor Approach with NMOS

5. SIMULATIONS AND RESULTS

In this section, simulations of the proposed methods are shown. Simulations are obtained in Microwind Tool. First step in obtaining the simulations is to compile the Verilog file in Microwind 3.1. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Microwind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Microwind. After that simulations are performed on the layout.

Simulations of proposed methods are shown below in figure 9-11. Simulations shown in these figures include the waveform of Voltage vs. Time and Voltage vs. Current. The corresponding simulations of sleep transistor approach with NMOS are shown in Figure 9. It can be observed from waveform that the performance obtained from the sleep

transistor approach with NMOS is very good as compared to conventional sleep transistor approach. Delay is also less and maximum current in this new approach is more.

Simulations of Sleep forced NMOS stack are shown in Figure 10. This new approach has low power consumption, good performance, more maximum current as compare to techniques like stack, sleepy keeper, sleep transistor approach etc.

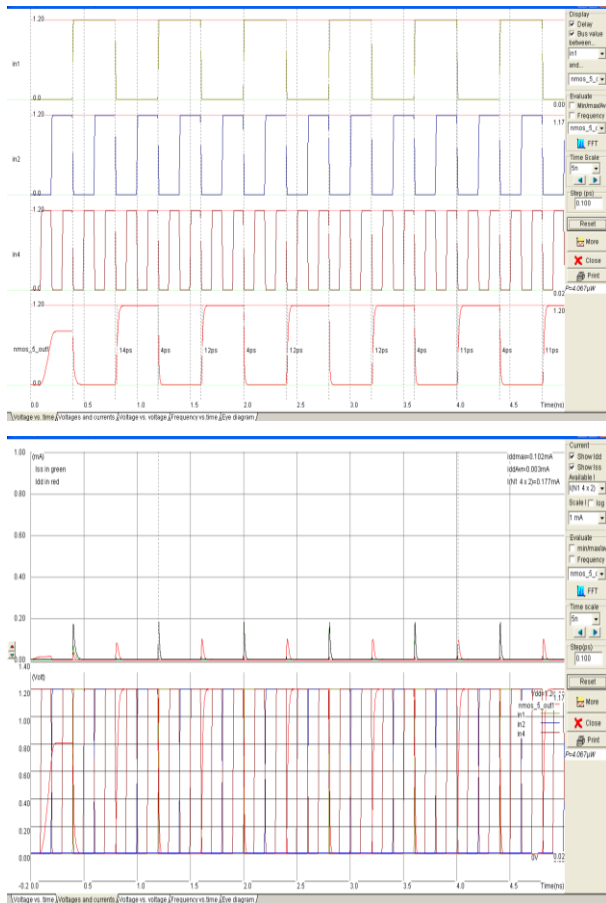


Fig 10: Sleep Forced NMOS Stack

Figure 11 shows the simulations of Variable body biasing with bypass technique. This technique has less delay, large maximum as compare to base case and conventional techniques. Variable body biasing with bypass has reduced the leakage current to minimum as shown in waveforms.

Simulation results of the proposed methods are compared with base case in Table 1 and with conventional techniques in terms of power, delay, maximum current, area and performance in the Table 2. It can be observed from the comparison tables that, there is a considerable reduction in power, leakage current and delay in the proposed method as compare to base case i.e. inverter and conventional techniques.

6. CONCLUSIONS & ACKNOWLEDGEMENTS

Scaling down of the technology has led to increase in leakage current. Nowadays, a leakage power has become more dominant as compared to Dynamic power. Leakage current is a primary concern for low-power, high-performance digital

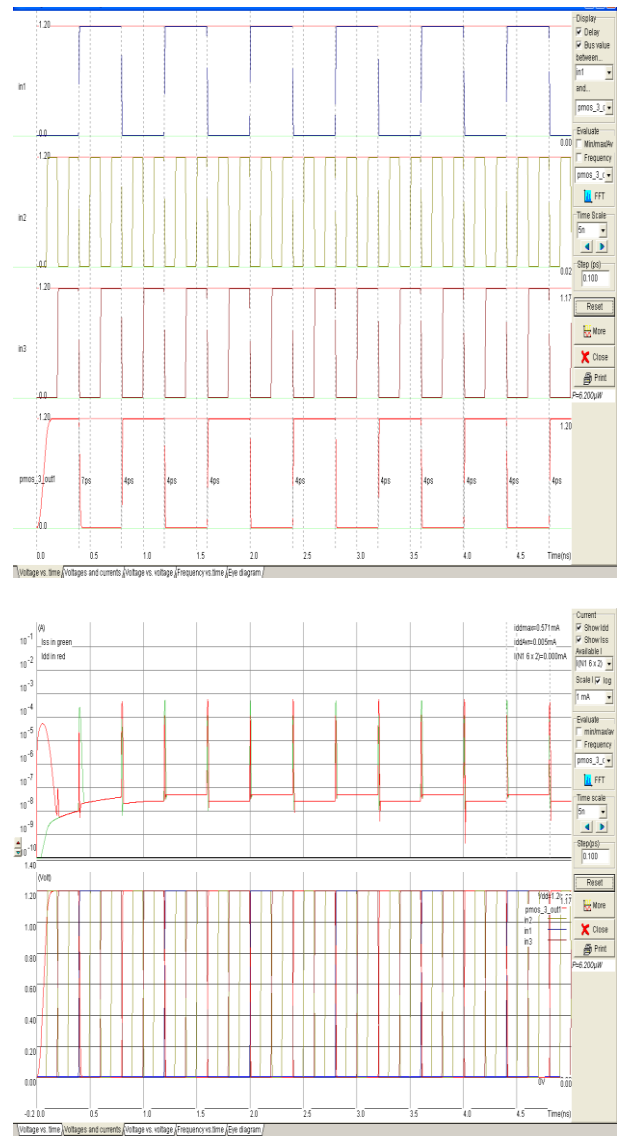


Fig 11: Variable Body Biasing with Bypass

CMOS circuits. In this paper, the efficient methodologies have been proposed for reducing leakage current in VLSI design. The proposed methods results in ultra low static power consumption with state saving.

Proposed designs have low delay, good performance, and these techniques are also more area efficient than the existing techniques and are having small leakage current. The proposed technique Variable body biasing with bypass is power efficient as well as it is providing more maximum current than base case i.e. inverter and also has the least leakage current among all the techniques discussed in this paper. The results are simulated using Microwind 3.1 tool in 90nm technology at room temperature.

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Table 1. Comparison Table of base case and proposed Leakage Reduction Techniques

Technique Parameter	Base Case	Sleep Transistor Approach with NMOS	Sleep Forced NMOS Stack	Variable Body Biasing with Bypass
Power(μ W)	11.176	4.067	5.436	6.200
Delay(ps)	9	1.5	12.5	3.5
Current(mA)	0.286	0.102	0.131	0.571
Area (μ m ²)	13.86	40.02	34.50	43.74
Performance	Good	Good	Good	Good
Leakage Current(mA)	0.341	0.177	0.119	0.00

Table 2. Comparison Table of existing and proposed Leakage Reduction Techniques

Technique Parameter	Forced Stack	Sleepy Stack	Sleepy keeper	Sleep transistor	Sleep transistor with NMOS	Sleep forced NMOS stack	Variable body biasing with bypass
Power (μ W)	8.782	6.014	5.514	2.747	4.067	5.436	6.200
Delay (ps)	20	9	41.5	4.5	1.5	12.5	3.5
Current(mA)	0.097	0.130	0.100	.096	0.102	0.131	0.571
Area(μ m ²)	28.50	50.22	50.22	33.06	40.02	34.50	43.74
Performance	Good	Good	Poor	Poor	Good	Good	Good

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