

# Less jitter sensitive NTF design for NRZ multi-bit continuous-time Delta-Sigma modulators

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**Abstract:** This paper studies the clock jitter error in multi-bit continuous-time Delta-Sigma modulators with non-return-to-zero (NRZ) feedback waveform. It proposes a few useful formulas for the design of a less jitter sensitive NTF. The analytic results and MATLAB simulations show that in the design of an NTF, there is a trade-off between the in-band quantization noise and the jitter induced noise of the modulator.

**Keywords:** Delta-Sigma modulator, continuous-time, NTF, jitter.

**Classification:** Integrated circuits

## References

- [1] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time Delta-Sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 6, pp. 661–676, June 1999.
- [2] H. Shamsi, O. Shoaie, and R. Doost, "Analysis of the Clock Jitter Effects in a Time Invariant Model of Continuous Time Delta Sigma Modulators," *IEICE Trans. Fundamentals*, vol. 89, no. 2, pp. 399–407, 2006.
- [3] L. Hernandez, A. Wiesbauer, S. Paton, and A. Di Giandomencio, "Modelling and optimization of low pass continuous-time sigma delta modulators for clock jitter noise reduction," *Proc. IEEE International Symposium Circuits Syst.*, vol. 1, pp. 1072–1075, May 2004.
- [4] R. Tortosa, J. M. de la Rosa, A. Rodriguez-Vazquez, and F. V. Fernandez, "Analysis of clock jitter error in multibit continuous-time Sigma Delta modulators with NRZ feedback waveform," *Proc. IEEE International Symposium Circuits Syst.*, vol. 4, pp. 3103–3106, May 2005.
- [5] R. Schreier and G. C. Temes, "Understanding Delta-Sigma Data Converters," John Wiley and Sons, Inc., first edition, 2005.
- [6] J. G. Kenney and L. R. Carley, "Design of Multibit Noise-Shaping Data Converters," *Analog Integrated Circuits and Signal Processing Journal*, vol. 3, pp. 259–272, 1993.

## 1 Introduction

Continuous-time Delta-Sigma modulators (CT DSM's) are a proper candidate for high speed, low power and moderate accuracy applications but they suffer from the jitter of the clock severely. Since the time-domain simulation of the jitter is very time-consuming, so it is beneficial to find analytic methods to predict the jitter effects [1, 2]. The analytic approaches prove that the jitter induced noise of the modulator depends on both the input signal characteristics and the NTF of the modulator [3, 4]. Although in [3] a criterion for the design of a less jitter sensitive NTF is proposed, however it is not straightforward. In section.2 the formulas of [2] are modified for multi-bit CT DSM and the trade-off of the design of a less jitter sensitive NTF is explained. In section.3 the proposed formulas are verified by a few MATLAB simulations and finally the paper is concluded in section.4.

## 2 Less Jitter Sensitive NTF Design

### 2.1 Accumulation of the Quantization Noise

The NTF design of a multi-bit CT DSM has an important influence on the jitter induced noise of the modulator [3]. The CLANS methodology is usually used to extract the NTF of a multi-bit DSM. The CLANS instruction of the Schreier tool-box is explained as follows [5, 6]:

$$\text{NTF} = \text{clans}(\text{order}, \text{OSR}, Q, r_{\max})$$

*Order*: The order of NTF.

*OSR*: The over-sampling ratio.

*Q*: The upper bound of quantization levels used by the fed-back quantization noise. It points to the accumulation of quantization error.

*r<sub>max</sub>*: The maximum radius for the NTF poles.

Consider a modulator with an m-bit mid-rise quantizer (i.e. N-level,  $N = 2^m$ ). Assume that the allowable input range of the quantizer is between  $-V_{ref}$  and  $+V_{ref}$ . So the step size of the quantizer,  $V_{LSB}$ , is identical to  $\frac{2V_{ref}}{N}$ . For a null input condition, both theoretical and simulation results prove that the modulator output swing is approximately between  $(-0.5Q + 0.5)V_{LSB}$  and  $(+0.5Q - 0.5)V_{LSB}$  [5, 6]. If a designer doesn't use the Scherier toolbox, the accumulation of the quantization noise,  $Q$ , can be easily determined with a null-input simulation of the modulator. Making use of the mentioned fact, in the following paragraphs it will be shown that the parameter  $Q$  has an important influence on the jitter sensitivity of the modulator.

### 2.2 Estimation of the Jitter Induced Noise for a Null Input Condition

In this section the jitter induced noise of the modulator is studied for a null input condition. The assumption of the null input condition simplifies our analyses and helps us predict the clock jitter error appropriately [3].

A real NRZ feedback waveform of a CT DSM is shown in Fig. 1 (a), involving the clock jitter error. This waveform can be decomposed to an

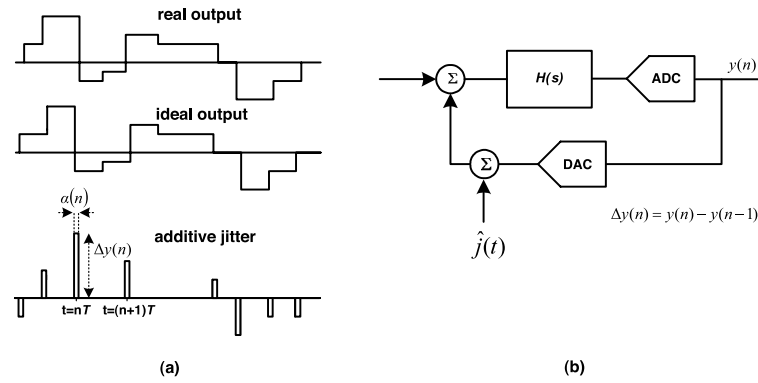


Fig. 1. (a) Clock jitter modeling. (b) The additive noise of the clock jitter

ideal output waveform and an additive jitter waveform as shown in Fig. 1 (a). Therefore the error of the clock jitter can be modeled as an additive noise in the feedback loop of the CT DSM, as shown in Fig. 1 (b) [2].

The additive jitter waveform  $\hat{j}(t)$  is described in relation (1) where  $\Pi(\cdot)$  denotes to a rectangular function as shown in relation (2). The parameter  $T$  points to the clock period of the system. Moreover; the random parameters  $\alpha(n)$  and  $\Delta y(n)$  represent the amount of the time deviation and the amplitude of  $\hat{j}(t)$  at  $t = nT$  respectively. Since for a null input condition the output swing of the modulator is approximately between  $(-0.5Q + 0.5)V_{LSB}$  and  $(+0.5Q - 0.5)V_{LSB}$ , therefore  $\Delta y(n)$  belongs to a set as shown in relation (1) [5, 6].

$$\hat{j}(t) = \sum_{n=-\infty}^{+\infty} \Delta y(n) \Pi\left(\frac{t - nT}{\alpha(n)}\right),$$

$$\Delta y(n) \in \{0, \pm V_{LSB}, \pm 2V_{LSB}, \dots, \pm(Q - 1)V_{LSB}\} \quad (1)$$

$$\Pi\left(\frac{t}{T}\right) = \begin{cases} 1 & |t| < \frac{T}{2} \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

Assuming the probability function of  $\Delta y(n)$  is identical to relation (3), its autocorrelation function  $R_{\Delta y}(i, k)$  is extracted as follows. The probability function of  $\Delta y(n)$  should be determined by the empirical simulation of the modulator.

$$P(\Delta y(n) = lV_{LSB}) = \begin{cases} P_l & l \in \{0, \pm 1, \dots, \pm(Q - 1)\} \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

$$R_{\Delta y}(i, k) = \begin{cases} \frac{4V_{ref}^2}{N^2} \sum_{l=-(Q-1)}^{Q-1} l^2 P_l & i = k \\ 0 & i \neq k \end{cases} \quad (4)$$

Performing a few manipulations like [2], the power spectral density of the additive jitter noise  $S_j(f)$  is obtained as shown in relation (5). In this relation  $sinc(\cdot)$  and  $f$  refer to the sinc function ( $sinc(z) = \frac{\sin(\pi z)}{\pi z}$ ) and frequency

respectively. Besides;  $p_\alpha(\cdot)$  denotes to the probability density function (pdf) of  $\alpha$ .

$$S_{\hat{j}}(f) = \frac{4V_{ref}^2}{N^2T} \sum_{l=-(Q-1)}^{Q-1} l^2 P_l \int_{-\infty}^{+\infty} \alpha^2 \sin^2(f\alpha) p_\alpha(\alpha) d\alpha \quad (5)$$

For in-band frequencies,  $S_{\hat{j}}(f)$  is approximately flat. Therefore the in-band power of the additive jitter noise  $P_{\hat{j}}$  is derived as follows:

$$P_{\hat{j}} = \int_{-f_B}^{f_B} S_{\hat{j}}(f) df = \frac{8V_{ref}^2 \overline{\alpha^2} f_B}{N^2T} \sum_{l=-(Q-1)}^{Q-1} l^2 P_l \quad (6)$$

Assuming  $\overline{\alpha} = 0$  and using the definition of  $OSR$ ,  $P_{\hat{j}}$  is rewritten as follows where  $\sigma_\alpha^2$ ,  $f_s$  and  $f_B$  denote to the variance of  $\alpha$ , sampling frequency and bandwidth of the modulator respectively.

$$P_{\hat{j}} = \frac{4V_{ref}^2 \sigma_\alpha^2}{N^2T^2 OSR} \sum_{l=-(Q-1)}^{Q-1} l^2 P_l \quad OSR = \frac{f_s}{2f_B} \quad (7)$$

### 2.3 The Effect of the Input Signal on the Jitter Induced Noise

The input signal of the modulator increases the jitter induced noise. For a large amplitude and high frequency signal, this fact is intensified more [4]. In this situation the relation (3) is not valid and the formulas of  $S_{\hat{j}}(f)$  and  $P_{\hat{j}}$  should be modified as follows:

$$S_{\hat{j}}(f) = \frac{4V_{ref}^2}{N^2T} \sum_{l=-(N-1)}^{N-1} l^2 P_l \int_{-\infty}^{+\infty} \alpha^2 \sin^2(f\alpha) p_\alpha(\alpha) d\alpha \quad (8)$$

$$P_{\hat{j}} = \frac{4V_{ref}^2 \sigma_\alpha^2}{N^2T^2 OSR} \sum_{l=-(N-1)}^{N-1} l^2 P_l \quad (9)$$

Since in multi-bit modulators the maximum amplitude of the input signal is about  $\frac{N-Q}{N} V_{ref}$  [5, 6], so the maximum power of the input signal  $P_s$  is calculated as follows:

$$P_s = \frac{1}{2} \left( \frac{N-Q}{N} \right)^2 V_{ref}^2 \quad (10)$$

Making use of relations (9) and (10), the signal to jitter induced noise ratio  $SNR_j$  is obtained as shown in relation (11). Moreover the signal to quantization noise ratio  $SNR_q$  and the signal to total noise ratio  $SNR_{total}$  are defined as shown in relations (12) and (13) respectively. In these relations  $P_q$  denotes to the quantization noise.

$$SNR_j = 10 \log \left( \frac{P_s}{P_j} \right) = 10 \log \left( \frac{(N-Q)^2 T^2 OSR}{8\sigma_\alpha^2 \sum_{l=-(N-1)}^{N-1} l^2 P_l} \right) \quad (11)$$

$$SNR_q = 10 \log \left( \frac{P_s}{P_q} \right) \quad (12)$$

$$SNR_{total} = 10 \log \left( \frac{P_s}{P_j + P_q} \right) \quad (13)$$

## 2.4 Trade-off between the Quantization Noise and Jitter Induced Noise

Although the formulas of section.2.3 are more accurate than those of section.2.2, however in this section for simplicity the formulas of section.2.2 are used to explain the design bottleneck of NTF.

As an extreme, for  $Q = 2$ , the relation (7) is simplified further as follows. The presence of  $N^2$  at the numerator of relation (14) decreases the jitter noise very much. However; as a drawback it will be shown in section.3 that the noise shaping behavior of the modulator is seriously degraded. Therefore a designer should make a compromise between the quantization noise and jitter induced noise of the modulator.

$$P_j = \frac{4V_{ref}^2\sigma_\alpha^2}{N^2T^2OSR} \quad (14)$$

As another extreme, for a large value of  $Q$ , the jitter noise of the modulator is increased greatly. This fact occurs when a designer tries to achieve an aggressive noise shaping for the CT DSM.

## 3 Simulation Results

In this section the design methodology of a 4<sup>th</sup> order less jitter sensitive 4-bit CT DSM with NRZ feedback waveform is described. The  $OSR$  of the modulator is 8. Making use of the Schreier tool-box and sweeping the parameter  $Q$ , a few loop filters  $\hat{H}(s)$  are obtained. Then the modulator is stimulated with a sinusoidal waveform (amplitude= $\frac{N-Q}{N}V_{ref}$ ,  $f_{in} = \frac{f_s}{2OSR}$ ) for various loop filters. The histogram of  $\Delta y(n)$  determines  $P(\Delta y(n) = lV_{LSB})$  for each loop filter. As an example, for  $Q = 9$ , amplitude= $\frac{7}{16}V_{ref}$  and input signal frequency of  $f_{in} = \frac{f_s}{16}$ , the probability function of  $P(\Delta y(n) = lV_{LSB})$  is depicted in Fig. 2 (a).

Making use of the analytic-empirical relation of (11),  $SNR_j$  is plotted versus  $Q$  in Fig. 2(b). In this relation  $\sigma_\alpha$  is chosen identical to  $10^{-3}T$ . This figure shows that for a small value of  $Q$ , the jitter induced noise of the modulator is decreased.

Performing a time-domain simulation, the parameter  $SNR_q$  is depicted versus  $Q$  in Fig. 2(c). In this simulation a jitter-free clock is employed. This figure shows that for a large value of  $Q$ , the in-band quantization noise of the modulator is decreased. Both Fig. 2(b) and Fig. 2(c) show that there is a trade-off between  $SNR_j$  and  $SNR_q$ . This fact complies with the rule of thumb argument of section.2.4.

Two profiles for  $SNR_{total}$  are depicted in Fig. 2 (d). The analytic-empirical profile is obtained by summing the profiles of Fig. 2 (b) and Fig. 2 (c) in a logarithmic scale. In order to verify the correctness of the analytic-empirical profile, an exactly time-domain simulation is also performed. It is considered that both methods provide identical results. As an advantage, these profiles help the designer choose  $Q$  properly. For  $Q = 5$  the transfer function of  $\hat{H}(s)$

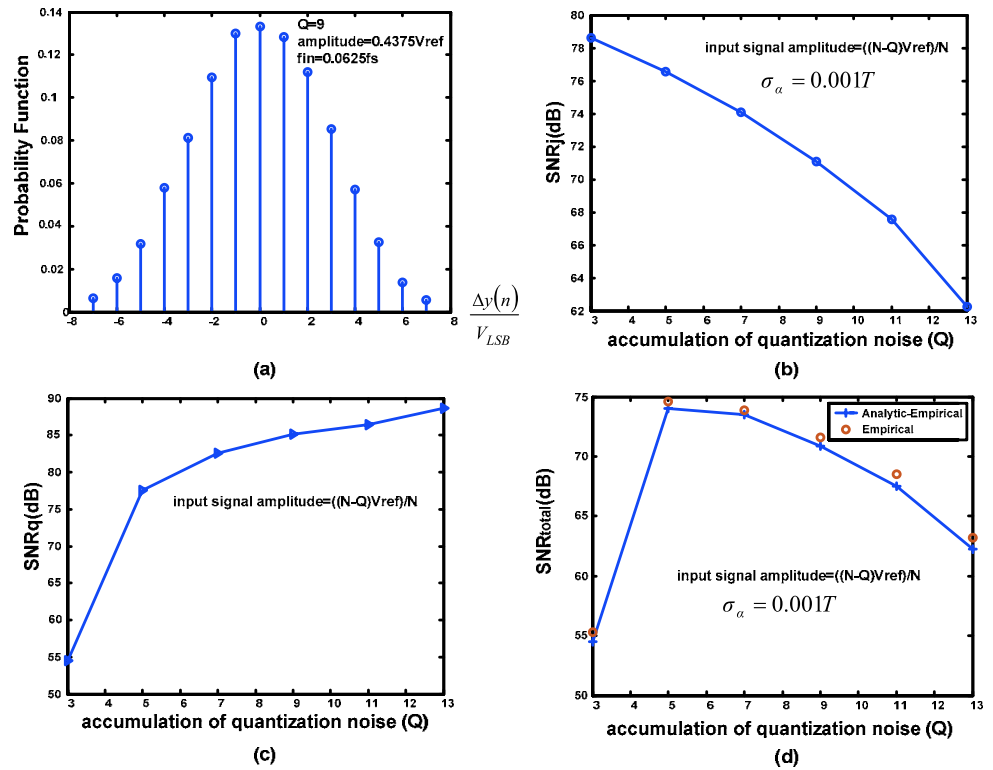


Fig. 2. (a) The probability function of  $\Delta y(n)$  (b)  $SNR_j$  (c)  $SNR_q$  and (d)  $SNR_{total}$  versus  $Q$

is obtained as follows.

$$\hat{H}(s) = \frac{-1.7104(sT + 0.4304)((sT)^2 + 0.4752sT + 0.3909)}{((sT)^2 + 0.01782)((sT)^2 + 0.1144)} \quad (15)$$

#### 4 Conclusion

This paper presents an analytic-empirical method for the estimation of the clock jitter error in multi-bit CT DSM's with NRZ feedback waveform. Making use of the definition of the parameter  $Q$ , accumulation of the quantization noise, it is shown that for a small value of  $Q$ , the jitter induced noise of the modulator is decreased but as a drawback the in-band quantization noise of the modulator is increased. In contrast for a large value of  $Q$ , the jitter induced noise of the modulator is increased but as an advantage the in-band quantization noise of the modulator is decreased. Therefore the designer should be aware about this trade-off and choose  $Q$  properly.